Isolated Quasi-Switched Boost Integrated T-Type DC-DC Converter for DC Microgrid

Daniel Ferreira
ISEL-DEEEA, Instituto Politécnico de Lisboa, Rua Conselheiro Emídio Navarro,1959-007 Lisboa, PT
CTS-UNINOVA, 2829-516 Monte da Caparica, Portugal
a47138@alunos.isel.pt

Armando Cordeiro
ISEL-DEEEA, LCEC, Instituto Politécnico de Lisboa, Rua Conselheiro Emídio Navarro,1959-007 Lisboa, PT
INESC-ID Lisboa, Rua Alves Redol, 9, 1000-029 Lisboa, Portugal
armando.cordeiro@isel.pt

Luis Rocha
ISEL-DEEEA, Instituto Politécnico de Lisboa, Rua Conselheiro Emídio Navarro, 1959-007 Lisboa, PT
INESC-ID Lisboa, Rua Alves Redol, 9, 1000-029 Lisboa, Portugal
luis.rocha@isel.pt

Enrique Romero-Cadaval
DEECE, University of Extremadura, Avda. de Elvas, s/n. Edificio Rectorado 06006, Badajoz, Spain
eromero@unex.es

Carlos Roncero-Clemente
DEECE, University of Extremadura, Avda. de Elvas, s/n. Edificio Rectorado 06006, Badajoz, Spain
carlosrc@unex.es

J. Fernando Silva
DEEC, IST, University of Lisbon, Rua Rovisco Pais, 1, 1049-001 Lisboa, PT
INESC-ID Lisboa, Rua Alves Redol, 9, 1000-029 Lisboa, Portugal
fernando.alves@tecnico.ulisboa.pt

Daniel Foito
ESTSetúbal, Instituto Politécnico de Setúbal, Campus do IPS, Estefanilha, 2914 508 Setúbal, Portugal
CTS-UNINOVA, 2829-516 Monte da Caparica, Portugal
daniel.foito@estsetubal.ips.pt

João F. Martins
Faculdade de Ciências e Tecnologia (FCT), Universidade Nova de Lisboa (UNL), (DEE), 2829-516 Caparica, PT
CTS-UNINOVA, 2829-516 Monte da Caparica, Portugal
jf.martins@fct.unl.pt

V. Fernão Pires
ESTSetúbal, Instituto Politécnico de Setúbal, Campus do IPS, Estefanilha, 2914 508 Setúbal, Portugal
INESC-ID Lisboa, Rua Alves Redol, 9, 1000-029 Lisboa, Portugal
vitor.pires@estsetubal.ips.pt

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***Abstract*— Over the last few years, there has been a high demand for new or improved isolated DC-DC to fulfill requirements of applications related with RES. In this context, this paper introduces a new isolated DC-DC converter, for use in renewable energy applications. The topology proposed contains an Active quasi-switched Boost Three-Level T-type DC-DC converter with continuous input current at the converter input side, connected to a high-frequency step-up isolation transformer, and a voltage doubler rectifier (VDR) on the output side. The steady-state analysis of the proposed converter is presented and discussed. Simulation results are presented to verify the theory and performance of the converter.**

Keywords — isolated DC-DC converter; active quasi-switched; high-voltage gain; voltage doubler rectifier.

I. INTRODUCTION

DC-DC converters play an important role in the integration of different Renewable Energy Sources (RES) into DC distribution networks, according to the desired requirements and adopted equipment interface [1]. They also have a special importance in many other applications, such as Electric Vehicles (EV), allowing to interconnect all the types of onboard electric devices operating with different voltages [2]. There is a constant research regarding the design of new DC-DC converter topologies with high-voltage gain ratio and buck-boost ability to extend the operation of RES, and other power sources, all over the available voltage ranges, extracting efficiently as much energy as possible. Several isolated and non-isolated power converters have been proposed recently in literature to achieve simultaneously these features [3]-[6] in several application. Nevertheless, there are numerous other aspects, such as galvanic isolation, safety, protection, costs, dynamic performance, filtering/EMC/noise emission requirements, input continuous currents, multistage energy conversion structures and intrinsic control algorithms, efficiency, reliability, weight-volume ratio, voltage stress over power devices and some others issues that should be taken into account during the design of the DC-DC converters. Usually the most important aspects are the voltage gain ratio, galvanic isolation requirement, effective cost, efficiency, input continuous currents, filtering/EMC/noise emission, followed by the simplicity of the circuit (reduced component count). Other aspects can also be considered whenever possible, but is quite difficult to include all the desired features.

For DC distribution network applications, the design of the front-end isolated DC-DC converter is usually one of the most challenging aspect because this stage is almost always associated with high currents in the primary part of the DC-DC converter, leading to high switching and conduction losses in the power devices which reduces the efficiency. Also, the galvanic isolation interface is responsible for high weight, volume and overall dimensions but this is essential to provide the necessary isolation and safety requirements. There main solutions adopted for such applications use configurations such as full-bridge DC-DC converter and dual-active-bridge (DAB) composed by a high-frequency duty ratio controlled Voltage Source Inverter (VSI) in the primary side of a high-frequency step-up isolation transformer and a controlled Voltage Source Inverter or a rectifier and filter assembly in the secondary side of the transformer, depending on bidirectional or unidirectional requirements [6]–[9]. In these configurations the isolation transformer is usually designed with a large turns ratio for effective step-up voltage This solution is known as direct step-up isolated DC-DC converter without input voltage pre-regulation, which offers less complexity, less component count and higher reliability but, on the other hand, presents less voltage regulation which becomes incompatible with certain applications. Usually, when high-voltage gain ratios are required, more auxiliary boost circuits are introduced before the isolated DC-DC [10], creating a solution with proper input voltage pre-regulation. This auxiliary boost circuit, which can be a single DC–DC converter with separate modulation and control [11] or can comprise an Z-source network, benefits from integrated modulation and control [12]–[16]. Z-source source networks are an emerging

technology in various power conversion applications, in which no additional active switches are required to provide step-up capability [17].

This paper is devoted to a new power circuit topology to be implemented in the front-end DC-DC converter for distributed power generation. The topology proposed contains an Active Z-Source Buck-Boost Three-Level T-type DC-DC converter with continuous input current at the converter input side, reduced passive element count, low voltage stress on additional power devices and also the self-balance capacitor voltage capability. The converter is also connected to a high-frequency step-up isolation transformer with a voltage doubler rectifier (VDR) in the output side. This circuit is ideal for applications were the input voltages are subject to large variations as usually happens with RES and were stable and higher voltages are required such as DC Microgrids.

II. Description of Proposed Topology

This paper proposes a single-stage Active Z-Source Three-Level T-type with reduced component count which is expanded from the switched-capacitor based Active Z-Source two-level inverter topology in [18]. Therefore, the proposed inverter has all inherent merits of the switched-capacitor based Active Z-Source such as single-stage power conversion, shoot-through (ST) immunity, improved voltage gain, continuous input current, low ST current stress, and low voltage stress on the capacitors, diodes, and switch. Since one of the main limitation of the Z-Source inverters is the impact of the ST state in the converter operation, the proposed three-level solution allows to minimize the duty-cycle of the ST state when high-voltage gain ratio is required. The proposed topology is illustrated in Fig. 1 where the additional SA power device combined with the bidirectional power devices S5 and S6 allow to provide the multilevel operation to minimize the duty-cycle of the ST.

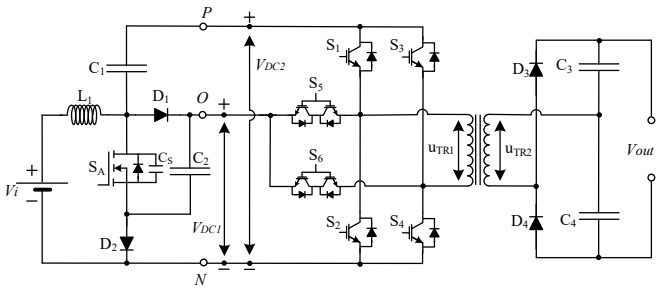


Fig. 1. Circuit diagram of proposed Active Z-Source Buck-Boost Three-Level T-type isolated DC-DC converter.

III. Analysis of the Proposed Converter

In this paper the purpose is to perform a PWM modulation and at the same time adjust the primary voltage of the transformer through the ST duty-cycle of the active quasi-switched circuit to achieve the desired output voltage. In the steady-state analysis of the proposed converter, it is assumed ideal power devices and the stray inductances of the circuit are very small and thus ignored. It is also assumed a small snubber capacitor to perform ZVS operation of the power device SA and the deadtime intervals associated to this operation is very short and ignored in this analysis. Finally, the capacitors C1 and C2 are considered large enough to maintain a fixed capacitor voltage. The operation of this converter can be divided in two different modes, ST state and non-ST state. Fig. 2 shows a simplified circuit in the ST state, where all the main power devices are turned on.

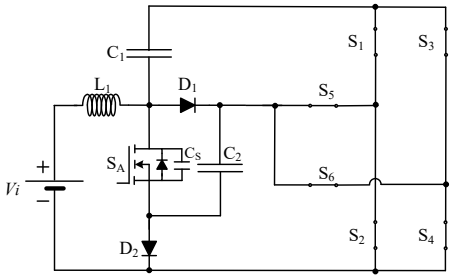
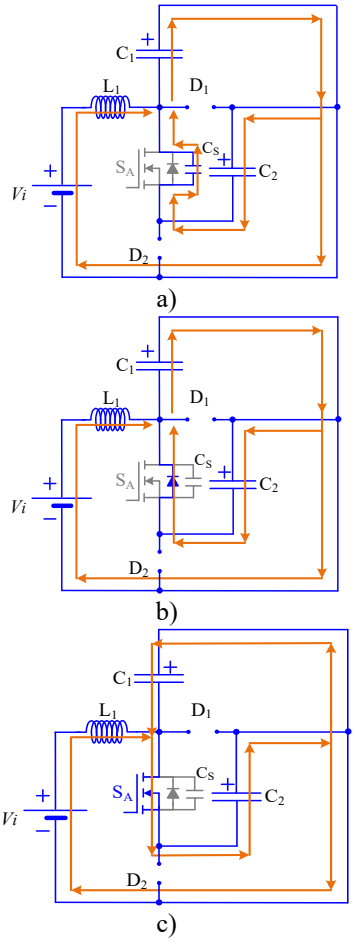
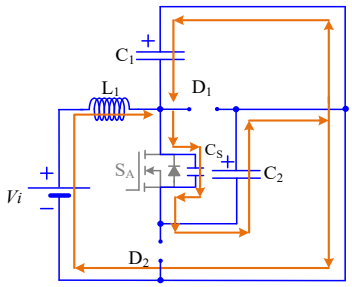


Fig. 2. Simplified topology during the ST operation.

During the ST state the operation can be divided in four different sub-states to achieve ZVS considering the snubber capacitor Cs. These modes are presented from Fig.3a) to Fig.3d). In Fig. 3(a) the main power devices of the single-phase inverter and the power devices of the T-type bridge are turned on at the same time, while switch S_A is turned off. Diodes D1 and D2 are reverse-biased and the currents are reduced to zero. In this sub-state the snubber capacitor Cs discharges until zero voltage and therefore the Drain–Source voltage over the power device S_A is zero. This means that, in the control strategy is necessary to create a small time delay to discharge the capacitor Cs. Fig. 3(b) shows the next sub-state which happens when the capacitor Cs start to charge inversely which force the body diode of S_A diode to turn on to freewheel the current. Notice that this procedure forces the balance of the capacitors C_1 and C_2 since they are in parallel. In this sub-stage S_A is turned on with near zero-voltage switching (ZVS) because the direction of the current is reversed through the body diode of S_A. This sub-stage ends when the current flowing to the body diode of S_A reaches zero. In this two sub-stages the inductor L_1 stores energy.





d)

Fig. 3. Operation of the circuit in ST mode considering a snubber circuit and stray inductances in the circuit, assuring ZVS operation.

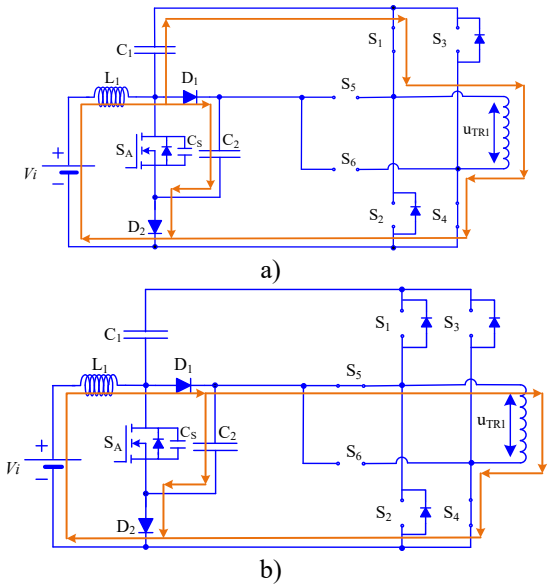
Fig. 3(c) shows the next sub-stage when the current starts to flow over the power device S_A, charging the capacitor C_1 and discharging capacitor C_2. The inductor L_1 continues to store energy in this sub-stage. Finally, in the last sub-stage, represented in Fig. 3(d), the power device S_A is turned off at hard switching, while the ST state remains in all the other power devices of the proposed converter. The voltage stress over S_A is equal to voltage difference between capacitors C1 and C2, which is very small.

In the ST state, while the switch S_A is turned on, the inductor current in L1 increases and the following equations are obtained as (see Fig 3c)):

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = v_{in} + v_{C1} \\ v_{C1} = v_{C2} \end{cases} \quad (1)$$

$$\begin{cases} v_{DC2} = 0 \\ I_{L1} = C_2 \dfrac{dv_{C2}}{dt} - C_1 \dfrac{dv_{C1}}{dt} \end{cases} \quad (2)$$

Fig. 4 shows the operation modes in non-ST state to apply +VDC2, VDC1 and zero voltage.



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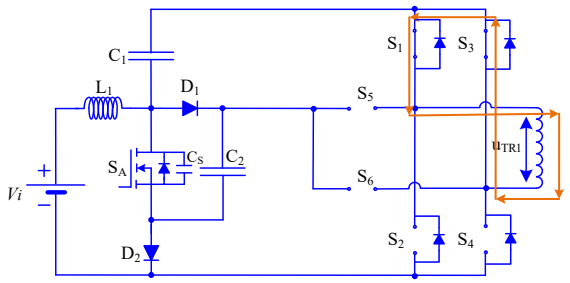

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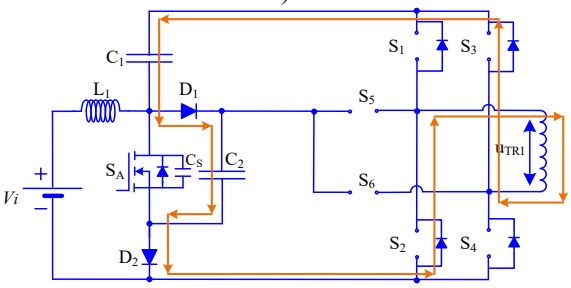


d)

Fig. 4. Operation of the circuit in non-ST mode to obtain the different voltage in the transformer input: (a) +VDC2, (b) +VDC1, (c) zero voltage, (d) freewheeling mode.

In the non-ST state, the inductor current in L1 decreases and the following equations are obtained as (see Fig. 4a)):

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = v_{in} - v_{C2} \\ v_{DC2} = v_{C1} + v_{C2} \end{cases} \quad (3)$$

$$\begin{cases} I_{L1} = C_2 \dfrac{dv_{C2}}{dt} + I_o \\ C_1 \dfrac{dv_{C1}}{dt} = I_o \end{cases} \quad (4)$$

The average capacitor voltages of the proposed inverter is calculated by applying the volt-second balance principle to inductor L1, from (1) to (4), as presented in (5).

$$\begin{cases} (V_{in} + V_{C1})D + (V_{in} - V_{C2})(1-D) = 0 \\ V_{C1} = V_{C2} \end{cases} \quad (5)$$

Solving (5) is possible to obtain (6) as the relationship between the capacitor voltages and the input voltage.

$$V_{C1} = V_{C2} = \frac{1}{(1-2D)} V_{in} \quad (6)$$

Since the output voltage V_{DC2} is given by (7) (see fig. 1 to identify V_{DC2}), the gain of the converter regarding the input voltage is obtained by (8), which is the maximum DC voltage on the inverter leg in non-ST state.

$$V_{DC2} = V_{C1} + V_{C2} = 2V_C \quad (7)$$

$$V_{DC2} = V_{C1} + V_{C2} = \frac{2}{(1-2D)} V_{in} \Rightarrow G_1 = \frac{V_{DC2}}{V_{in}} = \frac{2}{(1-2D)} \quad (8)$$

In the same way, V_{DC1} is given by (9).

$$V_{DC1} = V_{C2} = \frac{1}{(1-2D)} V_{in} \Rightarrow G_2 = \frac{V_{DC1}}{V_{in}} = \frac{1}{(1-2D)} \quad (9)$$

Considering the transformer ratio *n* and the VDR circuit in the output, the output load voltage can be expressed by (10).

$$V_{out} = \frac{2u_{TR1}.G_1}{n} = \frac{4u_{TR1}}{n(1-2D)} = \frac{4}{(1-2D)} u_{TR2} \quad (10)$$

Table I shows all the available states for each switch and diode according with the operating principle of the proposed converter and the corresponding voltages applied to the primary high-frequency transformer. The proposed inverter has two major states: ST and Non-ST (NST).

TABLE I. SWITCHING STATES OF SEMICONDUCTOR DEVICES

State		Switches							Diodes		u_{TR1}
		S1	S2	S3	S4	S5	S6	SA	D1	D2	
ST		1	1	1	1	1	1	1	0	0	0
		1	1	1	1	1	1	0	0	0	0
NST	P	1	0	0	1	0	0	0	1	1	$+V_{DC2}$
		0	1	1	0	0	0	0	1	1	$-V_{DC2}$
	O	0	0	0	1	1	0	0	1	1	$+V_{DC1}$
		1	0	0	0	0	1	0	1	1	$-V_{DC1}$
	N	1	0	1	0	0	0	0	1	1	0
		0	1	0	1	0	0	0	1	1	0
		0	0	0	0	1	1	0	1	1	0

1 – Turn on; 0 – Turn off.

IV. VOLTAGE BOOST CONTROL OF THE DC-DC CONVERTER

Fig. 5 shows the voltage control principle of the isolated Integrated T-Type DC-DC proposed in both ST(voltage boost) and NST operating modes. This figure shows the switching pattern for the devices of the T-Type single-phase VSI. The proposed voltage control strategy is based on a classic PWM with interleaved ST and NST operation, where the ST mode is only performed during the zero voltage or during the freewheeling mode operation of the high-frequency transformer. This solution avoids deteriorate the output waveform quality of the inverter such as happens in classical Z-Source DC-DC topologies. The switching states are known as active states when one and only one switch in each phase leg conducts. To generate the ST state all the main power devices should be turned on and the voltage boost is controlled through the duty-cycle of the additional power device S_A. Notice that there are two synchronized triangular waveforms. The top triangular waveform presents a double frequency of the bottom waveform in order to assure that the ST is performed in the both cycles of the VSI waveform. This means that the operating frequency of the Quasi-Switched Boost network will be two times higher when comparing with the switching frequency of the main power devices. Notice that the top triangular waveform is compared with two constant references, V_{ref2} and $V_{ref2} + \alpha$. Where the α variable is a constant value that assure that the duration of the gate signal applied to S_A is always less than the desired ST to assure the desired ZVS operation.

Fig. 6 shows a schematic control diagram for the switching states presented in Fig. 5. Notice that, according to the desired voltage control algorithm is possible to switch from the middle voltage obtained in the T-Type connection to the full bridge VSI operation (S5→S1; S6→S3). On the other hand, when the input voltage is high enough, the ST states are eliminated, and the Quasi-Switched Boost network combined with other devices operates as a traditional VSI.

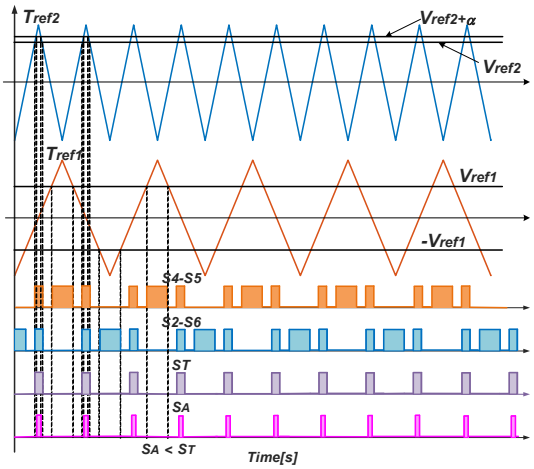


Fig. 5. Diagram of the switching states of semiconductor devices to perform voltage boost control.

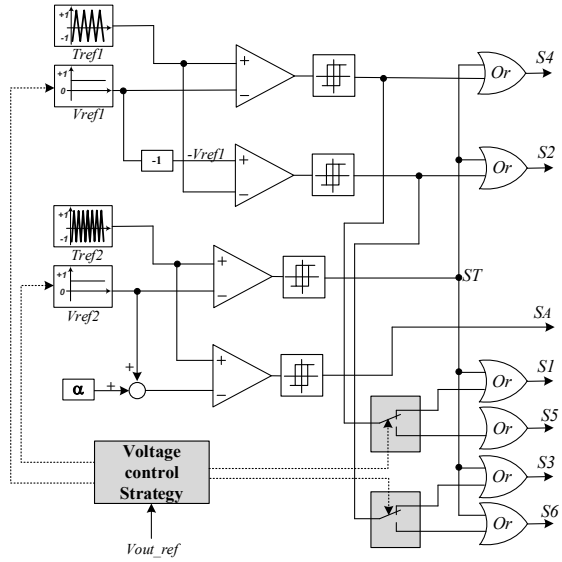
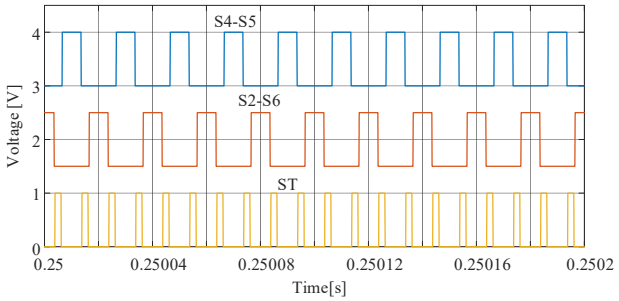


Fig. 6. Diagram of the schematic diagram of switching states to perform voltage boost control.

V. SIMULATION RESULTS

The theoretical concepts previously presented are now tested through computer-based simulations using the Matlab/Simulink software. The converter was powered by a constant 24 VDC voltage source. The passive components consisted of inductors *L1* with a value of 1 mH, and capacitors *C1=C3=C4* and *C2*, with values of 470 µF and 100 µF, respectively. The value of the snubber capacitor *Cs* selected was 1µF. High-frequency transformer with ratio n=1:3. A 50 kHz carrier frequency is utilized in a classical PWM modulator that controls the converter's operation. The simulation results for a duty-cycle of 0.23 can be seen in Figs. 7 and 8. From the results presented in Fig. 7, it is possible to see the gate signals of the main power devices (S2-S4-S5-S6) to apply half of boost voltage without ST operation (ST shown but not interleaved with NST in Fig. 7a). Fig. 7b) shows the integration of interleaved ST and NST operation when applying half of boost voltage. Some details of the ZVS operation during the turn on of power device S_A can be seen in Fig. 7c). The input continuous current (i_{L1}) can be seen in Fig. 7d). The voltages V_{DC2} and V_{DC1} are presented in Figs. 7e) and f), respectively. Figures 7g) and 7h) show the modulated voltage at the high-frequency transformer primary winding applying half of the boost voltage and voltage gain respectively, considering an input voltage *Vin* of 24V_{DC} and achieving an output voltage, *Vout* of 200V_{DC}.



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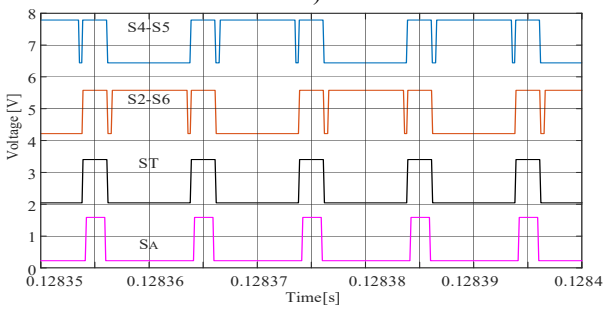

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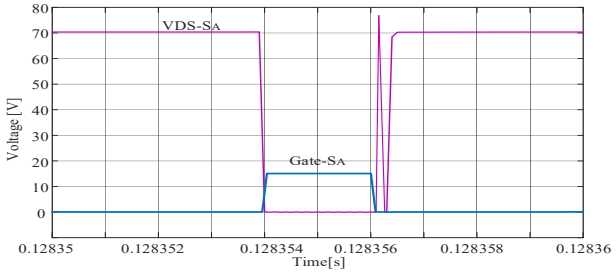

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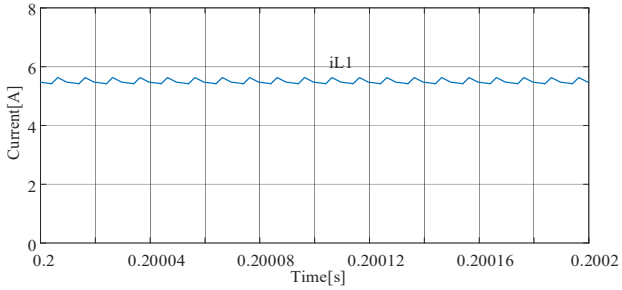

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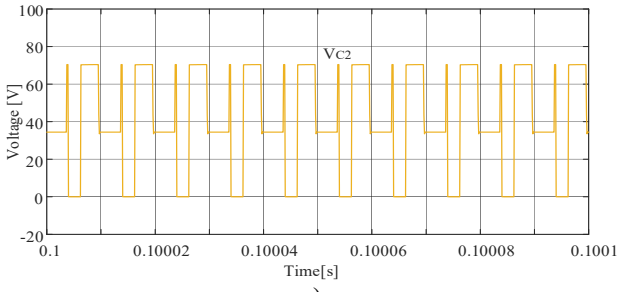

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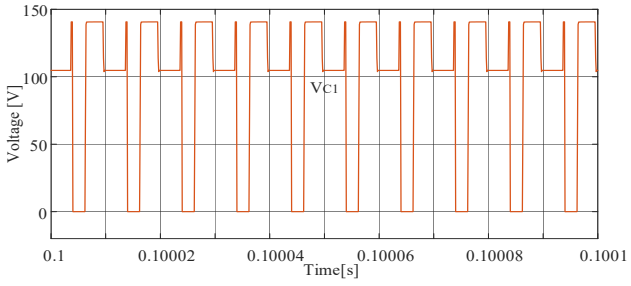

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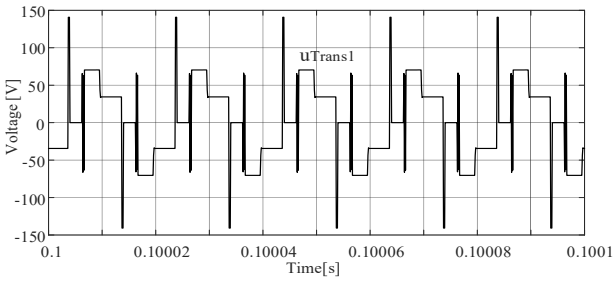

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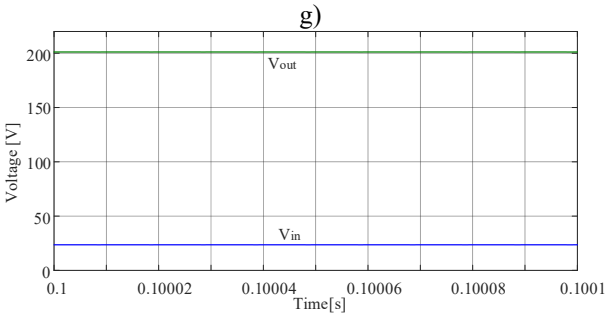
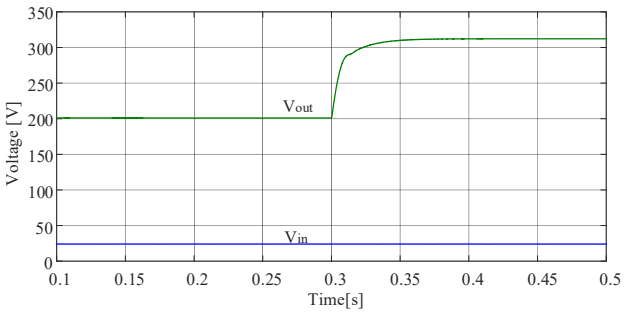


h)

Fig. 7. Simulation results of the proposed converter with D=0.23 and applying half of the boost voltage. (a) Signal gates without ST operation; (b) Signal gates with ST operation; (c) ZVS operation during the turn on of power device S_4; (d) input current (i_{L1}); (e) voltage V_{DC2} due to ST operation; (f) voltage V_{DC1} due to ST operation; (g) Voltage at the high-frequency transformer primary winding; (h) Input and output voltage.

Finally, Figs. 8a) and 8b) show the output voltage gain transition and input current transition changing from half to full boost voltage in the high-frequency transformer primary winding at t=0.3s. Note that the current overshoot is due to open-loop operation. A closed-loop control strategy can avoid this overshoot. Figure 8c) and 8d) shows some details of the input current and high-frequency transformer primary voltage applying the highest input boost voltage.



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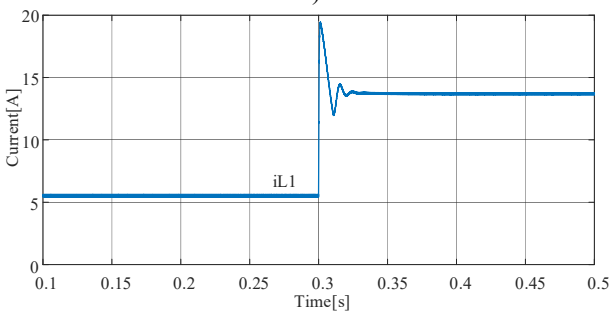

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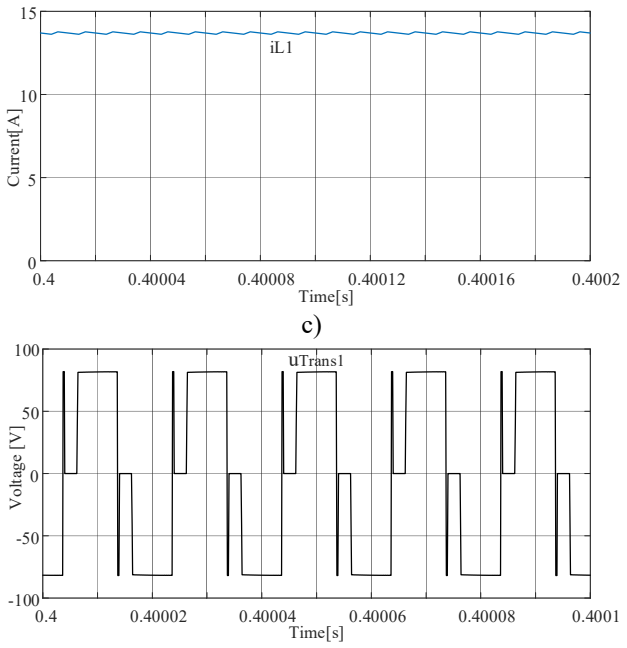

Fig. 8. Simulation results of the proposed converter with D=0.23 and applying the full boost voltage; (a) output voltage gain transition from half to full boost voltage in the high-frequency transformer primary winding at t=0.3s: (b) input current transition changing from half to full boost voltage; (c) input current in steady-state; (d) high-frequency transformer primary voltage.

VI. Conclusions

This paper presented an improved isolated Boost DC-DC converter topology that achieves high static voltage gains. The results showed that this topology offers improved voltage gain performance at lower duty-cycles, extending the capabilities of traditional Boost converter topologies. Furthermore, this converter features continuous input current and reduced voltage stress on the power switches and diodes in the primary winding, reduced passive element count and also the self-balance capacitor voltage capability. The unique combination of features in this DC-DC converter makes it an ideal choice for applications demanding extremely wide conversion ratio ranges, particularly in the realm of distributed DC networks. To validate the proposed converter performance, several simulations procedures were undertaken using the Matlab/Simulink software to perform a preliminary evaluation of the proposed solution.

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