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Limiting Internal Supply Voltage Spikes in DC-DC Converters

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***Abstract* — Implementing monolithic DC-DC converters for low power portable applications with a standard low voltage CMOS technology leads to lower production costs and higher reliability. Moreover, it allows miniaturization by the integration of two units in the same die: the power management unit that regulates the supply voltage for the second unit, a dedicated signal processor, that performs the functions required. This paper presents original techniques that limit spikes in the internal supply voltage on a monolithic DC-DC converter, extending the use of the same technology for both units. These spikes are mainly caused by fast current variations in the path connecting the external power supply to the internal pads of the converter power block. This path includes two parasitic inductances inbuilt in bond wires and in package pins. Although these parasitic inductances present relative low values when compared with the typical external inductances of DC-DC converters, their effects can not be neglected when switching high currents at high switching frequency. The associated overvoltage frequently causes destruction, reliability problems and/or control malfunction. Different spike reduction techniques are presented and compared. The proposed techniques were used in the design of the gate driver of a DC-DC converter included in a power management unit implemented in a standard 0.35µm CMOS technology.**

I. INTRODUCTION

THE growing industry of portable equipment, in order to increase the level of integration, to reduce the equipment bill of materials and weight, integrates in the same die the power management unit (PMU) and the signal processor unit generally composed by analog and digital blocks, outlining a system-on-chip (SoC) [1]. The processor unit performs the functions required for the device application and the PMU regulates the supply voltage for the processor [2].

The integration of the PMU in a SoC using a standard CMOS low voltage technology can be a design challenge even using *I/O* transistors (with higher voltage limits) if high currents and low cost packages (with bonding wires) are used.

In a PMU with a step-down DC-DC converter (buck), the components size of the off-chip LC filter should be small, in order to reduce print-circuit-board (PCB) area. However a reduced inductor value and a reduced capacitor value require a high switching frequency in order to maintain successful energy transference from battery (V_{BAT}) to the load (v_{out}).

A step down DC-DC converter, operating at high switching frequency, produces fast current variations in the path connecting the external power supply source to the internal pads. When switching off the supply current, the fast current variation produces an internal supply voltage overshoot due to the parasitic inductances inbuilt in bond wires, L_{BW}, and in package pins, L_{LF}, on the serial path connected with the switches [3]. Although the low values of these parasitic inductances when compared with the external inductor of the buck converter, L, their effects can not be neglected when using high switching frequency and high current since they are the main reasons for spikes on internal supply voltage, v_{IN}. These spikes can cause overvoltage that leads to device destruction, reliability problems or malfunctions on the converter feedback control [1],[4-5].

These supply voltage spikes can be reduced in resonant converters. The class of resonant converters uses extra circuitry connected to the output load (load-resonant) or connected to the switches (switch-resonant) to force a sinusoidal shape on current and voltage in the switches. Although, the design of zero current switching (ZCS) or zero voltage switching (ZVS) resonant converters main objective is the reduction of switching loss, it can also reduce supply voltage spikes. However, the extra circuitry used in resonant converters (inductances and capacitors) are more affordable for discrete realizations [6]. For monolithic CMOS realizations a hard switching converter with an alternative solution, inbuilt in the gate driver of the power switches is presented in this paper.

In hard switching converters, supply voltages spikes can be reduced via controlled current variations through the parasitic inductances in the power supply path, with a moderate switch turn-off and turn-on time [1].

The techniques to reduce internal supply voltage spikes were used to design a gate driver for a buck converter fabricated with a 0.35µm CMOS process. The converter input voltage range (V_{BAT}) is 1.8V to 4.2V and the output voltage (v_{out}) is programmable in the range 1.2V to 3.8V, with a maximum output load current of 180mA. The buck converter operates in discontinuous conduction mode (DCM) or in the

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frontier of continuous conduction mode (CCM). It is current controlled with variable switching frequency limited by $f_{sw} \leq 2$MHz; the controller limits the maximum current through the external inductance to 400mA.

In Section II, a conventional gate driver circuit is analyzed during the switching period. Section III presents a two slope gate driver circuit for supply voltage spikes reduction. Enhancements of two slope gate driver circuit are presented in Section IV, with a capacitive coupling scheme. Section V compares the previously presented solutions and, finally, Section VI presents the conclusions of this work.

II. CONVENTIONAL GATE-DRIVER AND TRANSITOR SWITCHING BEHAVIORAL

The simplest gate driver for the MOS power devices is a conventional buffer chain with appropriate transistor scaling [2],[7]. Fig.1 shows this conventional gate driver, detailed for the M_p power transistor (*GDRVp*), with the non-overlap sub-circuit omitted for clearness. The body parasitic diode D_n of power transistor M_n is shown because the current i_L flows through it when M_p is turned-off, in order to preserve the inductor current, until the order to turn-on M_n does not arrive from the controller (not shown). During this current switching, assuming that the external inductor current (i_L) is nearly constant, the current decrease in L_{p1} parasitic inductor (HS - High Side path) is accomplish by a equal magnitude current increase in L_{p2} parasitic inductor (LS - Low Side path). If the value of L_{p1} and L_{p2} are equal then the voltage spike on the positive supply pad (v_{IN}) is equal to voltage spike in the negative pad (*PGND*). The magnitude of this voltage spike (Δv) is given by eq. 1, assuming L_p=L_{p1}=L_{p2} and $\Delta i_1 = \Delta i_2 = \Delta i$; and $i_1 + i_2 \approx i_L$ and $i_p + i_n = i_L$.

$$\Delta v = L_p |di/dt| \quad (1)$$

The above explanation states that the voltage spike on negative supply pad (*PGND*) is almost independent of M_n turn-on time, but it is asserted by the M_p turn-off time.

Theoretical electrical models for wire bonds and for device packages have been proposed in the literature with different level of accuracy depending on the application [3],[8-9]. In this work, a lumped resistance-inductor-capacitor ($R_P L_P C_P$) parasitic model was adopted for wire bond and for package pins, but it will be represented by a parasitic inductor ($L_p = L_{BW} + L_{LF}$) for clearness (Fig.1).

In order to reduce supply voltage spikes (Δv), some design alternatives to the gate driver circuit for M_p switch are reported in the following sections, limiting the supply current slope. The gate driver circuit for M_n switch is a conventional buffering scaling chain (*DRVn*), and will be kept unchanged, when reporting the alternatives for M_p gate driver.

A. Conventional Fast Gate-Driver

Two conflict criterions can be used to design a conventional gate driver (*GDRVp*) to the M_p switch (Fig.1), with distinct results regarding turn-off time, maximum supply voltage spike, switching loss and silicon area.

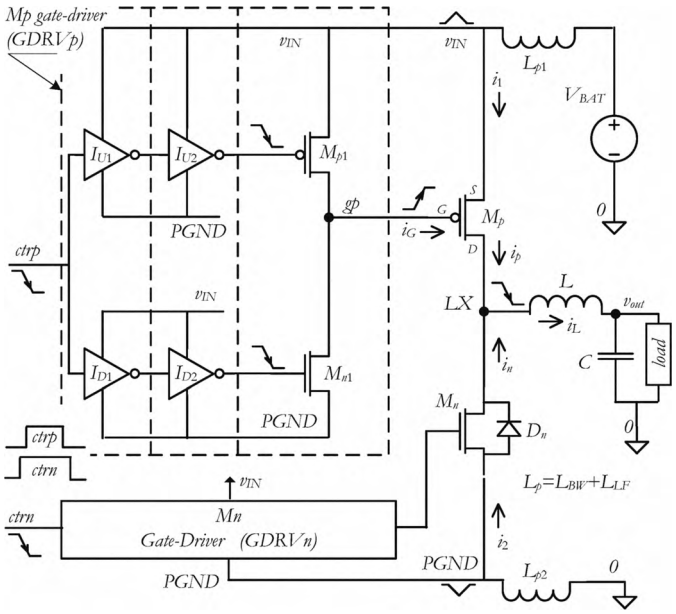

Fig. 1. Conventional gate driver circuit, detailed for M_p transistor (*GDRVp*).

A conventional gate driver designed for fast turn-off and on times will generate low switching loss, but it requires a large silicon area. When switching off 400mA with 8ns turn-off time, the spike in v_{IN} is approximately 0.8V, and the maximum M_p source-drain voltage is $|v_{SD}|_{\max} \approx$ 6.3V (with V_{BAT} = 4.2V).

B. Conventional Slow Gate-Driver

A conventional M_p gate driver designed for reduced supply voltage spikes can be obtained by slowing down the turn-off and on times, but it will cause significant switching losses. The turn-off time for M_p becomes 15ns when designing the driver in order to limit the supply voltage spike to 0.5V when V_{BAT} = 4.2V. The maximum M_p source-drain voltage is $|v_{SD}|_{\max}$ ≈ 5.8V (V_{BAT} = 4.2V).

The specifications of the step-down converter designed with a standard low-voltage CMOS technology, with a maximum switching frequency of 2MHz, demanded a M_p turn-off time of the conventional fast gate-driver (about 8ns), but it also demands a maximum supply voltage spike of the conventional slow gate driver (about 0.5V for V_{BAT} = 4.2V), in order to limit the overvoltage across M_p transistor. These two specifications are get-together simultaneously at expense of silicon area, to accommodate an enhanced two slope gate driver circuit.

In order to design a two slope gate driver circuit, the switching-off of the *p*-channel MOS transistor must be analyzed in detail.

C. pMOS Switching-off Detail

The simplified version of the *p*MOS switching-off waveforms, composed only of piecewise linear sections and without scale, are presented in Fig.2. The following analysis assumes a null parasitic inductance (L_p = 0), in order to focus on main aspects of the M_p transistor switching behavioral [1],[7],[10-11]. The analysis can be divided in four time frames: Before the first time frame M_p transistor is fully conducting in the triode

region, with a large overdrive, low v_{SDp} voltage and the current through M_p is increasing at an approximately linear rate given by $(v_{IN} - v_{out})/L$, and $i_1 \approx i_p \approx i_L$. At time frame one, when the gate voltage (v_{Gp}) of M_p starts rising, the v_{SGp} voltage starts to fall from v_{IN} to a Miller plateau level. The voltage in the internal M_p parasitic capacitors C_{GS} and C_{GD} is changing and the internal capacitors discharge-charge actions explains the difference observed at M_p drain (i_p) and source (i_1) currents: part of i_p cames from the charge of C_{GD}, but $i_p \approx i_L$. M_p maintains the triode region with a decreasing overdrive, but all the current is flowing through it.

During time frame two, M_p source-to-drain voltage (v_{SDp}) goes from its initial value ($i_1 \cdot R_{DS(on)}$) to the final value given by $v_{IN} + v_{D(on)}$, exceeding the supply voltage. The source-to-gate voltage is kept constant at the Miller plateau level and the gate current charges the C_{DS} and C_{GD}. During this time interval the M_p drain current, i_p, is almost constant, since the transistor overdrive is also constant. The M_p operation point moves from triode to saturation at the same time as the source-to-drain voltage raises.

On the third time frame, the M_p drain current, i_p falls from the predefined value toward zero at the end of interval, while the source-to-gate voltage (v_{SGp}) decreases from the Miller plateau level to the M_p threshold level $|V_{Tp}|$. During this time interval M_p transistor is operating in saturation but it is shifting to the cut-off region. The gate current, i_G, is charging-discharging the internal M_p capacitors C_{GD} and C_{GS}. In order to ensure the continuity of i_L current, that is almost constant during this time frame, the M_n body diode turns-on automatically, compensating the variation of i_p with identical variation at i_2, that flows through D_n while M_n is off. As soon as this parasitic diode turns-on, the voltage at LX node (v_{LX}) drops from its initial value ($v_{IN} - i_1 \cdot R_{DS(on)}$) to a clamped negative voltage defined by the forward bias diode.

During time frame four the M_p source-to-gate voltage drops form $|V_{Tp}|$ to zero, at the same time as the gate current (i_G) full charges-discharges C_{GD} and C_{GS}. At this time interval the drain current (i_p) is zero. The external main inductance current flows through the parasitic diode, D_n, setting $i_L = i_n = i_2$. These currents are now decreasing at a rate given by $(v_{out} + v_{D(on)})/L$. In practice, this time interval imposes a dead-time delay that avoids M_p and M_n simultaneous conduction, which would cause an undesired shoot-through current.

After time frame four, the DC-DC controller maintains M_p cut-off and it turns-on the synchronous rectifier transistor (M_n), in order to reduce power losses from $i_2 \cdot v_{D(on)}$ to $i_2 \cdot |v_{DSn(on)}|$.

The last signal waveform at Fig.2 ($|v_{SDp} \cdot i_p|$) represents the switching power losses during M_p turn-off sequence. These power losses depend on the duration of time frames two and three. The duration of all time intervals depends on tree main factors: M_p parasitic capacitors; M_p gate-driver strength; and M_p threshold and overdrive voltages.

The four time frames at Fig.2 have solid straight lines frontier definition, but HSpice waveform simulations show more flexibility to define the time frames border lines. For example, the current through M_p transistor (i_1, i_p) starts to decrease at time frame two and ends at time frame four, which is point up by *A-B* dashed line waveform at Fig.2.

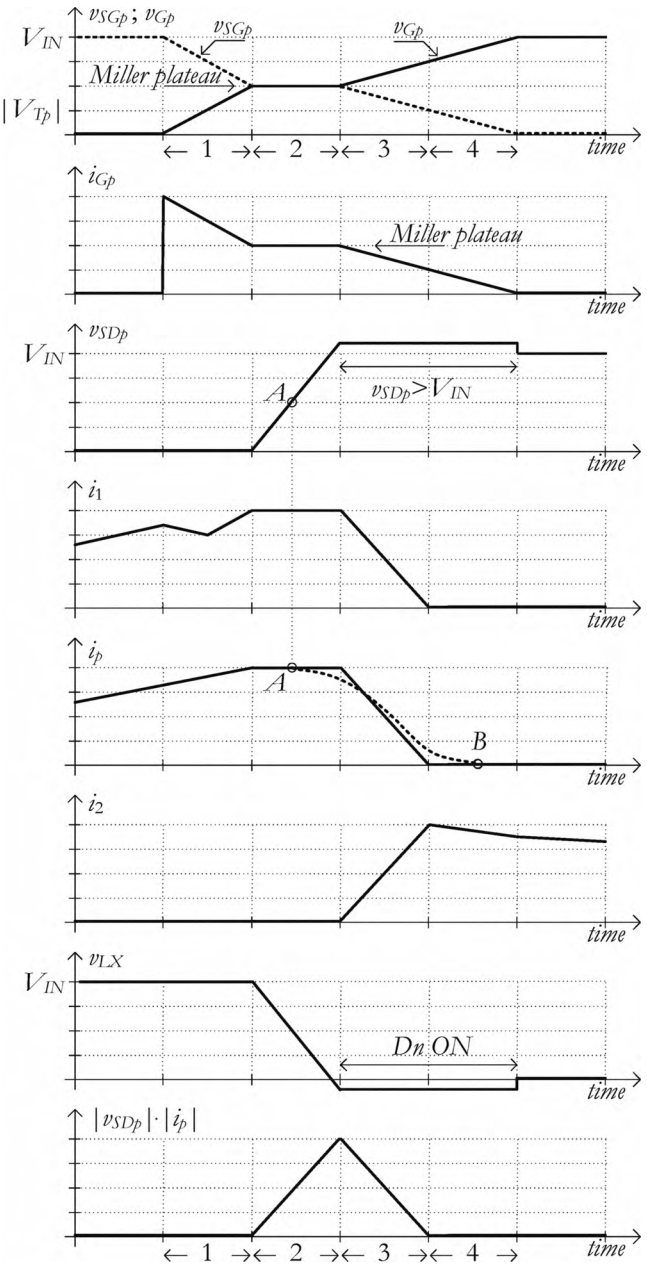

Fig. 2. Simplified waveforms when M_p switch (high side) turns-off.

The *A-B* dashed line shows a more realistic current waveform through M_p in order to define the M_p cut-off time criterion: the time from $v_{SDp} = \frac{1}{2} \cdot V_{BAT}$ (point-*A*) to null drain current (point-*B*).

The simplified waveforms at Fig.2 were sketched assuming zero parasitic inductance in the bonding wires and package pins ($L_p = 0$). Nevertheless, Fig. 2 shows that the major influence of those parasitic inductances occurs at time frame three, where the current through M_p falls to zero and the current through the *LS* path (M_n, D_n) increases with identical rate, causing supply voltage spikes in v_{IN} and *PGND*. Some influence of the parasitic inductances will also be noticeable during time frame one, when the charge-discharge of C_{GS} and C_{GD} cause variations on i_1.

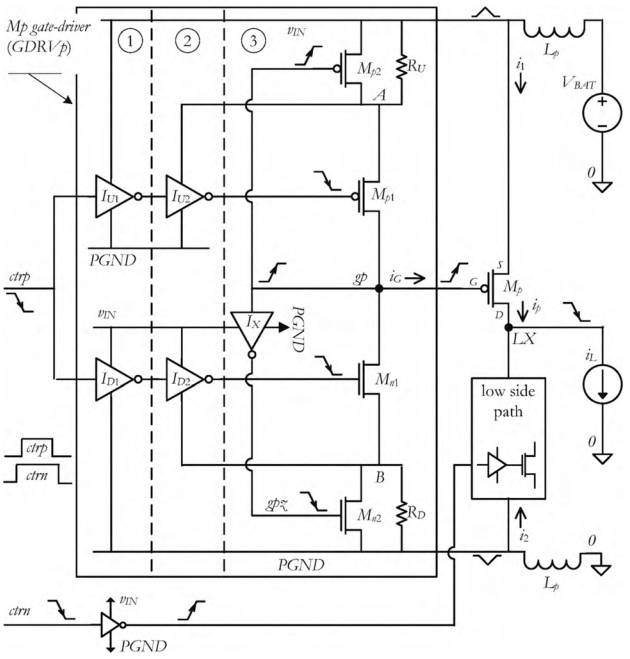

Fig. 3. Simple two slope gate driver circuit (*GDRVp*).

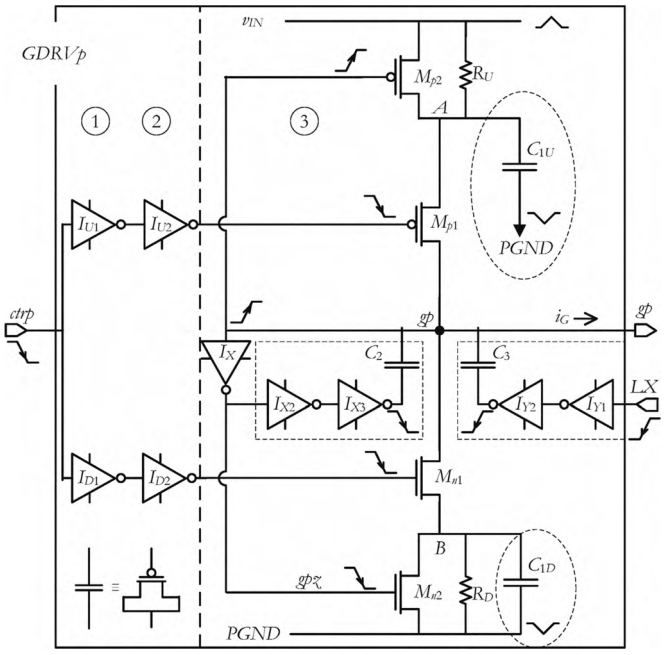

Fig. 4. Enhanced two slope gate driver circuit (all-in-one coupling).

In order to reduce the voltage spikes in v_{IN}, and *PGND* the M_p gate driver must control the current slope through the parasitic inductances.

III. TWO SLOPE GATE DRIVER

The main propose of this two slope gate-driver is to reduce time intervals one and two (Fig.2), and to expand time interval three. Fig.3 shows the simple two slope gate-driver circuit (*GDRVp*) for M_p. It also shows a block (*LS* path) representing the M_n MOS switch and the respective conventional gate-driver circuit (*GDRVn*, M_n, D_n).

The simple two slope circuit is composed by the three sections marked in Fig. 3. Section one and two are identical to the conventional gate-driver circuit, with a tapering buffer chain. Section three, the last driver stage, charges or discharges the M_p parasitic gate capacitors with two different current strengths.

The two slope driver uses a resistor (R_U) in series with the pull-up path that turns off M_p in order to retard time frame three. This resistor is bypassed by an additional *p*MOS, M_{p2}, which allows the reduction of time frames one and two. Since, for the intended operation, M_{p2} must be on when M_p is on (shrinking time frame one and two) and it must be off when M_p is sifting to off (delaying time frame three), the gate of M_{p2} can be controlled by the same signal as the gate of M_p. Ideally M_{p2} should be completely off when M_p is moving from saturation region to off region (time frame three).

The same approach is illustrated in Fig. 3 (M_{n2} and R_D) for the control of M_p turn-on time.

IV. ENHANCED TWO SLOPE GATE DRIVER

Lower voltage spikes with maximum supply voltage (V_{BAT}) can be obtained using capacitor coupling techniques superimposed to the two slope gate driver circuit. Fig. 4 shows three different useful capacitor couplings. Each of these solutions can be used independently and their effects will be explained separately.

Fig.4 shows the gate-driver of Fig.3 (*GDRVp*), with additional sub-circuits in section three. The added sub-circuits are inside the dashed lines and they only modify the gate-driver behavior during the switching transitions.

A. PGND coupling (C_1)

The sub-circuit inside the two dashed oval lines consists only in two capacitors (C_{1U}, C_{1D}) implemented by MOS transistors, coupling the internal *PGND* supply to nodes *A* and *B*.

This sub-circuit works as follows: During a Low to High (L-H) transition at node *gp* (M_p gate) the source-drain current through M_p starts to fall, and the supply pads parasitic inductances (L_p) produce an overshoot in v_{IN} and an undershoot in *PGND*. This voltage decrease is coupled to node *A* through C_{1U} capacitor, reducing M_{p1} overdrive and therefore reducing the driver strength and smoothing the current variation in M_p.

B. gp delay coupling (C_2)

An alternative way to reduce voltage spikes using capacitive coupling is implemented adding inverters I_{X2}, I_{X3} and the capacitor C_2 (Fig.4).

When the node *gp* is at low state, the M_p switch is closed, the output of I_{X3} inverter is at high state and C_2 capacitor is charged. The M_p switch opening process begins by raising the *gp* node voltage from zero toward v_{IN}. The *gp* node voltage increases by charging-discharging all parasitic capacitors connected to it, and also by discharging C_2 capacitor.

After a rising edge of node *gp* (with a delay defined by I_{X2} and I_{X3} propagation delays), the output of I_{X3} perform a fast H-L transition, slowing down the voltage increase at *gp* node. Ideally, this transition occurs when M_p source-to-gate voltage

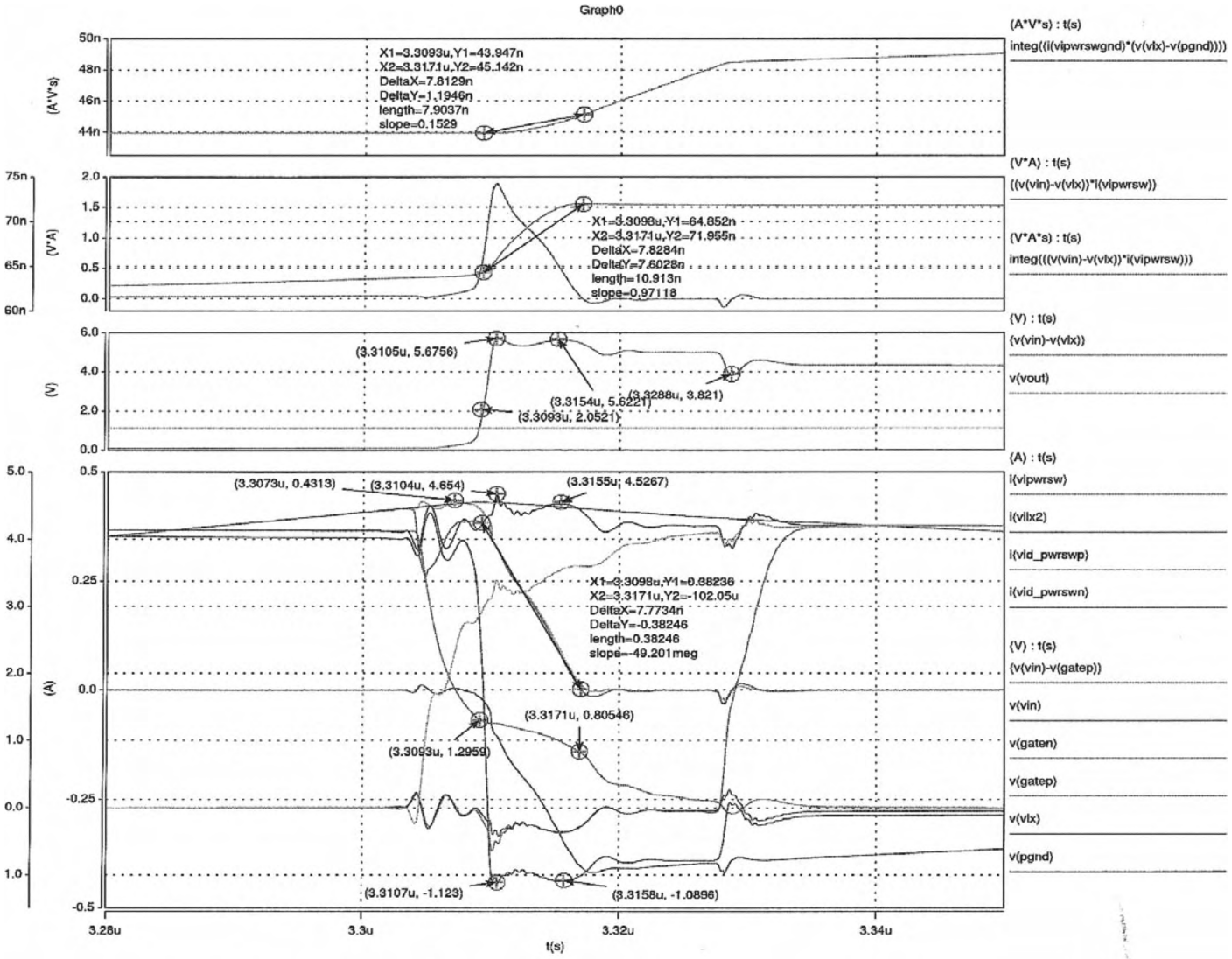

Fig. 5. Enhanced two slope gate driver signals waveforms (*gp* delay coupling).

is decreasing from Miller plateau level to the threshold level (Fig.2), reducing M_p high current slope and therefore the undesired voltage spikes.

The same sub-circuit produces a coupling scheme during the M_p turn-on process. In this case the *gp* voltage decreasing rate is slowed down when the output of I_{X3} inverter performs an L-H transition.

The coupling strength introduced by C_2 can be different at the M_p turn-on and off. This difference can be achieved by designing the inverter I_{X3} H-L transition time different from the L-H transition time.

Fig.5 shows the simulation waveforms when I_{X3} inverter outputs a faster H-L transition. Other sub-circuits in dashed boxes of Fig. 4 were dismissed for this gate-driver simulation. The maximum supply voltage spike when turning off 400mA is 0.5V (V_{BAT} = 4.2V), and the turn-off time for M_p switch is 8ns. The maximum M_p source-drain voltage is $|v_{SDp}|_{max} \approx 5.7$V.

C. *LX feedback coupling (C_3)*

Alternatively, the reduction of supply voltage spikes by capacitive coupling can be achieved by adding the inverters I_{Y1} and I_{Y2} and capacitor C_3 (Fig.4). The inverter I_{Y1} input is node *LX* (Fig.1).

The sensing in this coupling scheme takes advantage of the fact that a fast current decrease on M_p switch is automatically compensated by a symmetrical current increase on the low side path in order to maintain the external current (i_L). Fig.2 waveforms show that the *LX* node voltage decreases quickly from v_{IN} to a negative value as soon as the M_p drain current begins to decrease. This H-L voltage variation at *LX* node propagates through I_{Y1} and I_{Y2} and is applied to C_3. A fast H-L transition at I_{Y2} output slows down the increase rate at *gp* node. Similarly to the *gp* delay coupling described before, the *LX* feedback coupling scheme also works during the M_p turn-on process.

The similarity of *LX* feedback coupling and *gp* delay coupling schemes is obvious. However, the *LX* feedback coupling scheme, as described, can lead to circuit instability. When both power switches are off, the voltage in node *LX* has two components: 1) an average DC value of v_{out} and 2) a sinusoidal oscillation with decaying amplitude. The second component is the underdamped response of the external inductor in series with the high resistance of the open switches

($R_{DS(off)}$) and the parasitic capacitors in node *LX*. The oscillation at I_{Y2} output, propagated through C_3 to M_p and to the *LX* node, introduces positive feedback that can maintain the oscillation.

V. RESULTS

Table-I shows measurements from the conventional slow and fast gate-drivers and also from the two slope gate-driver circuit with three different alternatives: simple; with *PGND* coupling and with *gp* delay coupling. $|\Delta v|_{\max}$ is the maximum supply spike magnitude in *PGND* node or on the v_{IN} node. $|v_{SDp}|_{\max}$ is the maximum source-to-drain voltage at M_p. t_{off} is the M_p cut-off time as previously defined. t_{SNS0} is the delay time from when M_p gate voltage starts to rise until $i_p = 0$. rate1 is the ratio of two areas, $(W\!L)_{GDRVp}$ and $(W\!L)_{Mp}$; where $(W\!L)_{Mp}$ is the M_p transistor width multiplied to its length and $(W\!L)_{GDRVp}$ is the sum of all transistors areas (excluding MOS capacitors and I_{Yn} and I_{Xn} inverters) in the gate-driver circuit. rate2 is the ratio of two areas, $(W\!L)_{MOSCap}$ and $(W\!L)_{Mp}$; where $(W\!L)_{MOSCap}$ is the sum of capacitors (C_{u1} or C_2) and inverters areas (I_{Xn} for C_2). W_{SWPL} is the M_p turn-off energy loss. This energy loss results from time integration of the product $|v_{SDp}|.|i_p|$ during the M_p turn-off (t_{off}) time. W_{DnL} is the energy loss of the low side transistor body diode (D_n) during M_p turn-off time interval. This energy loss is a slice of the total body diode loss, since the integration interval excludes the non-overlap switching dead-time.

Table-I shows that a significant reduction on the maximum supply voltage spike can be achieved at the expense of gate-driver silicon area. The enhanced two slope gate-driver circuit with *gp* delay coupling presents low voltage spikes ($|\Delta v|_{\max}$) as the conventional slow gate-driver and a M_p turn-off time (t_{off}) identical to the conventional fast gate-driver. The superior performance of the two slope enhanced gate-driver costs a significant silicon area overhead when compared to the conventional gate-driver. Although the area overhead, the enhanced two slope gate-driver circuits is a suitable solution when a low voltage CMOS technology is used to design high switching frequency, high current, DC-DC step-down converters.

Table-1. Gate-driver circuit performance measured parameters (V_{BAT} = 4.2V, v_{out} =1.2V, $(I_L)_{max}$ = 0.4A).

GDRV type →	conventional		two slope		
parameter [unit] ↓	slow	fast	simple	PGND coupling	*gp* coupling
$\|\Delta v\|_{MAX}$ [V]	0.5	0.7	1.0	0.7	0.5
$\|V_{DSp}\|_{MAX}$ [V]	5.7	6.3	6.9	6.3	5.7
t_{off} [ns]	14.8	7.9	3.2	4.4	7.8
T_{SNS0} [ns]	60	40	9	10	16
W_{SWPL} [nJ]	14.8	8.8	3.8	5.0	7.6
W_{DnL} [nJ]	3.2	1.4	0.4	0.6	1.2
rate1 [%]	0.3	0.4	14	14	14
rate2 [%]	0	0	0	17	23

The gate-driver with *PGND* coupling, for a similar voltage spike value, is able to turn-off M_p much faster and with lower losses. *PGND* coupling is less sensible to battery voltage (V_{BAT}), which can be an advantage over the *gp* delay coupling.

VI. CONCLUSIONS

The design space of a gate-driver circuit for the HS MOS switch was addressed, with the objective to minimize supply voltages spikes due to the parasitic bonding wire and package pins inductances.

An original gate-driver circuit topology labeled two-slope gate-driver was proposed with three capacitor coupling optimizations. The proposed gate drives, for similar supply voltage spikes, presents faster turn-off times and significantly lower losses. Although the proposed drivers exhibit higher area overhead than conventional drivers, their use can be a suitable solution when low voltage CMOS technologies are used to design high current, high frequency, DC-DC converters.

LX capacitive coupling is the solution less sensitive to the operating conditions (V_{BAT}, v_{out}) but can lead to an unstable behavior. This solution will be addressed in future works.

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