# A Fault Tolerant Model Predictive Control with Self-Adaption for the Three-phase T-Type Inverter

Joaquim Monteiro
UnIRE, ISEL, Polytechnic University of Lisbon,
Lisboa, Portugal
INESC-ID Lisboa, Portugal
joaquim.monteiro@isel.pt

J. Fernando Silva
DEEC, IST, Universidade de Lisboa,
Lisboa, Portugal
INESC-ID Lisboa, Portugal
fernando.alves@tecnico.ulisboa.pt

Sónia Pinto
DEEC, IST, Universidade de Lisboa,
Lisboa, Portugal
INESC-ID Lisboa, Portugal
soniafp@tecnico.ulisboa.pt

V. Fernão Pires
ESTSetúbal, Instituto Politécnico Setúbal,
Setúbal, Portugal
INESC-ID Lisboa, Portugal
vitor.pires@estsetubal.ips.pt

2025 14th International Conference on Renewable Energy Research and Applications (ICRERA) | 979-8-3315-9989-8/25/$31.00 ©2025 IEEE | DOI: 10.1109/ICRERA66237.2025.11283941

***Abstract*— Multilevel inverters with three-level T-Type topology are widely recognized as a highly recommended solution for applications that require reliability and fault tolerance. However, achieving a fault tolerant operation system typically requires the implementation of fault detection algorithms along with modulator or control system. This paper proposes a different approach by introducing a self-adaptive control system designed to ensure fault-tolerant operation under open-switch fault conditions. The proposed control system is based on Model Predictive Control (MPC). The proposed controller intrinsically detects deviations from the desired setpoint and automatically cancels the usage of the faulty voltage vectors. Furthermore, the proposed control ensures capacitor voltage balancing, even under fault-tolerant conditions. The effectiveness of the proposed fault-tolerant MPC method is demonstrated through several simulation tests. The results obtained confirm the validity and feasibility of the proposed approach.**

***Keywords*— Fault-tolerant, model predictive control, Self-Adaptation, T-type converter***

## I. INTRODUCTION

Multilevel inverters have been extensively used in worldwide industrial applications due to their excellent features, high efficiency, low cost, and relative ease of implementation and operation. Thanks to these properties, the multilevel inverter has been applied in renewable energy systems (RES), flexible AC transmission systems (FACTS), high voltage direct current (HVDC) electrical drives, battery energy storage systems (BESSs) [1, 2]. In many of these applications it is extremely important to have high reliability and fault-tolerant power converters. These features are becoming increasingly important for user safety, the prevention of environmental damages, and possible economic losses [3-5]. In this context, the T-type multilevel inverter topology has the advantage in terms of the efficiency for medium switching frequency, when compared with neutral-point-clamped (NPC), or the cascaded H-bridge, or the flying capacitors (FC) topology [6] or even other new structures [7, 8]. Moreover, T-type multilevel inverters are widely used in low distortion, low-voltage applications, particularly where efficiency and cost are critical factors [9, 10]. In addition, Unlike NPC converters, T-type converters do not require clamping diodes, which contributes to the reduction of the overall component count [11]. In addition, this inverter topology takes advantage of lower conduction and switching losses, as well as reduced switching voltage stress [12].

One of the most common faults in the power devices of the T-Type multilevel inverter, as well as in power converters in general, is the open-circuit fault [13, 14]. This type of failure may result from lifted or cracked bonding wires in the power device modules due to thermal cycling, or from failure of the gate-drive. To address this issue, several approaches have been proposed to enhance the fault-tolerant capability of inverters [15, 16]. In [15] a converter topology for a switched reluctance machine (SRM) is proposed, providing fault tolerant capabilities to the drive under a switch fault. In [16], the fault-tolerant algorithms such as one-phase two-level switching tolerance control and three-level switching-oriented tolerance control are implemented by redefining the phase turn-on times and rearranging the switching sequences. In general, two main strategies can be adopted to achieve fault-tolerant operation: (i) increasing hardware redundancy by integrating additional power semiconductor devices or (ii) modifying the modulation and control strategies [17]. Several inverter topologies have also been developed to achieve fault-tolerant operation, primarily through modifications to the power circuit [18].

This paper presents a novel fault-tolerant control strategy based on a self-adaptive Model Predictive Control (MPC) specifically developed to guarantee reliable operation of power converters under open-switch fault conditions. The MPC technique is characterized by fast dynamic response, conceptual simplicity, and the ability to incorporate nonlinearities and constraints [19, 20]. It has been applied in several industrial systems, including energy conversion systems, HVDC systems, RES applications and many other power electronic applications [21, 22]. Unlike conventional fault-tolerant strategies, the proposed method eliminates the need for external fault detection mechanisms by inherently identifying deviations from the

desired reference during system operation. In the proposed strategy, when an open-circuit fault occurs in one inverter power switch, the fault is detected by comparing the applied vector voltages to the ideal voltages of the tracking vector chosen by the MPC. Once the fault is identified, the fault-tolerant control algorithm reconfigures the inverter switching states, within the MPC algorithm, to maintain the inverter operation under fault conditions. After a deviation is detected, the control system excludes the voltage vectors responsible for the abnormal condition, thus preserving overall system performance. In addition, the proposed control strategy incorporates mechanisms to ensure capacitor voltage balancing, even in the presence of faults. The performance of the proposed method is verified through several simulation tests, leading to the confirmation of fault tolerant capability.

## II. Topology of the T-Type Three-Level Converter

The proposed topology, based on a three-phase T-type converter, is shown in Fig. 1. The converter is supplied by a DC voltage source with a midpoint connection formed by capacitors $C_1$ and $C_2$. This midpoint is connected to a T-type three-level voltage source inverter. The topology includes six unidirectional semiconductor switches and three bidirectional switches connected at the midpoint.

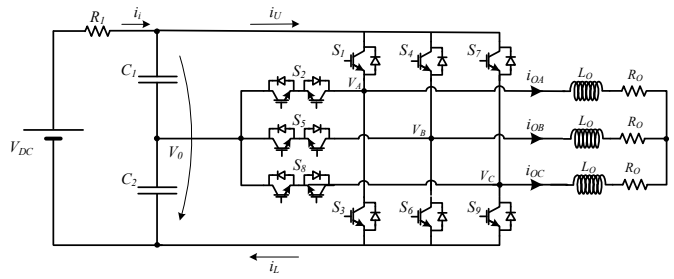



Fig. 1. Power circuit of three-phase T-type converter.

To control the T-type converter both in normal and fault tolerant modes a self-adaptative fault-tolerant model predictive control (MPC) strategy is proposed. The development of this controller requires a dynamic model of the inverter to determine the position of the AC voltage space-vectors, thereby ensuring that the AC currents track their references. Moreover, the voltage vector selected by the MPC must maintain the voltage balance capacitors $V_{C1}$ and $V_{C2}$. These voltage vectors are functions of the switches of each leg, represented by the discrete three-level variable $S_i$ (1).

To obtain the converter model, the switches are assumed to be ideal. They are represented by discrete, nonlinear switching functions that can take one of three possible values, depending on the state $S_i$. The corresponding output voltages assume three discrete levels. Accordingly, they are expressed in terms of the switching functions $H_j$, defined in (1) with $j \in \{A, B, C\}$ and $i \in \{1,4,7\}$. From (1), the output AC voltages are obtained as in (2), where $V_A$, $V_B$ and $V_C$ represent the voltages from phases $A, B, C$ to the $V_{DC}$ negative terminal.

$$H_j = \begin{cases} 1 & if\ S_i\ is\ On \wedge S_{i+1}\ is\ \text{Off} \wedge S_{i+2}\ is\ \text{Off} \\ 0.5 & if\ S_i\ is\ Off \wedge S_{i+1}\ is\ \text{On} \wedge S_{i+2}\ is\ \text{Off} \\ 0 & (if\ S_i\ is\ Off \wedge S_{i+1}\ is\ \text{Off} \wedge S_{i+2}\ is\ \text{On}) \vee \\ & (if\ S_{1,2,3}\ is\ On \wedge S_{4,5,6}\ is\ \text{On} \wedge S_{7,8,9}\ is\ \text{On}) \end{cases} \quad (1)$$

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = V_0 \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} H_A \\ H_B \\ H_C \end{bmatrix} \quad (2)$$

In order to derive the voltage vector diagram the Clarke–Concordia transformation is applied to (2). Accordingly, in $\alpha\beta$ coordinate plane, 27 voltage space vectors are obtained, Fig. 2.

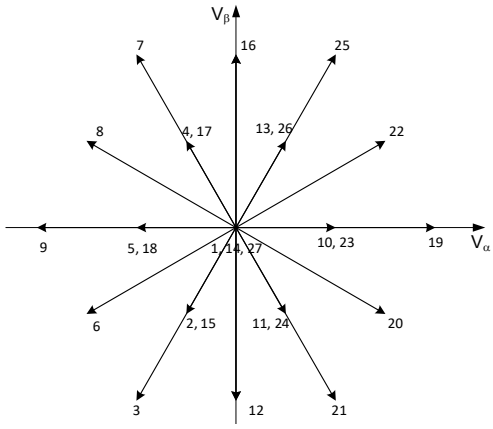



Fig. 2. Voltage vectors in the plane of the AB coordinates

By analyzing AC side of the power converter as a function of the switching states, the following equation is obtained:

$$\begin{bmatrix} \frac{di_{OA}}{dt} \\ \frac{di_{OB}}{dt} \\ \frac{di_{OC}}{dt} \end{bmatrix} = \frac{R_O}{L_O} \begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} i_{OA} \\ i_{OB} \\ i_{OB} \end{bmatrix} + \frac{V_O}{3L_O} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} H_A \\ H_B \\ H_C \end{bmatrix} \quad (3)$$

Transforming the previous equation from the $A$, $B$, $C$ frame to the $\alpha\beta$ frame equation (4) is obtained:

$$\begin{bmatrix} \frac{di_\alpha}{dt} \\ \frac{di_\beta}{dt} \end{bmatrix} = \frac{R_O}{L_O} \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + \frac{V_O}{L_O} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} H_\alpha \\ H_\beta \end{bmatrix} + \frac{1}{L_O} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (4)$$

This equation shows the AC currents as functions of the inverter applied AC voltages in the $\alpha\beta$ plane. These voltages

depend on the switching states. Although this converter provides 27 available vectors, only 19 of them have distinct load voltages. However, the eight load redundant vectors play an important role in balancing the voltages across capacitors $C_1$ and $C_2$.

## III. Proposed Fault-Tolerant Control Strategy

The proposed MPC algorithm controls the T-type converter under both normal and fault-tolerant operating modes. The algorithm controls the state variables through real-time optimization within a receding constrained prediction horizon. To guarantee safe operation during fault conditions, the primary control loop integrates fault diagnosis with fault-tolerance techniques, executed in parallel. The following sections describe the proposed control strategy in both normal and fault-tolerant modes.

### A. MPC in Normal Operation Mode

The proposed control algorithm (Fig.3) selects the most suitable voltage vector configuration from a set of 27 possible switching states, such that the error between the reference current and the predicted current is minimized. This selection process considers not only the instantaneous system dynamics but also the voltage balancing of the DC-link capacitors and the presence of potential faults within the available switching vectors.

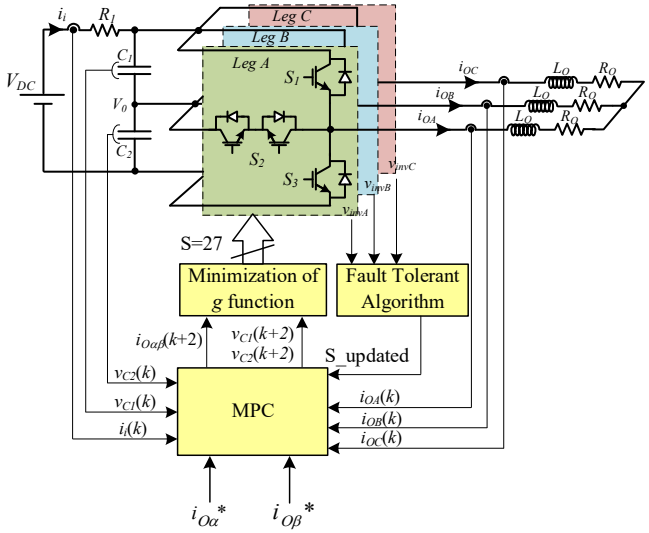



Fig. 3. Block diagram of a Fault-Tolerant Control Strategy

In the MPC strategy, the instantaneous values of the AC load currents, capacitor voltages, and input inductor currents are measured at time $t(k)$. Based on these measurements, the AC load currents and capacitor voltages are predicted for the next sampling time $t(k+1)$ for all available vectors. The optimal voltage vector is then selected by minimizing a cost function, which determines the switching state that ensures the minimum error cost between the references and the predicted values. From these values, and to compensate for the computational delay in control evaluation, the controller predicts the behavior of the AC grid currents and the voltages of the two DC capacitors at time $t(k+2)$, as explained below.

To implement MPC, a dynamic model of the inverter and load system is required (5).

$$\frac{di_{Oj}(t)}{dt} = \frac{-R_O i_{Oj}(t) + v(t)}{L_O} \tag{5}$$

where $L_O$ and $R_O$ represent the load inductance and resistance, respectively; $v$ is the voltage vector generated by the inverter; $i_{Oj}$ is the load current vector.

Using the Euler forward approximation method, the discretization of the output current derivative is given by:

$$\frac{di_{Oj}(t)}{dt} = \frac{i_{Oj}(k+1) - i_{Oj}(k)}{T_s} \tag{6}$$

where $T_s$ is the sampling period.

According to the above considerations, the AC load currents at time $t_{k+1}$ can be predicted using (7).

$$i_{Oj}(k+1) = \left(1 - \frac{R_O}{L_O}T_s\right) i_{Oj}(k) + \frac{T_s}{L_O} v(k) \tag{7}$$

where $i_{Oj}(k)$ is the measured AC currents, and $i_{Oj}(k+1)$ the AC currents predicted for the next sampling interval.

The discrete-time equations for the voltages across capacitors $C_1$ and $C_2$ are derived as given in (8) and (9).

$$v_{C1}(k+1) = v_{C1}(k) + \frac{1}{C_1} i_{C1}(k) T_s \tag{8}$$

$$v_{C2}(k+1) = v_{C2}(k) + \frac{1}{C_2} i_{C2}(k) T_s \tag{9}$$

The values of the capacitor currents depend on the switching states of the T-type inverter and on the AC output currents, as expressed in (10) and (11).

$$i_{C1}(k) = i_i(k) - S_{1A} i_{OA} - S_{1B} i_{OB} - S_{1C} i_{OC} \tag{10}$$

$$i_{C2}(k) = i_i(k) + S_{1A} i_{OA} + S_{1B} i_{OB} + S_{1C} i_{OC} \tag{11}$$

where $i_i(k)$ is the inductor current of $L_1$ and $S_{1A}$, $S_{1B}$, $S_{1C}$ express the switching states.

The computational time required for evaluating the control algorithm is addressed using delay compensation techniques, such that the future current at the instant t(k+2) is employed in the predictive control method. The future AC input current is obtained by time-shifting the model (7) one step forward, as:

$$i_{Oj}(k+2) = \left(1 - \frac{R_O}{L_O}T_s\right) i_{Oj}(k+1) + \frac{T_s}{L_O} v(k+1) \tag{12}$$

Applying the same reasoning delay compensation technique, to the expressions (8) and (9), the capacitor voltage at $(k+2)$ value is obtained as follows:

$$v_{C1}(k+2) = v_{C1}(k+1) + \frac{1}{C_1} i_{C1}(k+1) T_s \tag{13}$$

$$v_{C2}(k+2) = v_{C2}(k+1) + \frac{1}{C_2} i_{C2}(k+1) T_s \tag{14}$$

The MPC minimizes the AC load current errors, the capacitors voltage imbalance, by employing an appropriate cost

function for all tracking errors. Accordingly, the proposed MPC cost functional ($g$) consists of two weighted terms: one associated with the output currents, and other with the capacitor voltage imbalance (15).

$$g = g_i \delta_i + g_{vc} \delta_{vc} \tag{15}$$

where $g_i$ and $g_{vc}$ are the cost functions of the output currents and capacitor voltage imbalance, respectively. The weighting factors $\delta_i$ and $\delta_{vc}$ are introduced to provide a suitable numerical representation of these quantities in the control microprocessor.

The cost function for the AC load currents is defined as:

$$g_i = |i_{O\alpha}(k+2)^* - i_{O\alpha}(k+2)| + \left|i_{O\beta}(k+2)^* - i_{O\beta}(k+2)\right| \tag{16}$$

where $i_{O\alpha}(k+2)^*$ and $i_{O\beta}(k+2)^*$ represent the reference AC load currents in the $\alpha$ and $\beta$ axes, respectively, and $i_{O\alpha}(k+2)$ and $i_{O\beta}(k+2)$, the corresponding predicted AC load currents.

Similarly, the cost function of the capacitor voltages imbalance is defined as:

$$g_{vc} = |v_{c1}(k+2) - v_{c2}(k+2)| \tag{17}$$

where $v_{c1}(k+2)$ and $v_{c2}(k+2)$ are the predicted voltages of the $C_1$ and $C_2$, capacitors.

### *B. Faul-tolerant Operation Mode*

A fault detection strategy is integrated into the MPC algorithm to ensure operational reliability. As illustrated in the flowchart presented in Fig. 4, the voltage vector measured at the inverter is compared with the optimal reference vector to be applied. Voltage vectors that exhibit inconsistencies, such as conflicting signs relative to physically meaningful quantities like the orthogonal voltage components $v_{\alpha v}$ and $v_{\beta v}$ are classified as faulty. Once identified, these faulty vectors are excluded from the optimization process in subsequent control cycles to prevent their selection.

In order to increase the robustness of the detection scheme and mitigate false fault indications arising from noise or transient events, a fault persistence criterion is adopted. A fault condition is only confirmed when the inconsistency is detected consistently over a predefined number of consecutive control cycles. This approach enhances the system's fault tolerance while maintaining reliable and stable converter operation under varying grid and load conditions.

A fault in any power semiconductor reduces the number of available voltage vectors, as certain switching combinations become invalid. The impact on converter performance depends on which semiconductor is affected. For the first leg ($A$), two fault scenarios can be considered. If the fault occurs in either the upper or lower device ($S_1$ or $S_3$), several high-amplitude voltage vectors are compromised. Fig. 5 (a) and Fig. 5 (b) illustrate the corresponding AC voltage vectors in the $\alpha\beta$ plane under these fault conditions. In both cases only 19 out of the 27 voltage vectors remain available. Specifically, in the case of $S_1$ failure, only vectors up to 19 are available, whereas an $S_3$ failure renders the first 9 vectors unavailable.

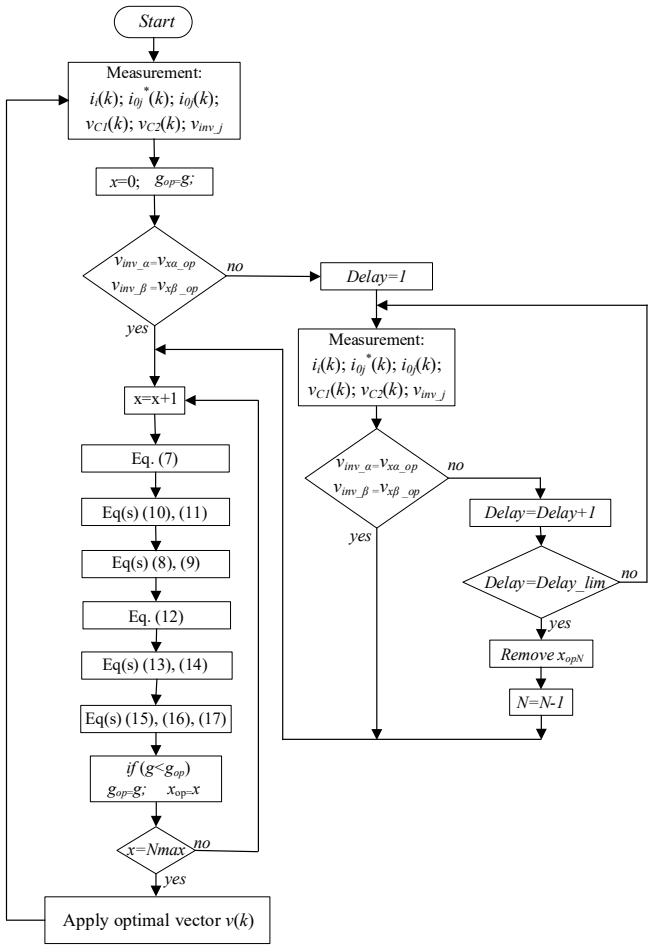



Fig. 4. Flow chart of the Fault Tolerant MPC with Self-Adaption.

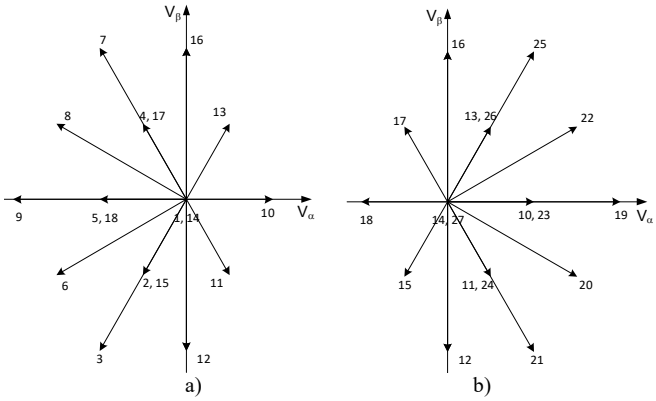



Fig. 5. AC voltage vectors in the αβ plane under fault conditions. a) For switch $S_1$; For switch $S_3$.

## IV. Simulation Results

To evaluate the performance of the proposed control system, designed to ensure fault-tolerant operation under open-switch fault conditions in the three-phase T-Type converter using the adopted optimal predictive control, several simulation tests were carried out using detailed models, implemented in MATLAB/ Simulink and the SimPowerSystems library. The parameters used in this control system are: $V_{DC}$= 400 V, $C_1 = C_2$ = 1000 µF, the load resistor and inductor per phase 30 Ω and 10 mH,

respectively. To demonstrate the dynamic behavior of the proposed control system, Fig. 6 a) and b) presents the load currents and the load voltage of phase *A* respectively, without the fault tolerant algorithm, when $S_3$ is in faulty. At the beginning, the current load reference is set to 5 A. Then, at t = 0.1 s, the gate signal of the lower switch in the first leg ($S_3$) is disabled, introducing an open-switch fault. Afterwards, at t = 0.2 s, the current reference is reduced to half of its initial value. As can see from the simulation results, the system without fault-tolerant control neither detects nor compensates for the fault.

Fig. 7 a), b) and c) successively shows the waveforms of the load current, the load voltage, and capacitor voltages under the same conditions when the proposed fault-tolerant algorithm is enabled. The results confirm that the open-circuit fault is correctly detected by the fault-tolerant detection algorithm, and the system maintains the operation through the fault-tolerant control strategy. It is also visible in the load currents waveforms that, when the current reference is reduced by half of its initial value, the load currents maintain near perfect tracking, contrary to the Fig. 6 simulations without fault tolerant algorithm.

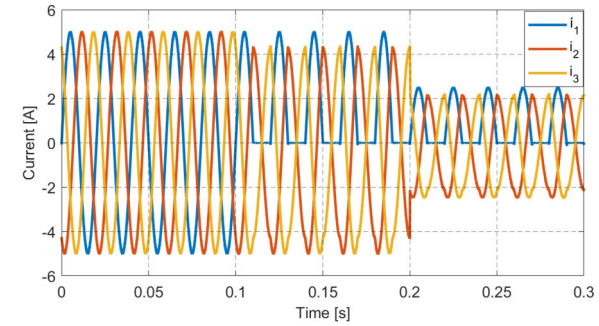
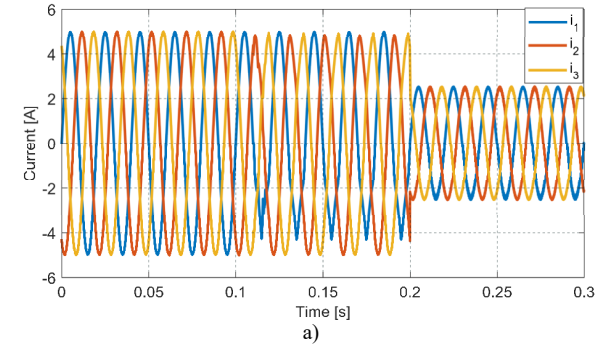



Fig. 6. Simulation results without Fault Tolerant Algorithm. a) Load currents. b) Load voltage in phase A.



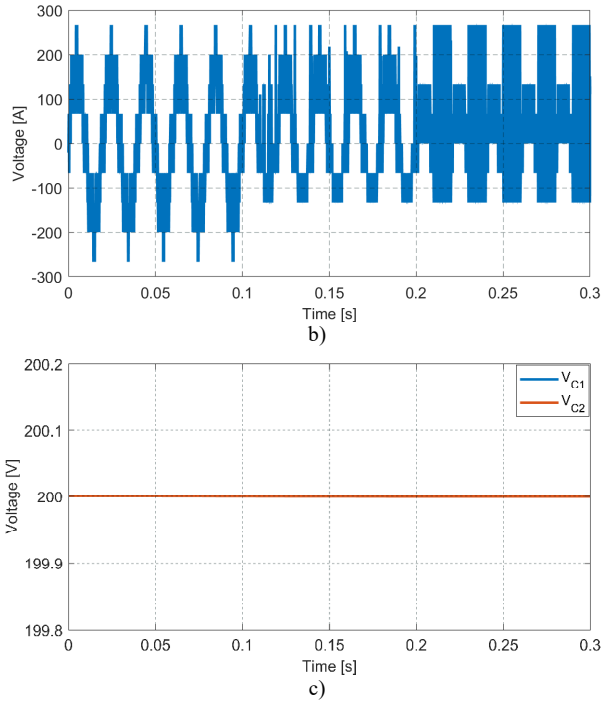
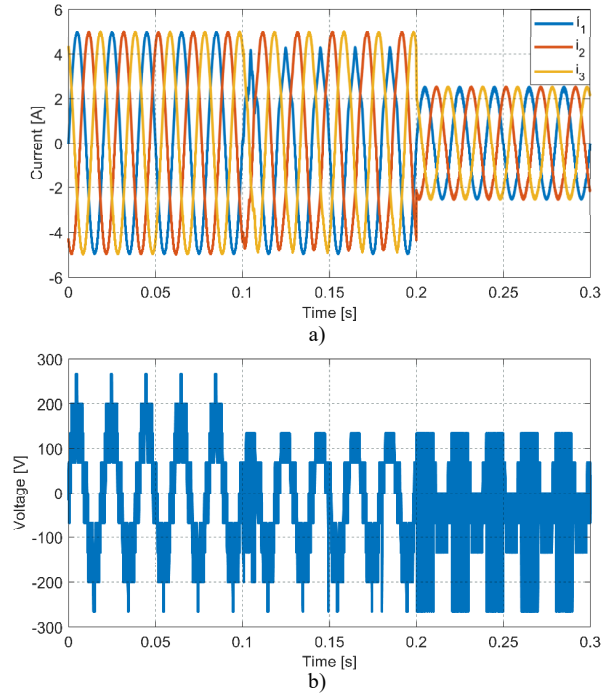
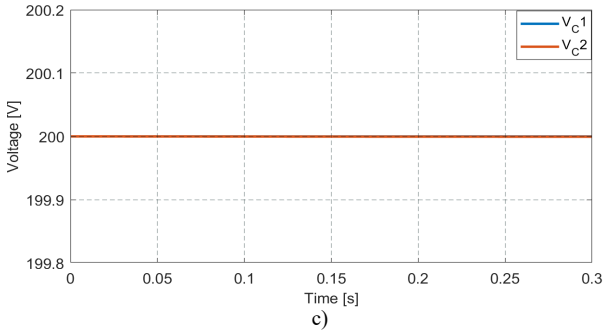




Fig. 7. Simulation results with fault tolerant algorithm on the switch $S_3$ a) Load currents. b) Load voltage in phase A. c) Capacitors $C_1$ and $C_2$ voltages.

To further evaluate the performance of the proposed fault-tolerant algorithm, additional tests were conducted. In Fig. 8, a fault in switch $S_1$ is considered. For a load current reference of 5 A, at t=0.1 t = 0.1 s, the gate signal of the upper switch in the first leg ($S_1$) is disabled to create an open-switch fault. Then, at t=0.2s, the current reference is reduced to half of its initial value. From these results it is possible to confirm that, the fault-tolerant detection algorithm also detects this open-circuit fault in another power switch. The converter maintains operation at near prefect tracking through the fault-tolerant control strategy.






c)

Fig. 8. Simulation results with fault tolerant algorithm on the switch $S_1$ a) Load currents. b) Load voltages. c) Capacitors $C_1$ and $C_2$voltages.

Based on these results, it is confirmed that the proposed fault-tolerant detection algorithm correctly identifies open-circuit faults in distinct power switches. Additionally, the control system then maintains near correct operation through the fault-tolerant control strategy.

## V. Conclusion

This paper presents a fault-tolerant MPC strategy with a self-adaption algorithm for the T-Type converters. The proposed fault-tolerant method identifies the voltage vectors that exhibit inconsistencies, such as conflicting signs when compared to physically meaningful quantities like the orthogonal voltage components $v_{\alpha v}$ and $v_{\beta v}$ and classifies them as faulty. The fault-tolerant control algorithm then reconfigures the converter switching states, which is part of the MPC routine, to ensure a correct operation of the converter under fault conditions. In fault-tolerant operation, the proposed controller must adapt its control action according to the specific power semiconductor device failure, in order to compensate for the resulting reduction in the available voltage vectors. The balancing of the capacitor voltages was ensured under both normal operation and fault-tolerant conditions. The effectiveness of the proposed self-adaptive control strategy was validated through simulation experiments. Results under both normal and faulty conditions confirmed the expected performance and validated the fault tolerance capability of the proposed method.

## Acknowledgment

This work was supported by UnIRE, ISEL – Polytechnic University of Lisboa and by national funds through Fundação para a Ciência e a Tecnologia, I.P. (FCT) under projects UID/50021/2025 and UID/PRR/50021/2025.

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