



ISEL

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Non-Intrusive ECG Acquisition Test-bed

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“If I have seen further than others, it is by standing upon the shoulders of giants.”

- Isaac Newton

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Abstract

Nowadays there is a variety of **ElectroCardioGraphy (ECG)** test equipment which can be used to assess the functionality of electrocardiographs. Current systems are intended for use in clinical or hospital environment, being highly accurate and more oriented to the generation of ECG tracings of arrhythmias, noise being fed from the power supplies, as well as deviations caused by breathing and muscular activity.

There is a growing demand for devices that can capture the ECG waveform during daily routines, applications include fitness tracking, computer gaming, providing alerts to drowsy drivers or just non-intrusive health monitoring. As these devices become more popular, there is also the need to develop test equipment that can replicate such scenarios of operation.

The system proposed in this project was developed for testing ECG devices for daily life use, in portable equipment and in less ideal environments, where there is more noise and interference, and in which the use of wet electrodes is impractical. In this project, a closed-loop test circuit is designed, allowing the testing of ECG platforms still in the development phase, which may be incorporated into devices used in everyday life.

The developed circuit allows testing of these platforms using user-defined ECG waveforms, as well as performing differential mode and common-mode noise analysis, simulating ECG signal amplitude variations, variations in skin-electrode impedance, motion artifacts and lead-off events. The circuit developed in this project allows for the recording of the test result coming from the device under test for further processing.

This project provides a novel application for a recently developed technique of impedance synthesis, based on transconductance amplifiers. Here the technique is applied to simulate the variations of the skin-electrode impedance.

Keywords: Electrocardiography (ECG), Biopotential Acquisition, Skin-Electrode Impedance, Biomedical Test Equipment, Mobile Biomedical Device, Variable Capacitance, Voltage Controlled Capacitance, Voltage Controlled Impedance, Lead-Off Detection, Closed-Loop ECG Test, ECG Noise Analysis, ECG Front-End

Resumo

Na atualidade, existe uma grande variedade de equipamentos de teste para EletroCardioGrafia (ECG). Estes sistemas são utilizados em ambiente clínico ou hospitalar, sendo equipamentos com uma precisão elevada e mais orientados à geração de traçados ECG de arritmias, interferência causada pelas redes de alimentação, bem como desvios causados pela respiração e atividade muscular.

Existe uma procura crescente de dispositivos de aquisição de ECG para utilizar durante as rotinas diárias, as aplicações incluem monitorização durante o exercício físico, jogos de computador, geração de alerta de fadiga para condutores, ou apenas para monitorização do estado de saúde de forma não intrusiva. À medida que estes dispositivos se tornam mais populares, existe a necessidade de desenvolver equipamento de teste que consiga replicar os cenários de utilização.

O sistema desenvolvido neste projeto é utilizado no teste de equipamentos ECG que podem ser utilizados diariamente, em dispositivos portáteis e em ambientes menos ideais, com ruído acentuado e interferência, e nos quais a utilização de elétrodos húmidos é impraticável.

O circuito desenvolvido permite testar essas plataformas utilizando ondas de ECG definidas pelo utilizador, bem como realizar a análise de ruído de modo comum e de modo diferencial, de simular variações de amplitude do sinal de ECG, variações na impedância pele-eléctrodo, artefactos de movimento e eventos de *lead-off*. O ficheiro de teste é totalmente configurável, permitindo ao operador do dispositivo a realização de uma grande variedade de testes. O sistema desenvolvido neste projeto permite a gravação do resultado do teste, permitindo a posterior realização de um conjunto mais extenso de análises.

Este projeto apresenta uma nova aplicação para uma técnica recentemente desenvolvida de sintetizar impedâncias, baseada em amplificadores de transcondutância, que neste caso é aplicada para simular as variações da impedância pele-eléctrodo.

Palavras-Chave: Eletrocardiografia (ECG), Aquisição de Biopotenciais, Impedância Pele-Eléctrodo, Equipamento de Teste Biomédico, Capacidade Variável, Capacidade Controlada por Tensão, Impedância Controlada por Tensão, Detecção de *Lead-off*, Análise de ruído em Equipamentos ECG, *Front-end* de ECG

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Resumo Alargado

No presente projeto um sistema de teste de *ECG Front End* é desenvolvido. Existe uma grande variedade de equipamentos de teste disponíveis na atualidade, cuja funcionalidade é testar equipamentos de ECG (eletrocardiograma) em ambiente clínico e hospitalar. Estes equipamentos apresentam um conjunto de funcionalidades, tais como, por exemplo:

- Geração de traçado ECG normal
- Geração de formas de onda de *pacemaker*
- Elevação do segmento ST
- Geração de arritmias
- Testes de rejeição de interferência da rede de alimentação elétrica (50 ou 60 Hz)
- Testes de deteção do complexo QRS
- Testes de rejeição da onda T
- Geração de artefactos de ECG (respiração, *baseline wander*, EMG)
- Geração de sinais de teste (onda sinusoidal, onda quadrada, onda triangular, pulso retangular e pulso triangular)

Os testes realizados por estes equipamentos permitem verificar a rejeição de artefactos e de interferência, bem como testar os algoritmos de cálculo de ritmo cardíaco e de deteção de arritmias, por forma a verificar se estes se encontram em conformidade.

O sistema implementado difere destes equipamentos uma vez que foi planeado para testar os circuitos presentes em equipamentos ECG pequenos, leves e portáteis que podem ser utilizados no dia-a-dia. Estes dispositivos, habitualmente, são utilizados em conjunto com eléctrodos secos de diversos tipos, podendo, por exemplo, os eléctrodos ser agarrados ou segurados com as mãos em vez de serem colados ou aplicados no corpo, permitindo uma aquisição de traçado ECG menos “invasiva” e mais confortável.

Uma outra grande diferença que existe entre o sistema desenvolvido e os equipamentos de teste de ECG existentes, prende-se com o facto de este sistema ser capaz de testar circuitos em fase de desenvolvimento.

Por forma a testar circuitos ECG que funcionam em condições menos ideais e mais mutáveis é necessário um sistema com um conjunto de funcionalidades diferentes, tais como:

- Variação de *offset* do sinal em modo comum (para simulação de maus contactos nos eléctrodos)
- Geração de sinal de interferência nas componentes de modo comum e diferencial do sinal ECG (simulação de interferência da rede de alimentação elétrica)
- Simulação de diferentes impedâncias da interface eléctrodo-pele (simulação de diferentes tipos de pele e de eléctrodo)
- Variação ao longo do tempo da impedância eléctrodo-pele (simulação de maus contactos nos eléctrodos, diminuição da impedância devido ao suor)
- Tempo de recuperação de sinal após *lead-off* (simula a situação em que um eléctrodo é temporariamente desligado, voltando posteriormente a ser ligado)

Após a especificação das funcionalidades, um diagrama de blocos simplificado é desenhado, contendo os elementos essenciais para implementação das funcionalidades requeridas. O diagrama de blocos simplificado do sistema encontra-se representado na figura 1.

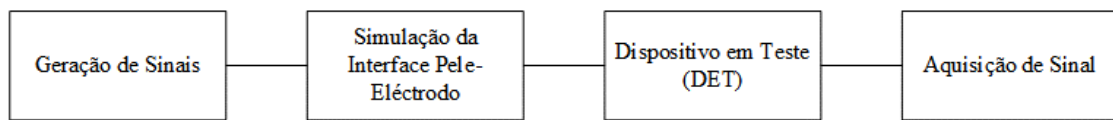


Figura 1: Diagrama de blocos do sistema (simplificado)

O sistema é composto por três blocos principais, um bloco de geração de sinais, um bloco que realiza a simulação da interface pele-eléctrodo e um bloco de aquisição de sinal. Existe ainda na figura um quarto bloco que representa o dispositivo em teste, sem o qual o sistema não pode funcionar. Uma particularidade interessante deste sistema é a presença de um bloco de aquisição de sinal, uma vez que o *ECG front end* é testado, ou seja, o próprio circuito de aquisição ECG, a saída do mesmo pode ser amostrada e gravada em suporte digital para realização de pós-processamento em *software*. Os equipamentos de teste existentes não possuem este bloco, porque destinam-se a testar equipamentos de ECG (ao invés de circuitos de aquisição ECG) que têm monitor ou que gravam os resultados em papel ou em formato digital, pelo que um bloco de aquisição de sinal não é necessário. Outra razão para a inexistência deste bloco, deve-se ao facto dos testes, regra geral, serem realizados no local, não havendo necessidade de uma posterior análise detalhada dos resultados em *software*.

Por forma a melhor compreender a arquitetura do sistema desenvolvido, um diagrama de blocos mais detalhado é apresentado na figura 2.

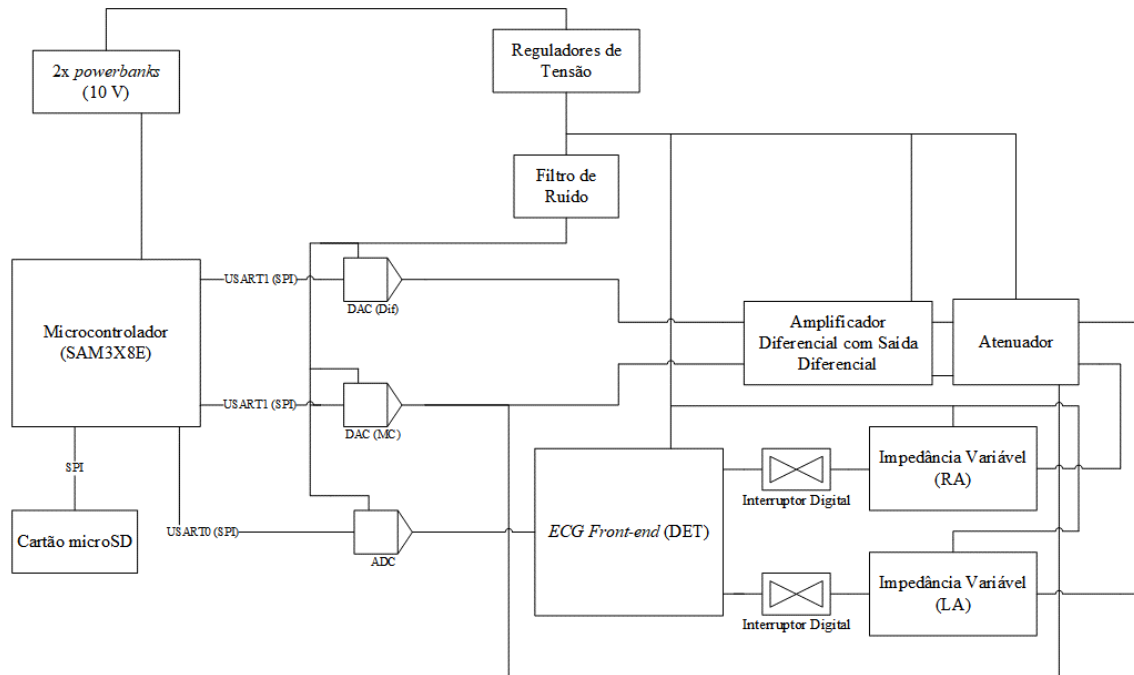


Figura 2: Diagrama de blocos do sistema (completo)

O sistema é composto por catorze blocos, um conjunto de duas *powerbanks* (baterias), reguladores de tensão, microcontrolador, cartão de memória microSD, conversores analógico-digital e digital-analógico, alimentados por uma tensão de alimentação filtrada por um filtro de ruído e interferência, um amplificador diferencial com saída diferencial, um atenuador, dois circuitos de impedância variável (um para simular o eletrodo positivo e outro para simular o eletrodo negativo, este sistema destina-se a testar circuitos *single lead*, em configurações de dois eletrodos) e dois interruptores digitais (um para cada eletrodo). Existe na figura um outro bloco, o *ECG Front-end*, que corresponde ao circuito de ECG testado, este bloco não faz parte do sistema, porém, o sistema não funciona sem o mesmo, este bloco é incluído para dar melhor a compreender o ponto de conexão do mesmo ao sistema.

O circuito é alimentado por duas baterias, *powerbanks*, com ligação USB, *Universal Serial Bus*, de 5 Volt, conectadas em série, que providenciam uma tensão de alimentação de 10 V. Um conjunto de reguladores de tensão gera as tensões necessárias para os diversos blocos constituintes do sistema e para o *ECG front-end*, a placa de circuito impresso do microcontrolador (representada como microcontrolador na figura 2) inclui um regulador de tensão para alimentação do microcontrolador (3.3 V) e um regulador de tensão para alimentação do cartão de memória (5 V). A tensão de alimentação dos conversores analógico-digital e digital analógico é filtrada para atenuação do ruído e interferência.

O microcontrolador fornece amostras de sinal aos conversores digital-analógico (D/A), através de uma interface SPI, *Serial Peripheral Interface*, e estes geram as componentes de modo comum e diferencial do sinal ECG. As componentes do sinal ECG entram num amplificador diferencial com saída diferencial, *fully differential amplifier*, e este converte as componentes de modo comum e diferencial num sinal ECG diferencial. As tensões geradas pelos conversores D/A são relativamente elevadas, tipicamente na ordem das centenas de milivolt ou alguns Volt, estes sinais apresentam elevada amplitude quando comparados a um sinal ECG típico, que apresenta valores de amplitude pico-a-pico na ordem dos milivolt ou centenas de microvolt. Por forma a contornar este problema, um atenuador é colocado à saída do amplificador com saída diferencial, com o intuito de atenuar o sinal de ECG para valores de amplitude mais reduzidos. Dois circuitos de impedância variável simulam o modelo da interface pele-eléctrodo, de acordo com o *single time constant model*, proposto por Swanson e Webster [Swanson D. K., Webster J. G.; A model for skin-electrode impedance, *Biomedical Electrode Technology - Theory and Practice*, pp. 117-128, Academic Press, 1974], apresentado na figura 3.

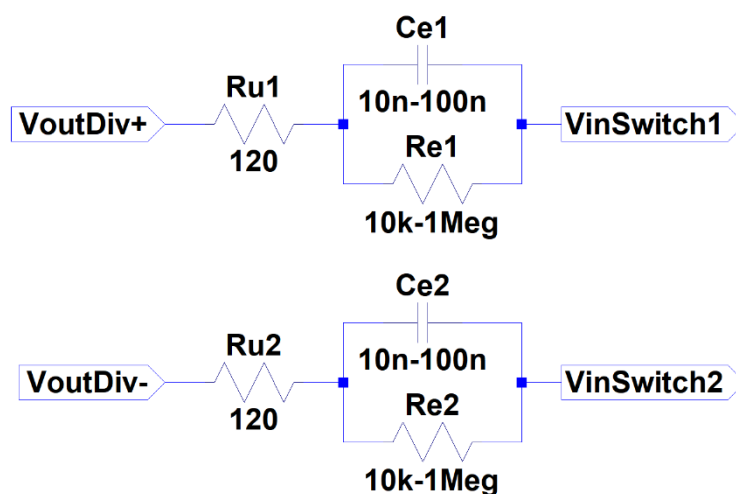


Figura 3: *Single time constant model* proposto por Swanson e Webster [Swanson D. K., Webster J. G.; A model for skin-electrode impedance, *Biomedical Electrode Technology - Theory and Practice*, pp. 117-128, Academic Press, 1974], mostrando a gama de valores configuráveis de resistência e capacidade

O modelo da interface pele-eléctrodo é simulado por uma resistência fixa de $120\ \Omega$, que representa a resistência dos tecidos desde o coração até ao ponto de ligação do eléctrodo, esta resistência tem pouca influência no ECG, devido ao seu valor reduzido. E, a componente mais importante do modelo de interface-pele eléctrodo, é o circuito formado por uma resistência (R_{e1} , R_{e2}) e por uma capacidade (C_{e1} , C_{e2}) em paralelo, que simulam o contacto do eléctrodo com a pele. O ajuste ou a variação do valor da resistência, pode ser efetuado entre $10\ \text{k}\Omega$ e $1\ \text{M}\Omega$, o elemento do circuito que efetua esta variação é um potenciómetro digital de 8 bit. Para simulação da capacidade uma técnica inovadora é utilizada.

O circuito de capacidade variável incorporado no sistema utiliza dois amplificadores de transcondutância e dois condensadores de referência para simulação de capacidades entre $10\ \text{nF}$ e $100\ \text{nF}$ [J. Costa, D. Almeida, "Circuit to Reproduce an Electronically Tunable Capacitor", paper in preparation]. O esquema simplificado do circuito é mostrado na figura 4.

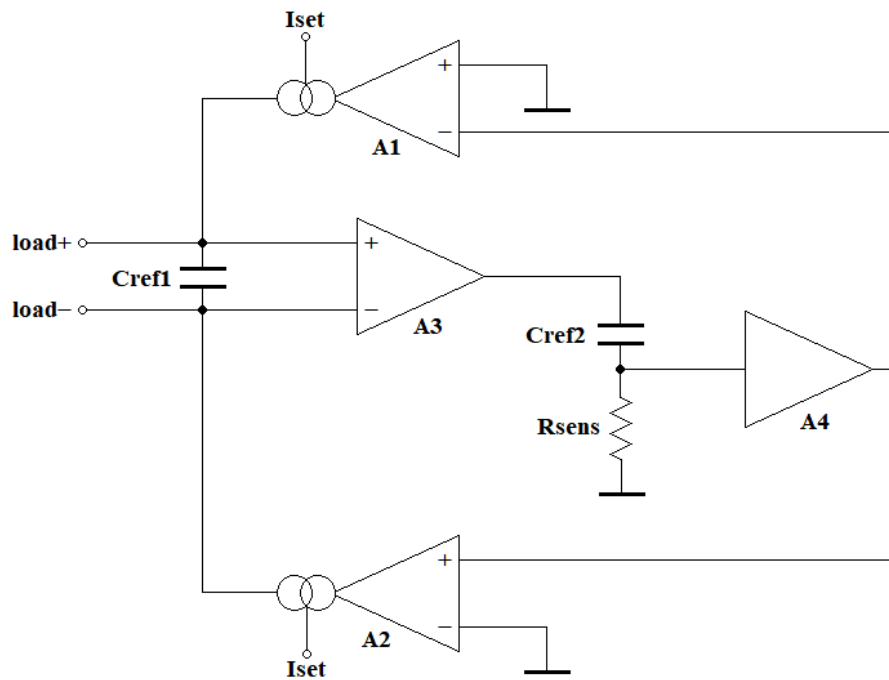


Figura 4: Circuito de capacidade variável [J. Costa, D. Almeida, "Circuit to Reproduce an Electronically Tunable Capacitor", paper in preparation]

O modo de operação do circuito é relativamente simples, existem dois condensadores de referência (C_{ref1} e C_{ref2}), uma resistência (R_{sens}), dois amplificadores de transcondutância com ganho ajustável (A1 e A2), um amplificador de instrumentação de ganho unitário (A3) e um seguidor de tensão (A4).

A tensão é aplicada aos terminais do circuito (load+ e load -), sendo medida pelo amplificador de instrumentação (A3), esta tensão é aplicada à malha RC composta por (Cref2 e Rsens), Rsens tem um valor baixo, logo a tensão aplicada aos terminais do condensador Cref2 será aproximadamente a mesma que a presente à entrada (aos terminais de Cref1). A corrente que flui através de Cref2, atravessa também a resistência Rsens, considerando que A4 tem impedância de entrada infinita e corrente de polarização nula, a diferença de potencial aos terminais de Rsens, permite “medir” a corrente que passa no condensador, fazendo uma conversão corrente tensão, na qual a corrente apresenta a mesma variação que a tensão medida em Rsens. Esta tensão é aplicada à entrada de dois amplificadores de transcondutância (A1 e A2), que atuam como fontes de corrente controladas por tensão em oposição de fase, note-se que o sinal não é aplicado à mesma entrada nos dois amplificadores, o amplificador de transcondutância A1 comporta-se como *sink* drenando corrente do nó load+ e o amplificador A2 comporta-se como *source* injetando corrente no nó load-. A capacidade pode ser controlada através do ajuste do ganho dos amplificadores de transcondutância, modificando o valor da corrente Iset, que pode ser fornecida por um conversor digital-analógico de elevada resolução, através de uma resistência ligada a cada terminal Iset, sabendo a queda de tensão na resistência, é possível determinar o valor da corrente, do ganho de transcondutância, e, por fim, da capacidade.

Existem ainda mais elementos no diagrama de blocos da figura 2, tais como um interruptor digital, para desligar os elétrodos simulados e efetuar testes de recuperação após *lead-off*. Um conversor analógico-digital (A/D), que permite a aquisição de sinal à saída do dispositivo em teste. E, por último, um cartão de memória que armazena os ficheiros de definição de teste, da forma de onda de eletrocardiograma, e o sinal adquirido à saída do dispositivo em teste.

Este sistema é unicamente controlado por ficheiros em cartão de memória, não sendo necessária a conexão a uma outra máquina, como, por exemplo, um computador, para a realização de testes. É, no entanto, necessário um computador, para edição e escrita de ficheiros de teste, para geração dos ficheiros de forma de onda de eletrocardiograma, para leitura e interpretação de resultados do ficheiro gravado à saída do *ECG Front-end*. Os dois ficheiros de teste são, um ficheiro de um período de onda ECG em formato WAVE, e um ficheiro de texto simples para especificação dos testes a realizar. O ficheiro de resultado tem a duração do teste e contém as amostras da tensão de saída do *front-end* em formato WAVE.

List of Acronyms

AC – Alternating Current

ADC – Analog-to-Digital Converter

ARM – Acorn RISC Machine or Advanced RISC Machine

ASCII – American Standard Code for Information Interchange

CDAC – Capacitor DAC

CLK - Clock

CMOS – Complementary Metal-Oxide-Semiconductor

CMRR – Common-Mode Rejection Ratio

CS – Chip Select

DAC – Digital-to-Analog Converter

DC – Direct Current

DNL – Differential Nonlinearity

DUT – Device Under Test

ECG – Electrocardiography, Electrocardiogram or Electrocardiograph

EEG – Electroencephalography

EM – Electromagnetic

EMI – Electromagnetic Interference

EMG – Electromyography

EOG – Electrooculography

ESD – Electrostatic Discharge

ESL – Equivalent Series inductance

ESR – Equivalent Series Resistance

FAT – File Allocation Table

HPF – High-Pass Filter

HS – High Speed

IA – Instrumentation Amplifier

IC – Integrated Circuit

IDE – Integrated Development Environment

I²C – Inter-Integrated Circuit

INL – Integral Nonlinearity

I/O – Input/Output

LCR – inductance/Capacitance/Resistance

LED – Light Emitting Diode

LOD – Lead-Off Detection

LPCM – Linear PCM

LSB – Least Significant Bit

MISO – Master Input Slave Input

MOSI – Master Output Slave Input

MSB – Most Significant Bit

NTFS – New Technology File System

OTA – Operational Transconductance Amplifier

PC – Personal Computer

PCB – Printed Circuit Board

PCM – Pulse-Code Modulation

PIO – Programmed Input/Output

PPG – Photoplethysmography

PSRR – Power Supply Rejection Ratio

RAM – Random-Access Memory

RC – Resistance/Capacitance

RF – Radio Frequency

RFI – RF Interference

RIFF – Resource Interchange File Format

RISC – Reduced Instruction Set Computing

RMS – Root Mean Square

SAR – Successive Approximation Register

SCL – Serial Clock Line

SCLK – Serial Clock

SD – Secure Digital

SDA – Serial Data line

SDI – Serial Data Input

SDO – Serial Data Output

S/H – Sample and Hold

SNR – Signal-to-Noise Ratio

SOA – Safe Operating Area

SPI – Serial Peripheral Interface

SPICE – Simulation Program with Integrated Circuit Emphasis

SRAM – Static RAM

SS – Slave Select

USART – Universal Synchronous and Asynchronous Receiver-Transmitter

USB – Universal Serial Bus

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1 Introduction

1.1 Motivation

Biopotential measurement equipment is indispensable for medical diagnosis and research, ECG (electrocardiography), EEG (electroencephalography), EMG (electromyography) and EOG (electrooculography) recordings are used to better understand our health, and to promptly diagnose diseases that can compromise our life and welfare.

In our society, technology is becoming more and more part of our lives, cars and other vehicles are becoming safer and safer and with more “smart” features, *smartphones* can do almost the same and in some cases more than some older computers, why not use this devices to better understand our health, instead of having to spend time and money to do an health check-up in a medical facility? Another advantage is the development of non-intrusive biopotential measurement technics and equipment to incorporate in cars, *smartphones*, tablet PCs, among others. A more sophisticated version of these devices could be used in doctors' offices in routine consultations, in emergencies in difficult-to-access places and in the hospital screening process, in conjunction with other tests such as PPG and / or blood pressure and blood glucose levels, this method provides a more detailed preliminary diagnosis, and may even help save lives and detect very serious and potentially life-threatening health conditions, in situations where the use of conventional ECG equipment is impractical.

ECG testing equipment is more oriented to diagnostics and monitoring equipment used in medical facilities, like hospitals and diagnostic centers, where the equipment is very reliable and the conditions are nearly ideal. This sort of equipment is more oriented to test several types of arrhythmia, including some life threatening health conditions, that should generate audible and visible warnings from the ECG monitoring equipment to alert the medical professionals, as well as helping them with the diagnosis and necessary treatments.

1.2 Goals

The solution developed and studied in this work is intended to help researchers make ECG and other biopotential measurement equipment less intrusive and more affordable. The main goal of this project is to make a prototype that aids the biomedical engineers in the development of non-intrusive and user friendly devices for everyone.

The proposed system allows a completely different set of tests that is lacking in the current ECG testing equipment, the main features introduced are simulation of the skin-electrode equivalent circuit for different types of electrodes, dry-electrodes and non-contact (insulated) electrodes, that can be used to implement ECG solutions to be incorporated in smartphones, tablets, laptops as well as in the steering wheel of vehicles [1], due to the fact that's not adequate to use gel electrodes and uncomfortable electrodes in those situations, in some of them, like while driving, it would reveal to be completely impractical. Tests that are currently lacking in ECG testing equipment can be performed, like lead off detection time, the necessary time for the ECG device under test to display a correct waveform after leads applied (settling time), as well as many other tests, currently found in the existing ECG testing equipment, like arrhythmia and abnormal heart conditions, that could warn users and maybe even help saving lives, by detecting heart conditions promptly, after more notorious complications arise, compromising the user's life quality. ECG front ends could be tested in "closed loop" – i.e. the output signal is analyzed to evaluate the quality of the ECG signal obtained, the circuit can operate with or without a right leg reference electrode, this feature could also not be very helpful, for example, while driving, and most people would prefer to just grab the steering wheel of a vehicle [1], a smartphone, tablet, or other gadget with both hands to obtain the ECG trace, heart rate and illness diagnostics.

1.3 Document Organization

The remainder of the document is organized as follows:

- The remainder sub-chapters of chapter 1 provide fundamental concepts, helpful to better understand the importance and scope of this project. A summary of the most important aspects of biopotential signal acquisition is included, as well as a comparison between state-of-the-art ECG test equipment and the system proposed;
- In chapter 2 the circuit's architecture is presented, the most important aspects of hardware and software development as well as the theory of operation are explained;
- In chapter 3 the variable capacitance circuit is tested. A series of tests are performed, to evaluate the performance of an ECG front-end;
- Chapter 4 finalizes the document, conclusions are taken, and some design considerations are made, future improvements are discussed.

1.4 Biopotential Acquisition and Measurement

1.4.1 The Biopotentials

There are diverse measurable biopotentials with clinical significance, like the ECG (electrocardiography), a medical examination that studies the electrical activity of the heart, the EEG (electroencephalography), studies the electrical activity of the encephalon (brain), EMG (electromyography), studies the electrical activity of skeletal muscles, and the EOG (electrooculography), studies the electrical activity of the eye. Table 1.1 contains information comparing the ECG with other biopotentials [2].

Source	Amplitude (mV)	Bandwidth (Hz)	Sensor (Electrodes)	Error Sources	Applications
ECG	1-5	0.05-100	Ag/AgCl	Motion artifacts, 50/60 Hz mains interference	Diagnosis of ischemia, arrhythmia and conduction defects
EEG	0.001-0.01	0.5-40	Au/Ag/AgCl	Thermal (Johnson-Nyquist) noise, 50/60 Hz mains interference	Sleep studies, seizure detection, cortical mapping
EMG	1-10	20-2000	Ag/C or stainless steel	RF interference, 50/60 Hz mains interference	Muscle function, neuromuscular disease, prosthesis
EOG	0.01-0.1	0-10	Ag/AgCl	Skin potential motion	Eye position, sleep state, vestibulo-ocular reflex

Table 1.1. Biopotential sources [2]

As can be noticed from the table above, there are two main characteristics common to all biopotentials [2]:

- The small to very small amplitudes (1 μ V to 10 mV)
- Low frequency range (from 0 Hz to 2 kHz)

The two main problems that affect biopotential acquisition are [2]:

- The presence of biological interference (skin-electrode interface impedance mismatching, motion artifacts, among others)
- Noise from the environment (mains interference, radio frequency interference, electromagnetic interference, switching power supply noise, among others)

1.4.2 The Biopotential Amplifier

Biosignals have very low amplitudes, the signal-to-noise ratio of the amplifier must be high, and the noise level should be very low, the signal path must be shielded against the most common sources of interference, like, for example, from the 50/60 Hz mains [3].

The amplifiers used in biopotential measurement or recording must have the following characteristics [3]:

- High differential gain (to amplify the low amplitude biosignals);
- Low or very low common-mode gain, high CMRR (a high common-mode rejection ratio is required for noise rejection in differential signals);
- Low noise level (as previously referred, a high Signal-to-Noise ratio is desirable, because it leads to a more accurate representation of biosignals, since the biopotentials have low or very low amplitude, a very low noise level is required);
- Stability against temperature and voltage variations (the circuit must behave in the same way, even if temperature or supply voltage changes over time, to provide accurate and reliable measurements);
- Electrical safety, comprising mains and earth ground isolation (to protect the patient or subject under test against hazardous currents that could flow to the body through the electrodes, usually a transformer, an opto-isolator or an isolation amplifier is used, the equipment could also be operated “off-grid”);
- Defibrillation protection (not all equipment are required to have this sort of protection, only hospital monitoring equipment must have it incorporated, however, all equipment must be protected from ESD).

1.4.3 The Instrumentation Amplifier

The instrumentation amplifier, if properly implemented, can combine the properties required for biopotential measurement (high to very high differential gain, low to very low common-mode gain, high common-mode rejection, high or very high input impedance). The vast majority of biopotential acquisition and measurement equipment rely on the instrumentation amplifier. These amplifiers are very simple and cheap, discrete opamps and integrated instrumentation amplifiers are commercially available, some might have an internal voltage reference generator, especially the ones used with single (asymmetrical) voltage supplies [3]. Figure 1.4.1 shows a generic instrumentation amplifier, which can be implemented in a discrete or integrated circuit, figures 1.4.2 and 1.4.3 show two implementations of the instrumentation amplifier in integrated circuits.

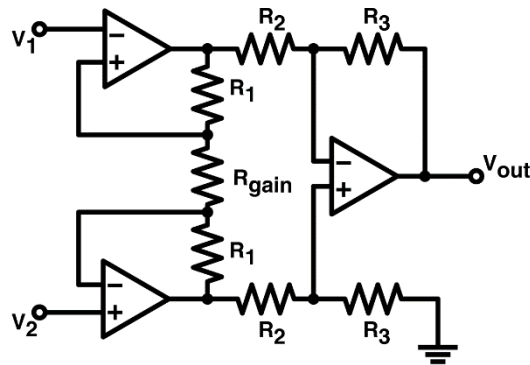


Figure 1.4.1. Instrumentation Amplifier [4]

The voltage output of the circuit is given by the following expression:

$$v_{out} = \left(1 + \frac{2R_1}{R_{gain}}\right) \times \frac{R_3}{R_2} \times (v_2 - v_1) [V]$$

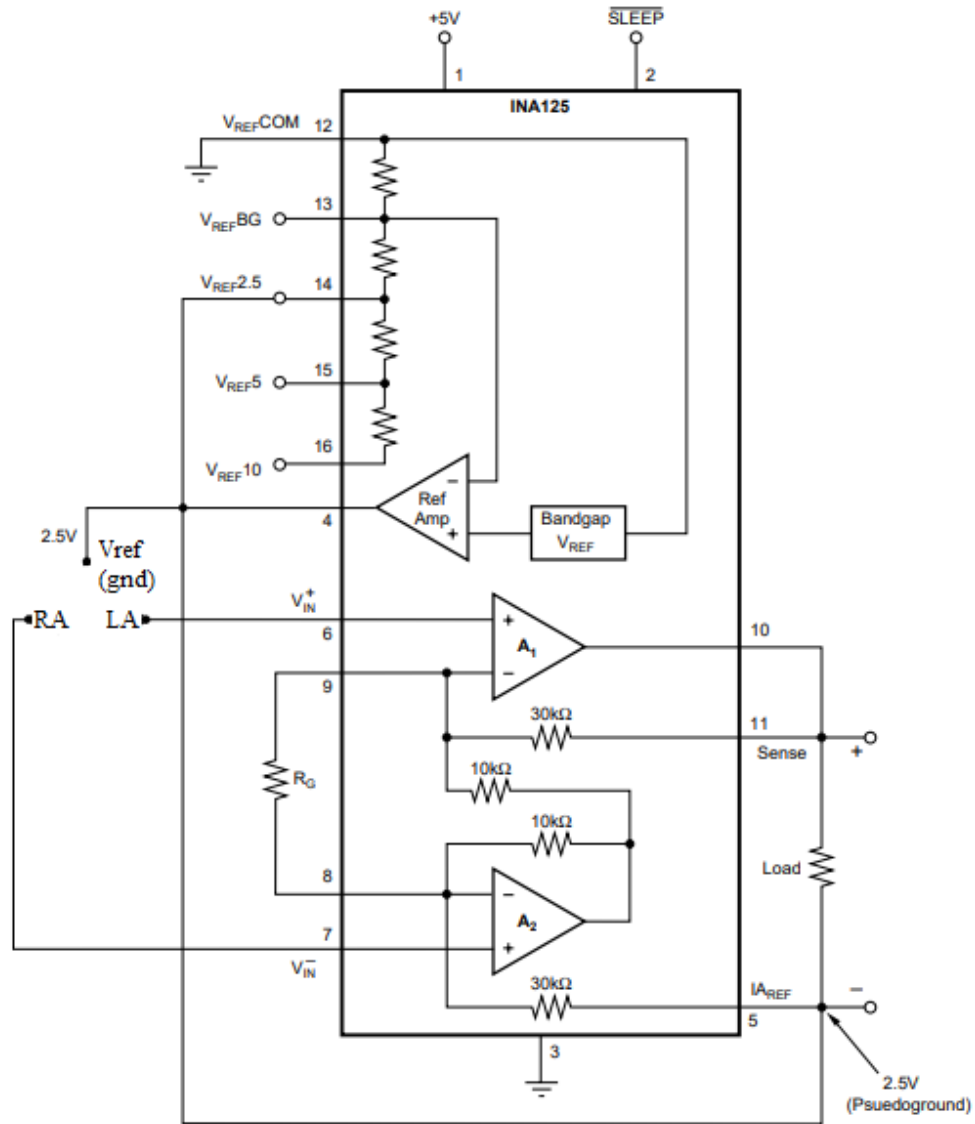


Figure 1.4.2. The INA125 from Texas Instruments Incorporated (Burr-Brown), an integrated instrumentation amplifier implemented with two opamps, and an internal voltage reference. ECG electrode connections represented for ECG lead I, and pseudoground set at 2.5 V (half supply voltage) [adapted from 5]

The voltage output of the circuit is given by (for a load impedance greater than 10 kΩ):

$$v_{load} = \left(4 + \frac{60k\Omega}{R_G}\right) \times (V_{IN}^+ - V_{IN}^-) [V]$$

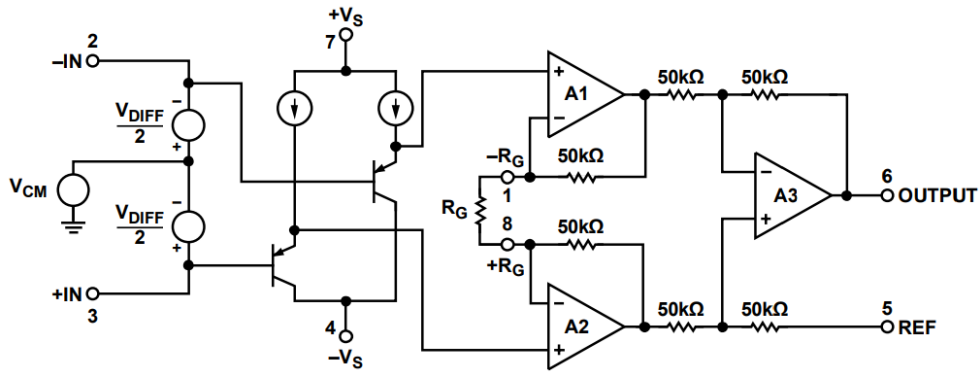


Figure 1.4.3. The AD623 from Analog Devices, an integrated instrumentation amplifier with voltage buffers at the inputs, incorporated to increase input impedance. This circuit uses the typical three opamp configuration [6]

The voltage output of the circuit is given by the following expression:

$$v_{load} = \left(\frac{100k\Omega}{R_G} \right) \times (v_{+IN} - v_{-IN}) [V]$$

1.4.4 Mains Interference Reduction

The mains interference is caused by the power lines, and is present in almost every place that has electric illumination and/or electric outlets. The reason for this interference is the fact that mains provide alternating current, the voltage function over time is generally a sinewave, with an RMS (Root Mean Square) voltage between 100 and 250 V, and an average frequency close to 50 or 60 Hz, this signal causes interference in sensitive equipment, due to capacitive coupling.

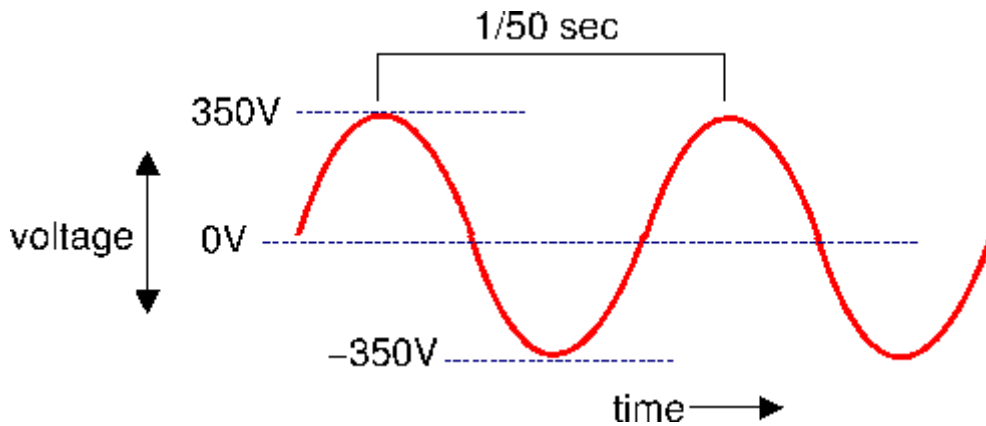


Figure 1.4.4. The variation of the mains voltage over time. Each cycle takes 1/50th of a second (meaning the fundamental frequency is 50 Hz) [7]

The capacitive coupling of the mains, causes interference to be added to the biosignals being measured or registered, this leads to incorrect measurements and incorrect waveform representation. Fortunately, in most cases, the signals are measured differentially, meaning that the noise appears with similar amplitude on both electrodes, ideally, this interference would be completely rejected by the biopotential amplifier. In practice, there is always some interference, due to the fact the CMRR is not infinite, and the interference does not affect all electrodes with the same amplitude [adapted from 2 and 3].

Sometimes, a third electrode (right leg electrode) is added to improve the CMRR and help rejecting the mains interference, in this solution, the average value of the common-mode voltage, is driven back into the body by a reference electrode [adapted from 2 and 3].

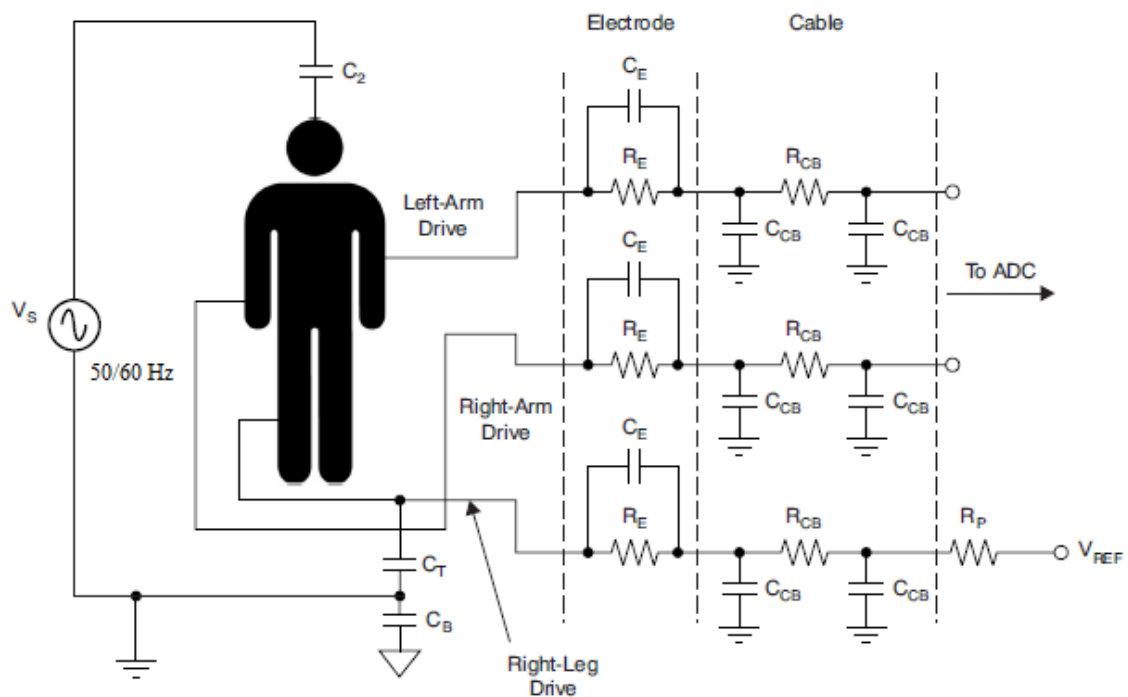


Figure 1.4.5. Applying the common-mode voltage at the patient's body [29]

1.4.5 Noise and Interference Filtering

The bandwidth of the biopotential amplifier must be limited to the range of frequencies of interest of the signal being measured or recorded (for example from 0.05 Hz to 100 Hz, in the case of the ECG front end) in order to reduce interference, and achieve more accurate results. In some cases, ferrite beads and small inductors, may be placed on the lead wires, to block high frequency electromagnetic interference (that could be caused by RF equipment or switching supplies). Another measure that could be taken, is the addition of small capacitors between each electrode lead and ground, to further improve the interference rejection. The DC potentials arising at the skin-electrode interface must be blocked, otherwise, due to the high voltage gain requirements, the amplifier could saturate, the use of a high-pass filter is recommended. At least one low-pass filter should be included in the amplifier chain, to reduce RF interference and reduce muscle artifacts. The mains interference, with a fundamental frequency of 50 or 60 Hz, and its harmonics (if present) are the biggest problem in biopotential measurement and acquisition [9, 10]. A notch filter may be incorporated to remove (or heavily attenuate) mains interference. Since a notch filter, even if digitally implemented, isn't ideal, its bandwidth differs from 0 Hz, some frequencies that have significance in the spectrum of the biosignal being measured, might be filtered, leading to distortion. The filter should be as close to ideal as possible, and should be avoided if maximum accuracy is desired [adapted from 2].

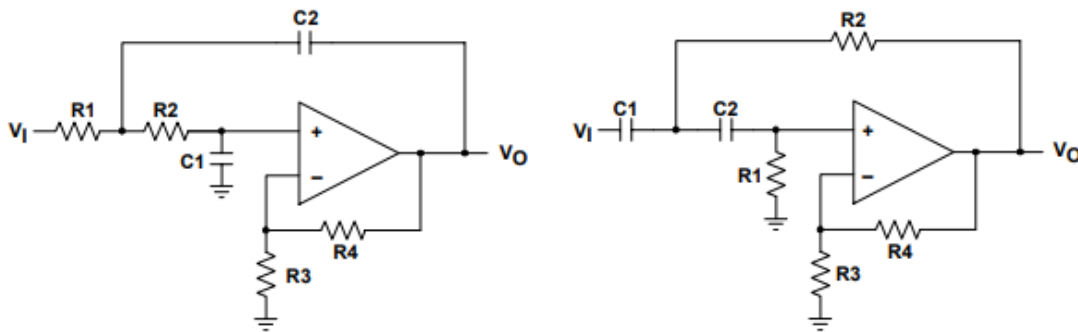


Figure 1.4.6. Second order Sallen-Key active filters, low-pass filter (on the left) and high-pass filter (on the right). These two filters could be used to implement a band-pass filter [11, 12]

The expression that gives the cut-off frequency of the filters (at half of the power) is the following (assuming that $C1 = C2$ and $R1 = R2$, for simplification) [11,12]:

$$f_{c(-3\text{ dB})} = \frac{1}{2\pi RC} \text{ [Hz]}$$

The expression that gives the quality factor of the filters is the following [11, 12]:

$$Q = \frac{1}{3 - K} = \frac{1}{3 - \left(1 + \frac{R_4}{R_3}\right)}$$

$\frac{R_4}{R_3}$ should be less than 2, values close to 2 or higher, result in instability and can make the circuit oscillate [11, 12].

The approximate value of the pass-band voltage gain is given by the following expression [11, 12]:

$$K = 1 + \frac{R_4}{R_3}$$

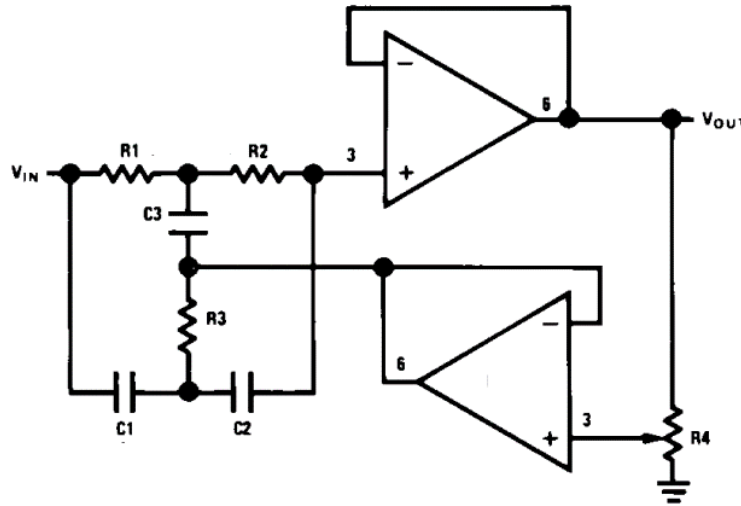


Figure 1.4.7. Adjustable Q Active Notch Filter [13]

The cut-off frequency of the notch filter is given by [13]:

$$f_{c(-3\text{ dB})} = \frac{1}{2\pi R_1 C_1} \text{ [Hz]}$$

The following conditions need to be met [13]:

$$R_1 = R_2 = 2R_3$$

$$C_1 = C_2 = \frac{C_3}{2}$$

1.4.6 Artifacts

The main source of artifacts is the potential arising at the skin-electrode interface [9]. The changes in the junction potential at the skin-electrode interface cause slow changes in the baseline (baseline wander), and, in some instances could cause a temporary saturation of the amplifier [14]. The event can be detected manually or automatically (by discharging a high pass-capacitor in the amplifier to restore the baseline) (figure 1.4.8) [2].

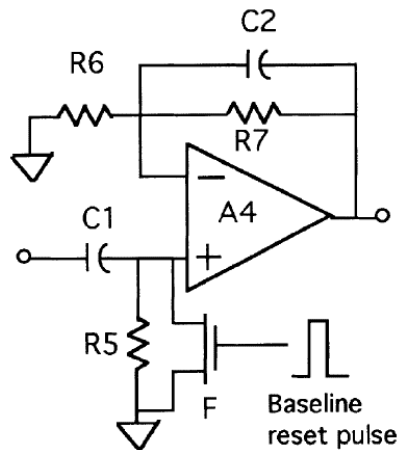


Figure 1.4.8. Artifact Detection Circuit [2]

The movement of the subject under test or the disturbances of the electrodes can produce motion artifacts [9]. These artifacts could be reduced using filters, but such filtering, typically high-pass, can cause distortion of the biopotentials being measured. Digital signal processing could be used to identify the artifacts and remove them from display.

A biopotential source, that could be the desired signal in one case, might cause artifacts in another case. As an example, the EOG signal from the eyes blinking can produce artifacts in EEG signals. The EMG signals cause artifacts in all the other biopotential measurements. ECG signals in particular, can show significant artifacts caused by EMG signals. The pacemaker pulse can be detected and amplified as a short pulse (of about 2 ms) preceding the QRS complex, it can trigger QRS detection, giving false heart rate measurements. Some circuits are designed to identify and remove this artifact [adapted from 2, 14].

1.4.7 Electrical Isolation

Electrical isolation improves the safety of the biopotential measurement and/or acquisition equipment, since it limits the amount of leakage current that flows from the instrument to the patient [15]. Leakage current to the instrument ground should be minimal and within safety limits, this current could be introduced by other sensors or equipment electrically connected to the patient's body [16]. Electric isolation can be optical, or electrical. In the first case, a opto-coupler, also called opto-isolator is placed in the signal path, the electrical voltage from the electrodes is amplified, modulated (these circuits have a power supply isolated from the mains and ground), and converted to light by a light-emitting diode (LED) driven by a transconductance amplifier, then the signal is converted back to an electrical current by a phototransistor, converted to voltage, demodulated, amplified and filtered. In the second case, a transformer is placed on the signal path between the electrodes and the amplifier stages, the transformer provides galvanic isolation, since the primary and secondary windings are electrically isolated, no direct path to ground exists.

The problem about using transformers are the frequencies of operation of such devices (usually high for small transformers), which are very different from the frequencies present in biosignals spectra, causing huge losses in a signal with very low power. A possible solution, consists in the amplification of the biopotential, using a low noise differential amplifier, and the modulation of a higher frequency carrier wave, that is suitable for the transformer, examples of this approach are the isolation (or isolated) amplifiers [2].

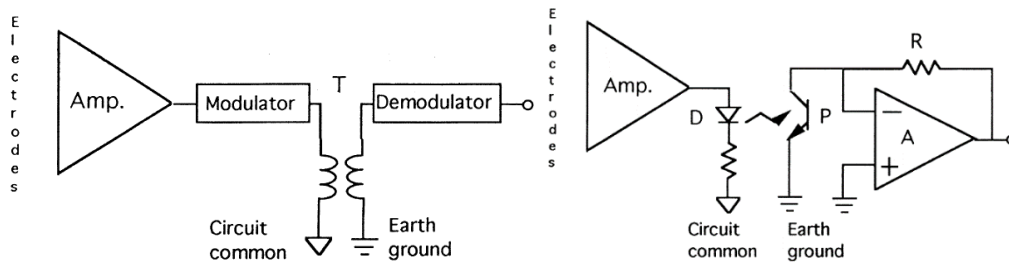


Figure 1.4.9. Transformer isolation circuit (on the left), optical isolation circuit (on the right) [2]

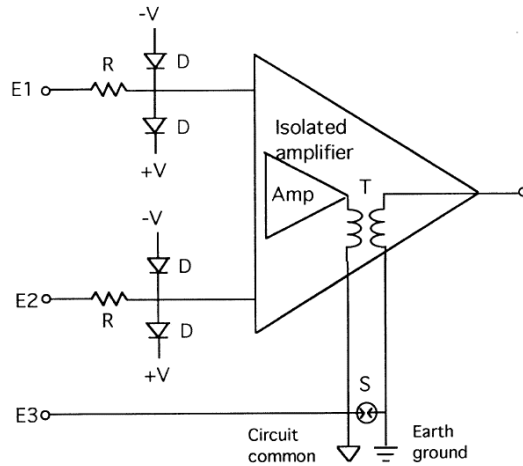


Figure 1.4.10. Isolation Amplifier [2]

1.4.8 Environmental Interference Reduction Measures

As previously stated, there are many sources of interference, like power lines (power mains), RF and EM interference caused by machines, RF equipment, digital devices, switched-mode power supplies, among others, are always present to some extent, at the place where the biopotential is acquired. Induced magnetic fields in the leads, as well as the electric currents induced onto the body (by capacitive coupling), are potential sources of interference.

The amplifier must be shielded as well as the electrodes and leads, to help reducing the interference, the case (chassis) of the equipment must be made of a ferromagnetic metal, connected to ground or to the circuit common and the wires should have an outer conductor also connected to ground or to the circuit common, if the case is not made of metal, the noise sensitive sections (low or very low amplitude signals) of the circuit should be shielded inside a metal box, that could also be connected to ground or common. The pair(s) of lead wires should also be twisted together to reduce the induced electromagnetic interference [2].

The circuit should also have filtering stages, as previously discussed, the interference should be attenuated and the desired signal should be amplified. RC filtering at the input of the amplifier stages is helpful in removing RF interference. The higher interfering frequencies can be blocked by a choke or an inductor in series with the input leads. As previously stated, grounding the chassis of the equipment and the lead wires is very helpful to reduce interference, specifically electromagnetic and electrostatic interference [2].

The capacitive coupling of the patient's body induces interfering currents that are picked up by the biopotential amplifier as common-mode voltage [17]. A high common-mode rejection ratio (CMRR) is an essential property of a biopotential amplifier [18]. The use a driven right-leg electrode, as previously explained, when possible, further improves the CMRR and interference rejection [2, 17].

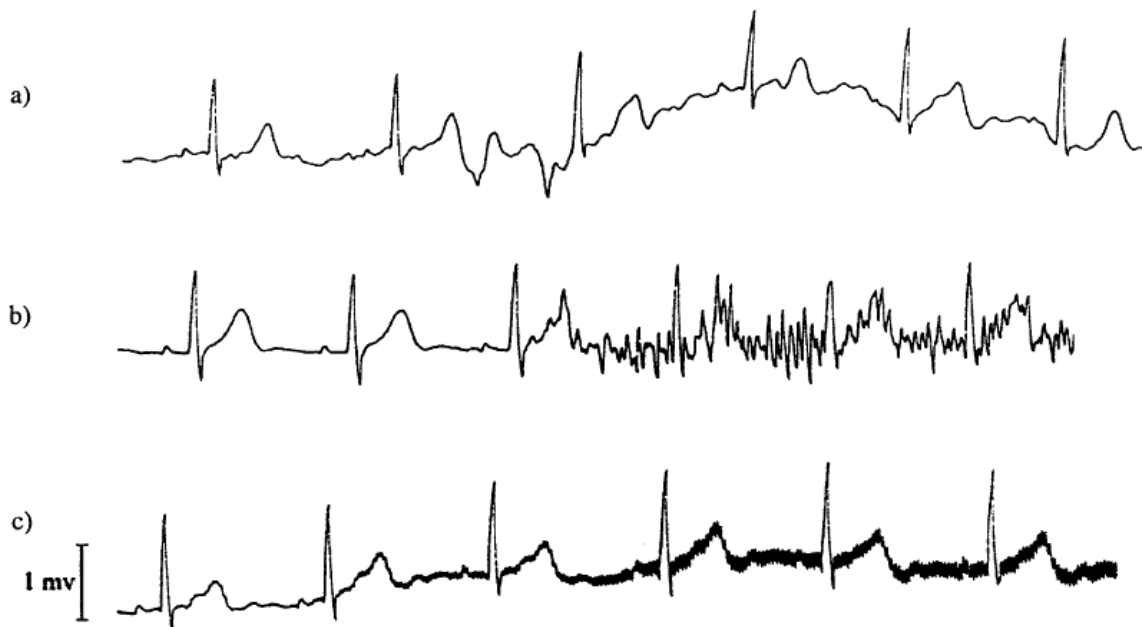


Figure 1.4.11. Examples of interference in ECG signals recorded: (a) baseline wander (possibly caused by respiration or motion), (b) muscle (EMG) signal interference, (c) electromagnetic interference (power mains [60 Hz] and RF) [2]

1.5 ECG Test Equipment

Nowadays, the electrocardiograph is an indispensable instrument to measure and record the electrical activity of the heart. It is used in medical examination centers, in hospitals and some other medical facilities, as it is very helpful to diagnose serious health conditions. The ECG is also performed in heart monitors, during some medical procedures that need anesthesia, like surgery, and in patients that need intensive care, or that are recovering from surgery or some serious illness. These devices should be very accurate, very robust and have to be able to withstand large surges, like those caused by defibrillation or electro-cauterization, they should also be very insensitive to artifacts and interference.

Instruments have been developed, to perform tests in heart monitors and ECG recording equipment, these instruments generate abnormal heart rhythms, interference and artifacts.

1.5.1 Importance

High quality test equipment is of vital importance, especially for medical applications, since the human life is considered the most valuable possession. Heart monitors and other ECG acquisition equipment for diagnosis purposes, must perform flawlessly, as a fault could result in death or severe injury to the patient being examined.

To insure maximum accuracy of the tests, the test equipment must be certified and properly calibrated, to insure it is operating in accordance with the norms and directives applied to medical equipment.

A series of tests must be performed regularly to medical equipment, like the electrocardiographs, to ensure maximum reliability and accuracy, the instruments must be working in conformity with the norms. The most common tests performed are made to ensure the proper detection of abnormal electrical activity of the heart, to evaluate the accuracy of the equipment, to assess the rejection of artifacts and interference, and finally to verify the safety of the equipment, that should be properly isolated from dangerous voltages, that could cause large currents to flow into the body, which would result in injury or even death of the patient.

1.5.2 Tests Performed

A relatively vast set of test features is implemented in state of the art ECG test equipment, the most common are (consult Appendix D):

- ECG signal generation
- Pacemaker waveform generation
- Arrhythmia simulation
- ST segment elevation and suppression
- Waveform generation
 - Sinewave
 - Square wave
 - Triangle wave
 - Triangle pulse
 - Square pulse
- R-wave detection
- Tall T-wave rejection test
- Mains interference (50/60 Hz sinewave waveform)
- Baseline wander



Figure 1.5.1. An example of state of the art ECG test equipment, the ProSim™ 8 Vital Signal and ECG Patient Simulator from Fluke Corporation (front panel view) [19]

1.5.3 Possible Improvements

All of the instruments presented, have a relatively similar set of testing functions (consult Appendix D). These instruments are developed to test medical equipment in which the accuracy and reliability is critical. The set of tests performed (or part of it) is based on a series of norms and directives, which must be fulfilled, to guarantee the safety and operability of the medical equipment. Since this industry is heavily regulated, the impedance of the electrodes and gel used, must be within certain levels, all the equipment must be properly grounded and protected from power surges.

In the future, ECG devices will be made more affordable and could even be an integrating part in daily use equipment. The home environment is very far from being noise and interference free, and the electrodes are different from those found in medical ECG equipment, gel-less electrodes may be used, and electrodes could be held with the hands, for example, instead of being attached to the body. This, of course, poses lots of issues, since the environment is full of interference (from Wi-Fi devices, switched-mode power supplies, power outlets, mobile telephony, among others). Since the electrodes could be held with the hands and gel-less electrodes are used, skin-electrode impedance will vary over time and will be different from person to person. It will be dependent of the skin type (that could be thicker or thinner and wetter or drier) and the size of the hands. The main problems related with non-professional ECG acquisition can be summarized in the following topics:

- Skin-electrode impedance variations (due to different skin types, different hand sizes, varying humidity of the skin, the usage of gel-less electrodes, unable to provide a low impedance conductive media between the electrodes and the skin, motion of the skin during the test)
- Environment interference (mains power, Wi-Fi, mobile telephony, switched-mode power supplies, electric motors and other sources of EM and RF interference)
- Artifacts (baseline elevations and depressions caused by motion, tremor and respiration, could be worsened if the electrodes are grabbed too lightly or too heavily, in the case of handheld electrodes)
- Safety and protection of the subject under test (isolation from dangerous voltages, power surges and spikes)

Most ECG test equipment is designed to operate with ECG acquisition systems that have at least three electrodes, two for differential biopotential measurement and one for the reference. Since nonprofessional ECG equipment could have only two electrodes, the test may not be properly performed.

The result of the tests can be visually and/or acoustically verified, but could not be recorded by the test equipment, because the ECG equipment used for monitoring and diagnosis, generally does not provide an interface (output or bidirectional) for the test equipment. The results, if needed, must be recorded in the equipment under test or on an external recording device. In this scenario, a more thoroughly computer analysis is complicated to perform. More flexibility of the tests performed might be desirable, with options such as:

- Adjustable common-mode and differential mode components of the signal*
- Skin-electrode impedance:
 - Different options of skin-electrode impedance
 - Skin-electrode impedance variation
 - Simulation of the variation of the skin-electrode impedance over time
- Lead-off detection time and recovery time**
- User defined waveform generation*

* some test equipment may already present similar features

** electrode malfunction is simulated on some ECG testers

1.5.4 Comparison with the Proposed Device

The comparison of existing equipment with the device proposed in this project, will be divided in two sections, the advantages, and the disadvantages of this novel ECG testing device, when compared to the existing state of the art ECG testing equipment. Both conventional and non-conventional testing methods are considered in this comparison. Tests performed to professional and non-professional ECG devices are considered.

Advantages:

- More flexibility of the tests performed (the operator is free to choose the adequate ECG test signal or arbitrary waveform, define its amplitude factor, the sequence of events, modify parameters over time and define the duration of the test);
- Individual adjustment of common-mode and differential components of the signal (amplitude, offset and frequency adjustment of the common-mode and differential components of the signal, used to test the noise rejection ability of the ECG front end);
- Adjustable skin-electrode impedance (the capacitive and resistive components of the skin-electrode model could be changed to simulate different types of electrodes, including gel-less electrodes and non-conventional electrodes);
- Variable skin-electrode impedance (the response of the ECG front end to skin-electrode variations over time could be tested, to simulate situations of poor skin-electrode contact). The capacitive value can be adjusted continuously using a digital to analog converter;
- Lead-off performance tests (lead-off events could be simulated with this device, to determine the lead-off recovery time);
- ECG signal recording (when the device is used to test ECG front-ends directly, the signal from the output of the front end can be recorded and posteriorly used to perform a more complete software analysis);
- Reduced cost.

Disadvantages (and possible improvements):

- The equipment developed in this project is currently able to test only one lead at a time (the current ECG testing equipment generally have the ability to test 12 leads, this could be implemented but with added costs and an increase in system complexity);
- The ECG test files must be edited before they are uploaded to the SD card (developers of the device could provide libraries with a set of tests to be performed, including arrhythmia traces, pacemaker simulation, ST segment elevation and depression, baseline wander, motion artifacts and performance test waves, like, for, example, T-wave rejection and QRS detection);
- The heart rate is fixed (the heart rate is the defined in the file loaded by the user, there are several solutions, not currently implemented, like, several wave files with different heart rates, or ECG wave compositing using separate waveform files);
- Only one file could be loaded at a time, meaning the user must change the test file definition each time the ECG waveform is changed (this problem is related to limitations of memory, if the test is temporarily halted during each wave change, giving time for the waveform to be loaded to memory, more than one waveform could be used in a single test).

2 ECG Test System

In this chapter the developed system is presented. A novel ECG testing equipment that comprises a new set of features that are not present in the currently produced ECG testing instruments. This chapter is divided in seven sub-chapters, organized as follows:

- System Architecture
- Circuit Description
- Skin-electrode Interface Simulation
- System's Mode of Operation
- Software Programing
- Simulations

In the System Architecture sub-chapter, the overall architecture of the circuit is presented, the system is shown as a block diagram and the functions of the different parts are superficially covered, the system is analyzed as a whole. In Circuit Description, each individual part's role in the system is explained. The Skin-electrode Interface Simulation sub-chapter introduces an innovative application for a variable capacitance circuit, developed specifically to simulate the reactive component of the skin-electrode impedance. In System's Mode of Operation, the interface protocols used to establish connections between the microcontroller and the circuit are clarified, the hardware-software relationship is covered, the user interface and the system's mode of operation are explained. Software Programing is a sub-chapter which focuses in microcontroller programing. Simulations is a sub-chapter reserved to SPICE simulation results.

2.1 System Architecture

The implemented system is intended to be used as an ECG Front-end performance tester. This system was designed to help the designers of non-professional ECG equipment, performing tests to the front-ends while the project is still in the development phase.

The implemented system, possesses many functionalities that are normally absent in state-of-the-art test equipment, it provides more flexibility of the tests performed. The user is allowed, not only to change the ECG wave and interference parameters, but also to adjust the parameters of the skin-electrode interface, like the skin-electrode impedance (that could also be variable during the test) and to perform lead-off event tests.

The circuit is composed of four main blocks (figure 2.1.1), like is shown in the simplified block diagram.

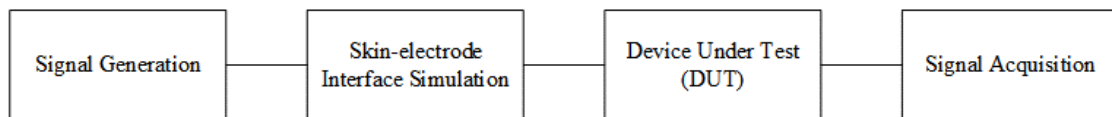


Figure 2.1.1. Simplified block diagram of the implemented system

The **Signal Generation** block is responsible for the generation of the ECG signal and the interference signals used during the test. This block is able to provide (an almost) noise free ECG waveform with amplitudes of about 1 mV. The **Skin-electrode Interface Simulation** block, implements an artificial skin-electrode interface, this block has customizable impedance and could be used for simulating the variation of the impedance over time. The Device Under Test or DUT is the ECG front-end or device that is currently being tested, it generally has a differential input and a single ended output. The signal acquisition block records the signal coming from the DUT and records it in a file, allowing the user to perform software analysis of the recorded data.

2.1.1 Block Diagram

To better understand the system architecture, a more complete block diagram is presented in this sub-chapter, the blocks now correspond to circuits that perform an important action in the system. The complete block diagram is presented on figure 2.1.2.

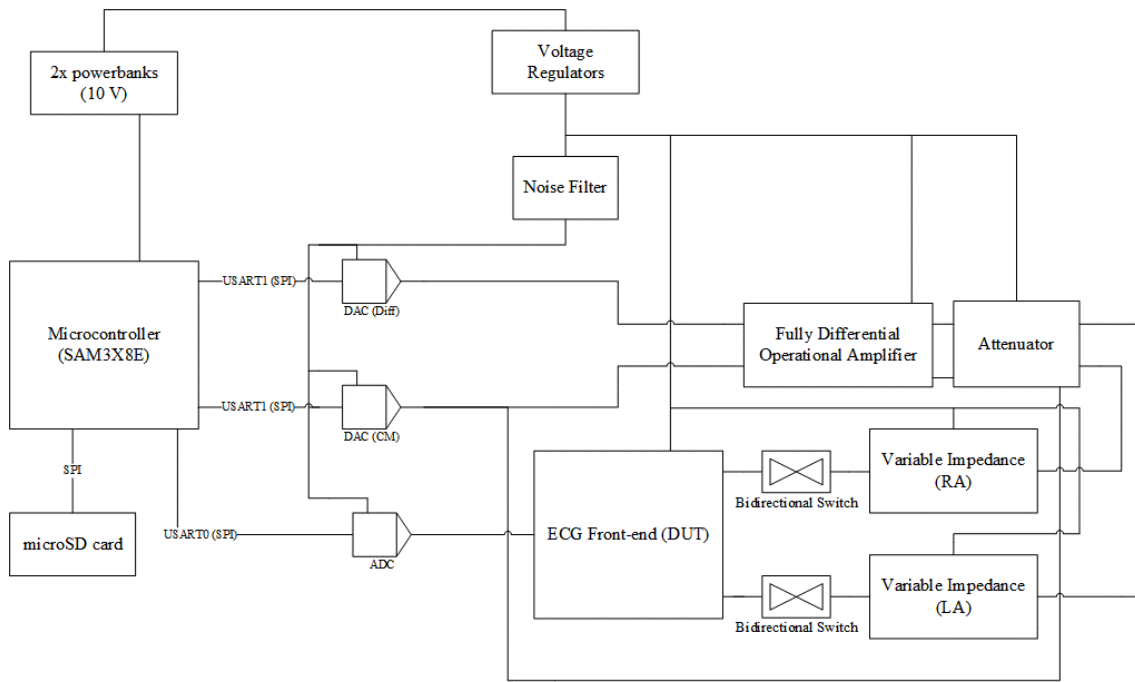


Figure 2.1.2. Complete block diagram of the implemented system

In the block diagram, a very important element is introduced, the Microcontroller, in this case, an ARM (SAM3X8E) from Atmel Corporation, found on the Arduino Due board. The block is responsible for controlling the test functions, impedance and lead-off control signals, signal generation, test file reading, signal reading and recording.

The “power supply section”, is formed, by two battery powerbanks in series (5 V + 5 V), and a set of voltage regulators to provide a stabilized voltage for the different elements of the system. The microcontroller (that is part of an Arduino Due clone board) has its own set of regulators, apart from the main circuit.

Two DACs are used to generate the common-mode and differential components of the test signal (though the DACs are shown separated in the diagram, they actually are part of a single integrated circuit). The **D**igital-**t**o-**A**nalog **C**onverters (DACs) generate the signals with samples supplied from the microcontroller, which is connected to this devices by an SPI interface.

The fully-differential operational amplifier, with differential and common-mode inputs and differential output, is used to convert the single-ended signals coming from the DACs into a differential signal. This conversion is needed because the electrocardiogram signal is differential.

An attenuator is needed to provide very low voltages at the input of the front-end, typically, the ECG amplitude values are between 1 mV and 5 mV [2].

Since the DAC's specified power supply voltages are much larger (usually between 2.5 and 5 V), and a precise, low drift, 10 mV or less power supply is difficult to implement. There are two low complexity and low cost solutions, one is the integer division of the signal by software, that can be done (and is actually performed), but it's not acceptable for very low amplitudes, because the signal loses resolution (number of steps available for amplitude representation) to a degree that causes an unacceptable amount of quantization error. The other solution consists in generating the signals with an amplitude of Volts or hundreds of millivolt and adding an attenuator to the signal path, a device that lowers the voltage amplitude of a signal.

The variable impedance circuits simulates the skin-electrode interface, these are controlled by the microcontroller, allowing the user to define the impedance as a constant value or to be varied over time. The impedance can be varied or defined as a constant, independently in both leads. The resistive and reactive components can also be varied or defined independently.

Two bidirectional switches are in the signal path, these switches are used to simulate lead-off, by disconnecting the signal from the DUT. The bidirectional switches are controlled by the microcontroller.

An **Analog-to-Digital Converter (ADC)** is incorporated in the system, to sample the signal coming from the DUT, the samples are sent to the microcontroller via an SPI interface.

The noise filter is incorporated to provide a noise free voltage, which is used as reference in the converters (ADC/DAC).

A microSD card slot is also included, the memory card stores at least two input files, the test file (a text file containing the test sequence) and one or more waveform files (containing the ECG samples for one period). The microcontroller records one output file containing the results of the test.

2.2 Circuit Description

In this section a more detailed description of the constituting elements of the system is made. The integrated circuits are introduced, accompanied by a brief explanation of the main desirable features the devices possess. Some circuit schematics are also shown, these were made using the software from Linear Technology Corporation, LTSpice. Some component models might have been replaced with similar models available on the software libraries.

2.2.1 Operational Amplifier

The operational amplifiers present in this system are OPA2350, the main reasons of choice are the low supply voltage operation (from 2.7 V to 5.5 V), the fact the opamp is rail-to-rail (input and output), the unity gain stability, the low input noise density ($5 \text{ nV}/\sqrt{\text{Hz}}$), the high input resistance ($10 \text{ T}\Omega$), due to the CMOS input stage, and the fact there are two opamps per package. This opamp also possesses other desirable features, like a high slew-rate ($22 \text{ V}/\mu\text{s}$), a wide gain-bandwidth product (38 MHz), and a relatively high open-loop gain (120 dB typically). Figure 2.2.1 shows the block diagram of the opamp [20].

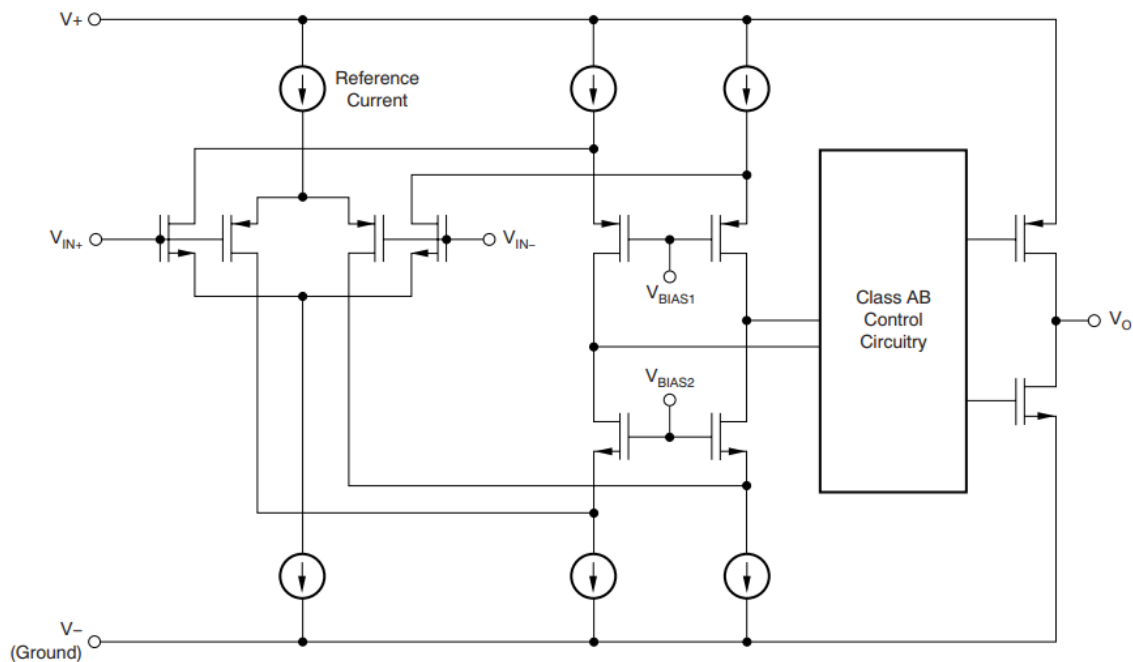


Figure 2.2.1. OPA2350 simplified schematic (only one opamp circuit is represented) [20]

2.2.2 Microcontroller

The microcontroller board is an Arduino Due, this board was chosen because it features a powerful 32-bit ARM processor running at a clock frequency of 84 MHz (the AT91SAM3X8E). The processor operates at a voltage of 3.3 V, so care should be taken while interfacing 5 V devices. It has 54 I/O pins which are more than sufficient for this application.

The Arduino Due also features two 12-bit Digital-to-Analog converters, and 12 analog input pins with 12-bit resolution, however, as explained further in the next paragraph, the supplies are noisy and the quality of the converted signals is not acceptable in the context of this project. The microcontroller has 512 KB of code (flash) memory and 96 KB of program (SRAM) memory, for this project. Two USARTs, an SPI and two I²C interfaces are available in the Arduino Due board, these are indispensable in this project [21].

The chosen board (Arduino Due) can be supplied from the USB 5 V, or using an external DC power supply with a voltage between 7 V and 12 V. At first, the system was intended to be supplied directly from the board (using the 5 V and 3.3 V supplies and an external 2.5 V regulator for the virtual ground), however, the board is not able to provide the necessary current safely. There is also another problem, the supplies are not “clean” enough, to provide a stable, interference free supply, for the noise sensitive analog circuits, like the converters (DACs and ADCs), differential amplifier and attenuator [21]. The Arduino Due board is shown in figure 2.2.2 [22].



Figure 2.2.2. Arduino Due board (top view) [22]

The Arduino is programmed using a PC connected to the programming port, without the need for another programming device, which makes it easier to program. Open source Arduino software is installed on the PC (the Arduino IDE illustrated in figure 2.2.3), and the programmer, defines the code in C/C++ language. Since Arduino is an open source project it has benefits, like a large variety of libraries and example programs provided from a large community of users.

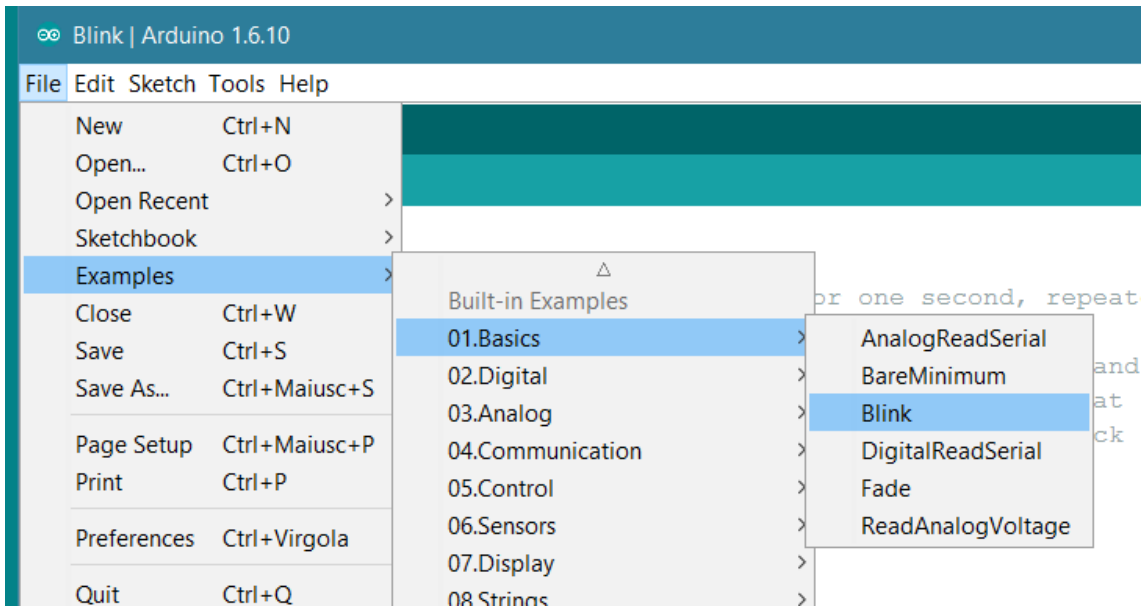


Figure 2.2.3. Arduino IDE (loading the LED blink example) [23]

All control functions of the system are performed by the microcontroller, it is responsible for controlling the I²C and SPI devices (in the role of master device), and the lead-off circuits.

The microcontroller supplies samples to the digital-to-analog converters at the desired signal generation sample rate (usually 1 kHz for the signal path and 100 Hz for control signals), and requests samples from the ADC at the desired signal acquisition sample rate (usually 1 kHz). It is also responsible for reading and interpreting the test file and the one period waveform file(s). The samples supplied by the ADC are recorded by the microcontroller. All files are stored in the SD card, which must be formatted as FAT16.

The code memory is stored in flash, this means the device's power could be cycled, or the device turned off, and the microcontroller does not need to be reprogrammed. Meaning that to operate the device it only needs to be plugged to the power supply, the microSD card should be inserted and then the reset button is pressed to start performing the test (red button in figure 2.2.2).

2.2.3 Memory Card Reader

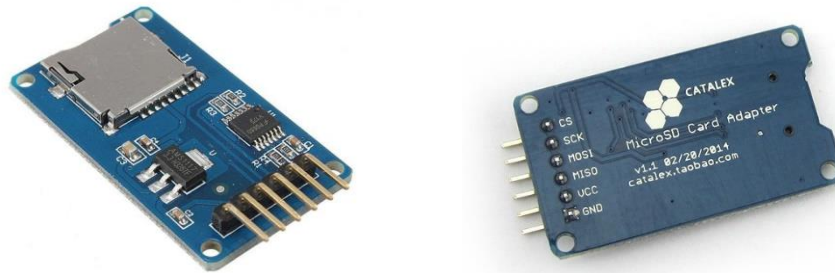


Figure 2.2.4. Catalex microSD card reader, top-view (on the left) [24], bottom-view (on the right) [25]

A microSD card reader is required in order to store the necessary files, the test file, waveform file(s) and to the record file. SD cards can be connected directly to an SPI interface, this mode of operation is supported, however, there is a drawback, because SD memory cards use 3.3 V logic and some microcontrollers 5 V logic (that is not the case of the AT91SAM3X8E that uses only 3.3 V logic). To protect the SD card from possible connections to 5 V logic SPI devices, the Catalex microSD card module features a 74VHC125 quad buffer with 3-state outputs. The tri-state control inputs are connected to the circuit common (or ground), like figure 2.2.5 illustrates. The buffers are unidirectional and can be used to interface 3.3 V to 5 V logic. Resistors of 3.3 k Ω are placed in series with the input of the buffer to limit current spikes.

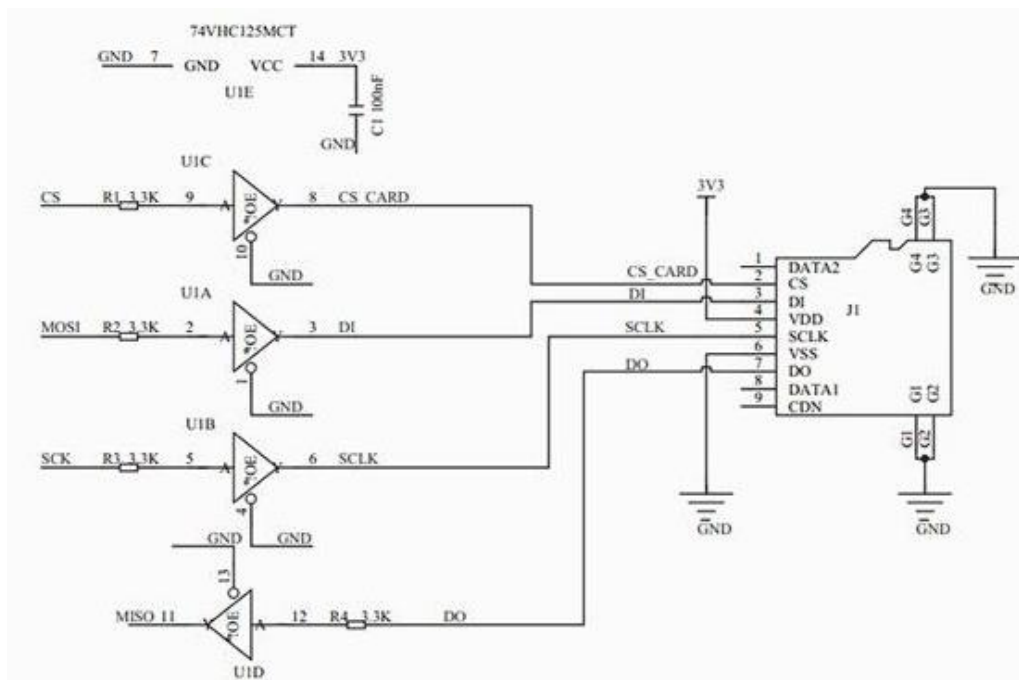


Figure 2.2.5. microSD card connections and 5 V logic to 3.3 V logic interface (buffers) [26]

The microSD adapter board has another integrated circuit, a 3.3 V linear voltage regulator (shown on figure 2.2.6).

The regulator circuit is used as power supply to the SD card and the buffer IC, due to the fact that the circuit is intended to be used with an external 5 V supply, which is provided in Arduino boards by the USB port connection. The 5V that supplies the 3.3 V memory card regulator in this project comes from the 5 V regulator included in the Arduino Due board.

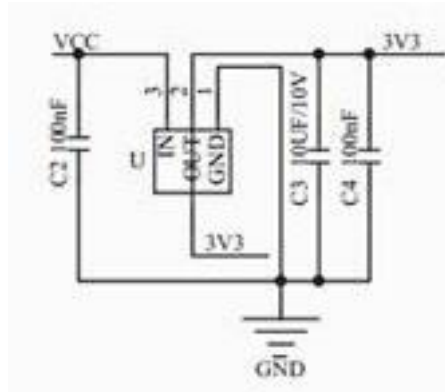


Figure 2.2.6. 3.3 V linear voltage regulator incorporated in the microSD card PCB [26]

2.2.4 Power Supply

The system is supplied from two independent USB voltage sources (5 V + 5V) connected in series. The voltage sources elected for this project are powerbanks. These devices are battery powered and can be operated “off-grid”, meaning less interference coming from the mains power, because batteries supply DC current only. The power supply also features filtering and reservoir capacitors. Two film capacitors (that act as filters, also called decoupling capacitors) are placed in parallel with two larger aluminum electrolytic capacitors (reservoir capacitors). The filter capacitors or decoupling capacitors avoid interference and high frequency oscillations in the power supply voltages, when, for example, digital circuits or high frequency circuits are operated. Reservoir capacitors provide a better power supply regulation, due to their high peak current, keeping the power supply sag low, during peak current demands. The schematic of the power supply circuit is presented in figure 2.2.7.

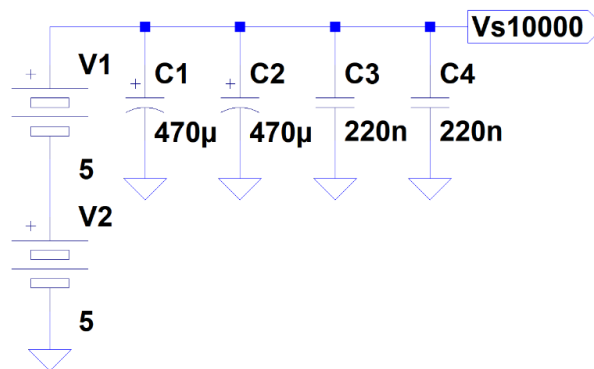


Figure 2.2.7. Power supply schematic, showing the two batteries connected in series, reservoir and decoupling capacitors

The USB supplies represented, must be independent of each other (must not share the same circuit common). Meaning that if the grounds (negative terminals) of both batteries are connected by a low resistive path, the voltage source V2 will be shorted. Such connection might seriously damage the battery and the wiring (by overheating), posing a risk of fire or injuries to the system operator.

The total current consumption of the circuit is about 230 mA while operating (220 mA in idle condition), of these, about 100 mA (90 mA in idle) of current are consumed by the Arduino board and microSD card shield, the rest of the circuit consumes about 130 mA of current. The powerbanks used to supply the circuit should have at least 1000 mAh of capacity.

2.2.5 Voltage Regulators

A voltage regulator is used to keep the supply voltage constant regardless of the load conditions, and the input voltage (that could vary over time due to battery discharge). The voltage regulators used in this project are LM317T adjustable linear regulators, meaning the output voltage can be set by defining the values of a resistive divider (R1 and R2), shown on figure 2.2.8. The LM317T has a wide output voltage range from 1.2 V to 37 V (the input voltage should be at least 3 V higher than the desired voltage), features current limiting (1.5 A), thermal shutdown and Safe Operating Area (SOA) control, making it a reliable regulator.

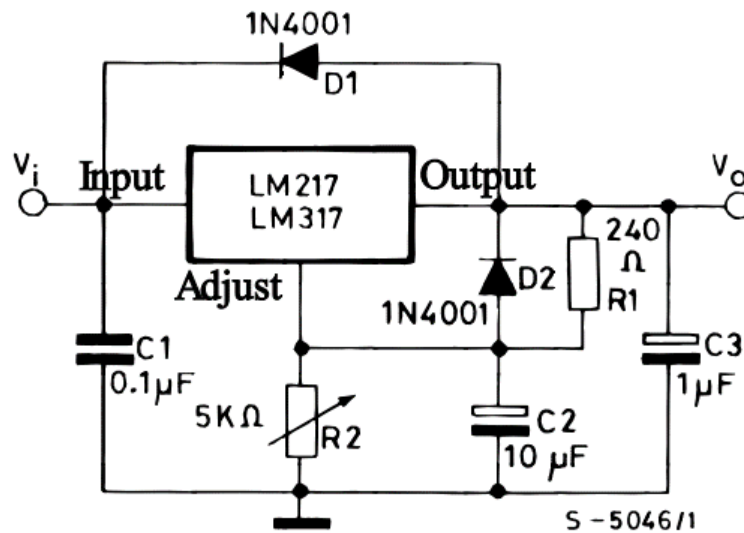


Figure 2.2.8. Voltage regulator showing the typical application [27]

The adjustment of the output voltage is performed by changing the feedback circuit resistors, R1 and/or R2, R1 is generally fixed (it is desirable to keep its suggested value to maintain the adjust pin current at the required value) and the value of R2 is adjusted accordingly to the needs.

The expression to calculate the output voltage is:

$$V_o = V_{ref} \left(1 + \frac{R_2}{R_1} \right) + I_{adj} R_2 [V]$$

Voltage references and regulators rely on bandgap voltage reference circuits, these produce a constant voltage that is independent of the temperature, voltage supply variations and loading conditions. It typically produces a voltage of about 1.25 V, the typical value of the reference voltage, V_{ref} . The value of I_{adj} typically is around 50 μ A (contributing to a raise in the output voltage of 50 mV per $k\Omega$ of R_2).

The typical application circuit (figure 2.2.8) also shows capacitors, which are used for power supply decoupling (C1 and C3) and to improve ripple rejection (C2). Two diodes are incorporated in the schematic (D1 and D2), these protect the device from capacitor discharge after power supply disconnection, when large output (D1) and adjustment terminal (D2) capacitors are used.

The simplified schematic of the LM317T regulator is shown in figure 2.2.9. The schematic shows the bandgap circuit, composed of four transistors (Q16, Q17, Q18 and Q19) and two resistors (R14 and R15). The series pass device and driver transistors are also included (Q26 and Q25). The rest of the circuit are constant current sources, protection circuits, feedback circuits and small value stabilizing capacitors [27].

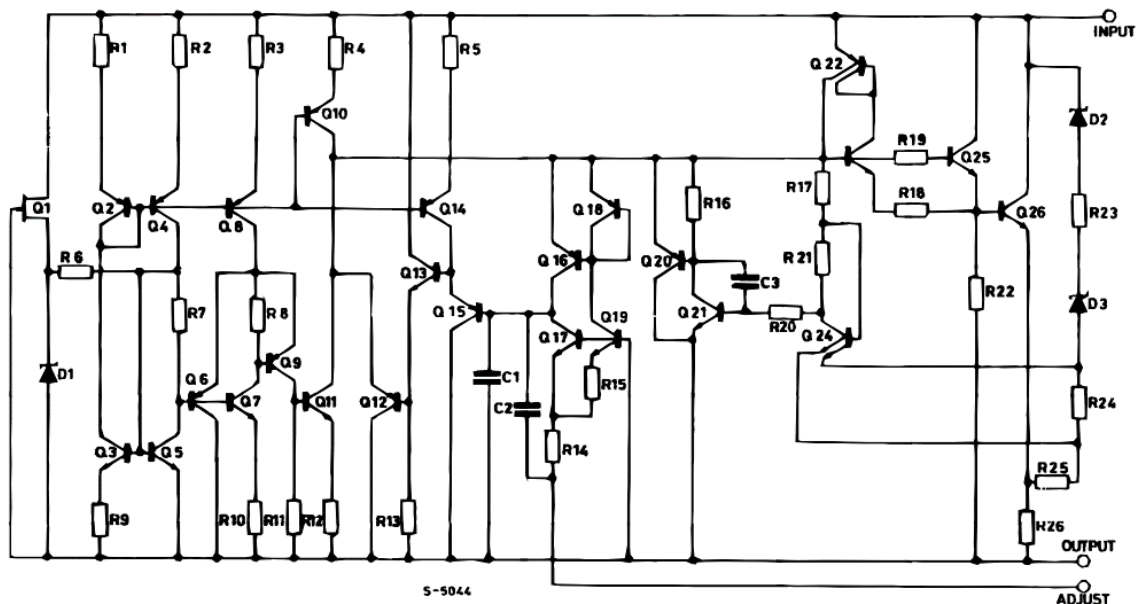


Figure 2.2.9. Simplified schematic of the LM317T linear voltage regulator [27]

5 V Regulator

A 5 V linear regulator supplies the analog sections of the signal generation and acquisition DACs and ADC, the analog circuitry, the lead-off circuit and the variable capacitance circuit. The LM317T is used to create this voltage from the 10 V power supply. Rearranging the expression of the output voltage of the regulator in order to obtain the value of the resistor R2, and considering the value of R1 220 Ω .

$$R_2 = \frac{R_1(V_o - V_{ref})}{I_{adj}R_1 + V_{ref}} = \frac{220 \times (5 - 1.25)}{50 \times 10^{-6} \times 220 + 1.25} \approx 654.2427 \Omega$$

The closest resistor value for the most common resistor series (E12) is 680 Ω , with this resistor value the voltage at the output of the regulator is:

$$V_o = V_{ref} \left(1 + \frac{R_2}{R_1}\right) + I_{adj}R_2 = 1.25 \times \left(1 + \frac{680}{220}\right) + 50 \times 10^{-6} \times 680 \approx 5.1476 \text{ V}$$

The value is closer to 5.1 V than to 5 V, but is still acceptable because the deviation is of less than 5 %. The circuit performance would not be affected by this variation. The schematic of the circuit is shown on figure 2.2.10.

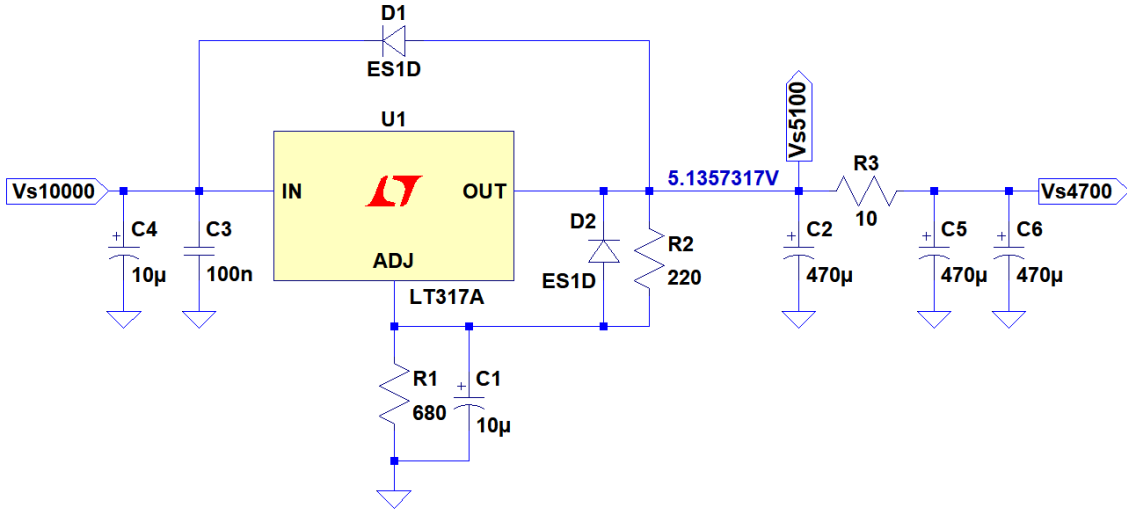


Figure 2.2.10. Schematic of the 5.1 V regulator with RC filter at the output

As can be noticed, in figure 2.2.10 another element is incorporated in the schematic, an RC filter formed, by R3, C5 and C6, this circuit element is used to lower the noise and interference present in the analog circuits' supply, however, because of the current consumption of about 40 mA of these circuits, the voltage at the output of this filter lowers to about 4.7 V. The cut-off (half power) frequency of the filter is given by the following expression:

$$f_{c(-3 \text{ dB})} = \frac{1}{2\pi R_3(C_5 || C_6)} = \frac{1}{2\pi \times 10 \times (470 \times 10^{-6} + 470 \times 10^{-6})} \approx 16.9314 \text{ Hz}$$

The cut-off frequency obtained even taking in account deviations from component's manufacturing tolerances is sufficient to cause attenuation to interfering signals (caused mains powerlines and digital noise).

The voltage labeled Vs10000 (10000 mV) is supplied by the powerbanks, the voltage labeled Vs5100 (5100 mV) supplies the variable capacitance circuits (that have a current consumption of about 80 mA), the voltage labeled Vs4700 (4700 mV) is used to supply the analog circuitry, analog section of signal generation and acquisition A/D and D/A converters and the lead-off circuit, it has in account the voltage drop caused by the 33 mA current passing through the filter resistor R3 (with a power rating of 1 W).

The diodes used are 1N4007s and not ES1D, and the regulator is an LM317T and not an LT317A, these devices were used in the schematic because they have similar characteristics and the LTSpice library does not contain the devices incorporated in the system.

Voltage measurements were made, the voltage value of Vs10000, depends on battery percentage, but usually has values in the range of 8.5 to 9.5 V. The voltage values of Vs5100 and Vs4700 are of 5.03 V and 4.7 V, respectively. The current supplied by this regulator is relatively large (being about 113 mA in total), which gives a total power dissipation in the regulator of (ignoring the regulator quiescent current, considering $I_i = I_o$):

$$P_{diss} = (V_i - V_o) \times I_o = (10 - 5.1) \times 113 \times 10^{-3} = 0.5537 \approx 0.6 \text{ W}$$

The power dissipated by the device is relatively high, meaning that the junction temperature must also be determined, to check if the device is in its Safe Operating Area (SOA), assuming an ambient temperature of 25 °C:

$$T_J = P_{diss} \theta_{JA} + T_A = 0.6 \times 50 + 25 = 55 \text{ }^\circ\text{C}$$

The junction temperature is relatively high and the regulator's case is very hot to the touch, however, the device is operating well within its Safe Operating Area. The limit of the safe operating temperature is 125 °C, and the power dissipation of the device is internally limited. The operating temperature of the device was measured at about 50 °C.

4.5 V Regulator

A reference voltage is required for the proper operation of the signal generation and acquisition A/D converter and D/A converters. This voltage should be almost noise and interference free. To supply the 4.5 V another LM317T linear voltage regulator is incorporated in the system.

The necessary R2 value (see figure 2.2.8 [LM317 description]), can be calculated using the following expression:

$$R_2 = \frac{R_1(V_o - V_{ref})}{I_{adj}R_1 + V_{ref}} = \frac{220 \times (4.5 - 1.25)}{50 \times 10^{-6} \times 220 + 1.25} \approx 567.0103 \Omega$$

The closest resistance value, for the most common resistance series (E12) is 560 Ω , using a resistor of this value gives an output voltage of:

$$V_o = V_{ref} \left(1 + \frac{R_2}{R_1}\right) + I_{adj}R_2 = 1.25 \times \left(1 + \frac{560}{220}\right) + 50 \times 10^{-6} \times 560 \approx 4,4598 V$$

This value is very close to the desired value of 4.5 V. The schematic of the voltage regulator and power supply bypassing and filtering is presented in figure 2.2.11.

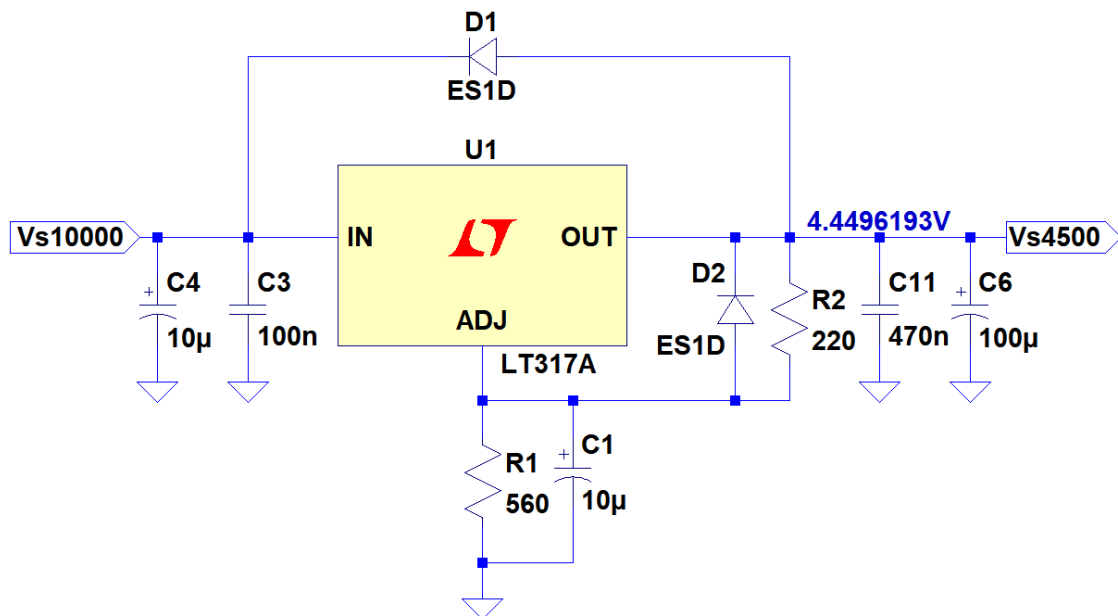


Figure 2.2.11. Schematic of the 4.5 V linear voltage regulator

The voltage labeled Vs10000 is supplied by the powerbanks, and the voltage labeled Vs4500 drives the input of the filter which drives the reference inputs of the A/D and D/A converters.

The regulator circuit implemented on the developed system uses a LM317T and 1N4007 diodes.

Reference Voltage Filtering

A low-pass filter is added after the regulator (voltage input labeled Vs4500) to improve interference rejection, an active filter implemented with two operational amplifiers. This filter circuit is suggested in the Analog-to-Digital Converter's (ADC's) datasheet [28].

The circuit is presented in figure 2.2.12. Power supply decoupling capacitors omitted on the schematic ($0.1 \mu\text{F}$ in parallel with $10 \mu\text{F}$, connected across the supply terminals of the opamps).

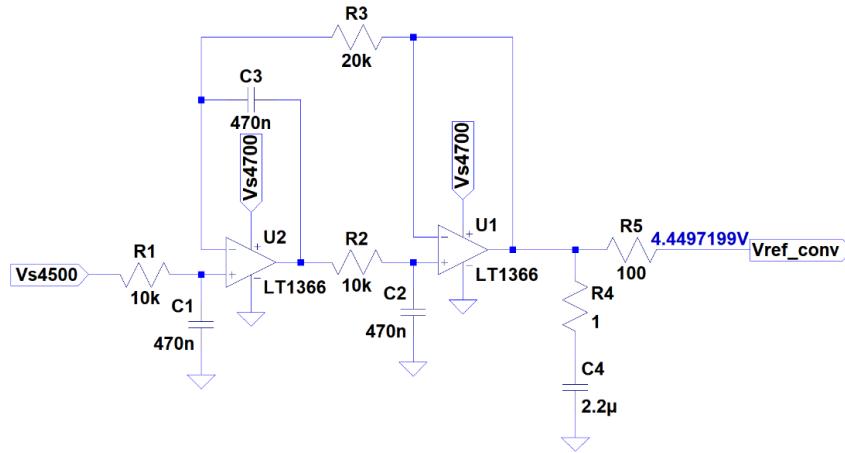


Figure 2.2.12. Low-pass filter that drives the voltage reference input of the converters

The operational amplifiers are supplied from the 5 V, filtered supply, Vs4700. The DC gain of the circuit is unity, and the cut-off frequency of the circuit (half power) is:

$$f_{c(-3 \text{ dB})} = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 10 \times 10^3 \times 470 \times 10^{-9}} \approx 33.8628 \text{ Hz}$$

The cut-off frequency of about 34 Hz, is adequate, because most of the interference occurs at frequencies of 50 Hz and above. A snubber circuit (Zobel network), formed by R4 and C4 is also incorporated to avoid high frequency oscillations, it has a cut-off frequency of:

$$f_{c(-3 \text{ dB})} = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 1 \times 2.2 \times 10^{-6}} \approx 72.3432 \text{ kHz}$$

As can be seen in figure 2.2.12 from the simulation of the operating point, the output voltage remains almost unchanged, with a value of about 4.45 V. The opamps used to implement the filter in the project are the two opamps contained in the OPA2350 integrated circuit package, the circuit was simulated with different opamps because LTSPice lacks the models for the opamp used.

The reference voltage of the converters, labeled Vref_conv in the schematic, was measured, and its value is of about 4.49 V.

3.3 V Regulator

Some circuits cannot be supplied with a voltage of 4.5 or 5 V, and may require a lower supply voltage to function properly, some devices may even be damaged if supply voltages higher than 3.5 or 3.6 V are used. As an example of these devices, is the ECG front-end used for testing, the AD8232, that can be damaged if the power supply voltage is higher than 3.6 V.

The regulator used to supply the 3.3 V is the LM317T, adjustable voltage regulator. The required R2 value (see figure 2.2.8 [LM317 description]), is calculated with the following expression:

$$R_2 = \frac{R_1(V_o - V_{ref})}{I_{adj}R_1 + V_{ref}} = \frac{220 \times (3.3 - 1.25)}{50 \times 10^{-6} \times 220 + 1.25} \approx 357.6527 \Omega$$

The value obtained for R2 is between two values of the E12 series of resistors, 330 Ω and 390 Ω . With a 330 Ω the voltage at the output of the regulator is:

$$V_o = V_{ref} \left(1 + \frac{R_2}{R_1}\right) + I_{adj}R_2 = 1.25 \times \left(1 + \frac{330}{220}\right) + 50 \times 10^{-6} \times 330 \approx 3.1415 V$$

The same equation is used to obtain the voltage output of the regulator with a 390 Ω resistor:

$$V_o = 1.25 \times \left(1 + \frac{390}{220}\right) + 50 \times 10^{-6} \times 390 \approx 3.4854 V$$

An analyses of the values, suggests that the value of R2 should be set to 330 Ω , because, a voltage of 3.5 V is higher than required, and given possible variations due to component tolerances, this voltage could not be suitable to power the AD8232 ECG front-end. The system must be designed to be robust and reliable, so a larger margin is more adequate. The circuit schematic is presented on figure 2.2.13.

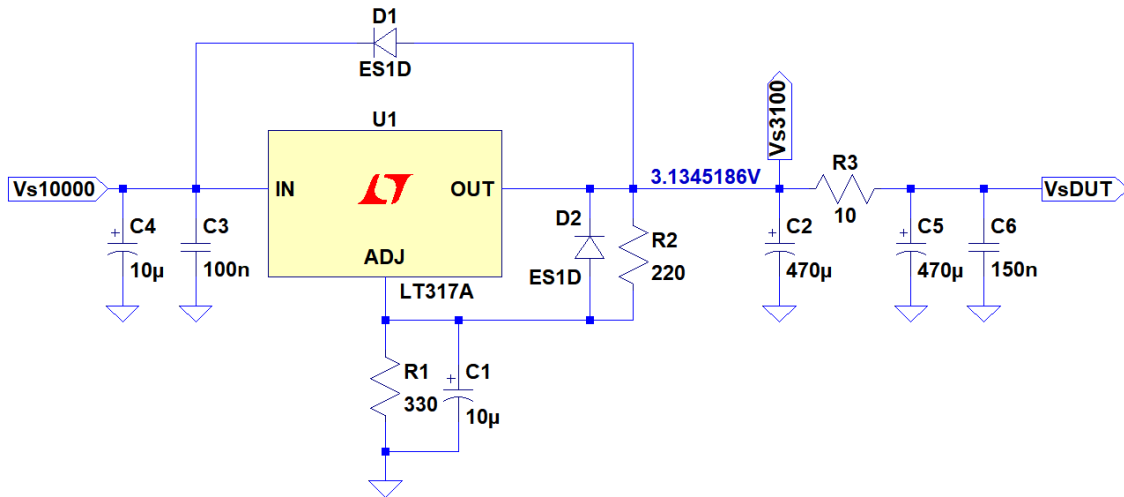


Figure 2.2.13. Schematic of the voltage regulator and RC supply filter

Like the 5.1 V supply, this voltage source also features an RC filter, formed by the components R3, C5 and C6, the cut-off (half-power) frequency of this network is given by the following expression (ignoring the contribution of C6 due to its low capacitance value when compared to C5):

$$f_{c(-3\text{ dB})} = \frac{1}{2\pi R_3 C_5} = \frac{1}{2\pi \times 10 \times 470 \times 10^{-6}} \approx 33.8628\text{ Hz}$$

The cut-off frequency is adequate, because most interfering signals have harmonics at or above 50 Hz.

The regulator's input voltage is supplied directly from the power banks (labeled Vs10000 in figure 2.2.13). The output voltage is labeled Vs3100 (3100 mV) before the RC filter, this voltage is used to supply the capacitance control digital-to-analog converters and the digital potentiometers. The device under test (DUT) is supplied with the voltage after the filter, labeled VsDUT on figure 2.2.13. The voltage regulator used in the implementation is the LM317T and the diodes are 1N4007.

The voltage values were measured at 3.25 V before the resistor and 3.2 V after the resistor. Since the total current drawn from the powerbanks is of about 230 mA, of this value, 100 mA are drawn by the microcontroller board, 80 mA by the variable capacitance circuits, and about 33 mA of current are drawn by the A/D and D/A converters of the signal path, analog circuitry and the lead-off circuit, leaving about 17 mA, of these 5 mA are drawn by the DUT and 12 mA by the capacitance control DACs and digital potentiometer.

2.5 V Regulator

A 2.5 V regulator is also needed to create a midpoint voltage, which acts as a virtual ground for some analog circuits and to the variable capacitance circuit. A LM317 based circuit, similar to the ones used to create the other supplies is used. Since 2.5 V is the double of the bandgap voltage used as reference in the voltage regulator, the resistor R2 (see figure 2.2.8 [LM317 description]), could be defined with the same value as R1 (220 Ω). The output voltage of the regulator for R1=R2 is given by:

$$V_o = V_{ref} \left(1 + \frac{R_2}{R_1} \right) + I_{adj} R_2 = 1.25 \times 2 + 50 \times 10^{-6} \times 220 \approx 2.511\text{ V}$$

This voltage value is very close to the midpoint that is about 2.5 V. The circuit's schematic is shown on figure 2.2.14.

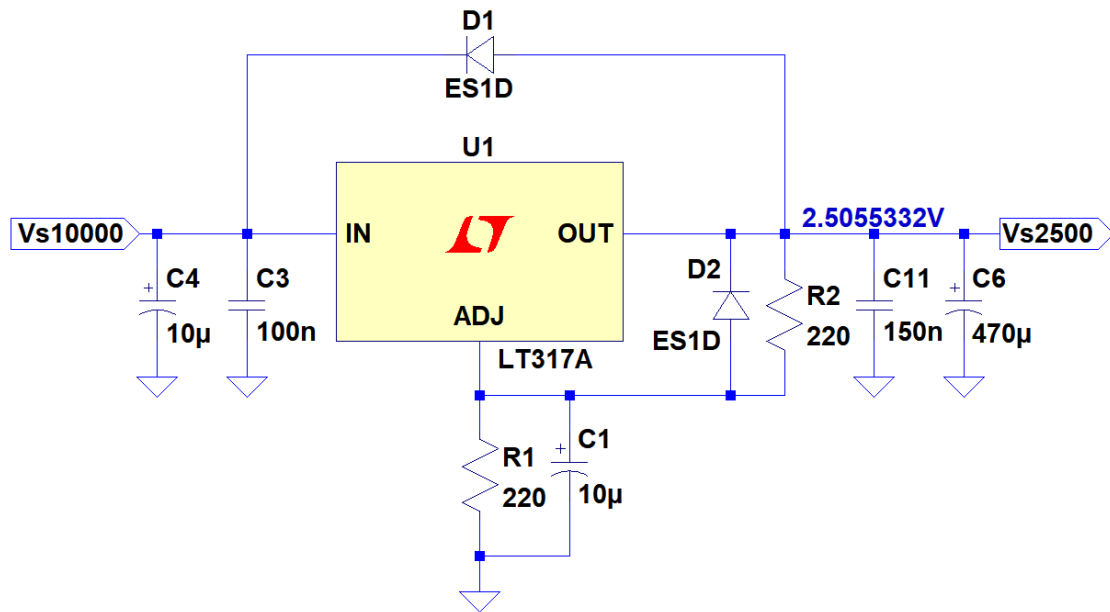


Figure 2.2.14. Midpoint voltage regulator circuit schematic

As in the other regulators, the integrated circuit used is the LM317T and the diodes are 1N4007. The measured voltage at the output is of about 2.6 V due to component tolerances, and the estimated supplied current is of less than 5 mA.

2.2.6 Digital-to-Analog Converter

The digital-to-analog converter used to generate the ECG signal (common-mode and differential components), from samples supplied by the microcontroller is the DAC8552, manufactured by Texas Instruments Incorporated. It is a 16-bit, dual channel DAC with SPI compatible interface. The main features that made this device the choice for this project, apart from its resolution and interface, were the low supply voltage operation, suitable for 3 to 5 V power supplies and the fact that it possesses a reference voltage input (that could also be set in the range of 3 to 5 V, but should never exceed the power supply voltage, V_{DD}). The block diagram of the DAC is presented in figure 2.2.15.

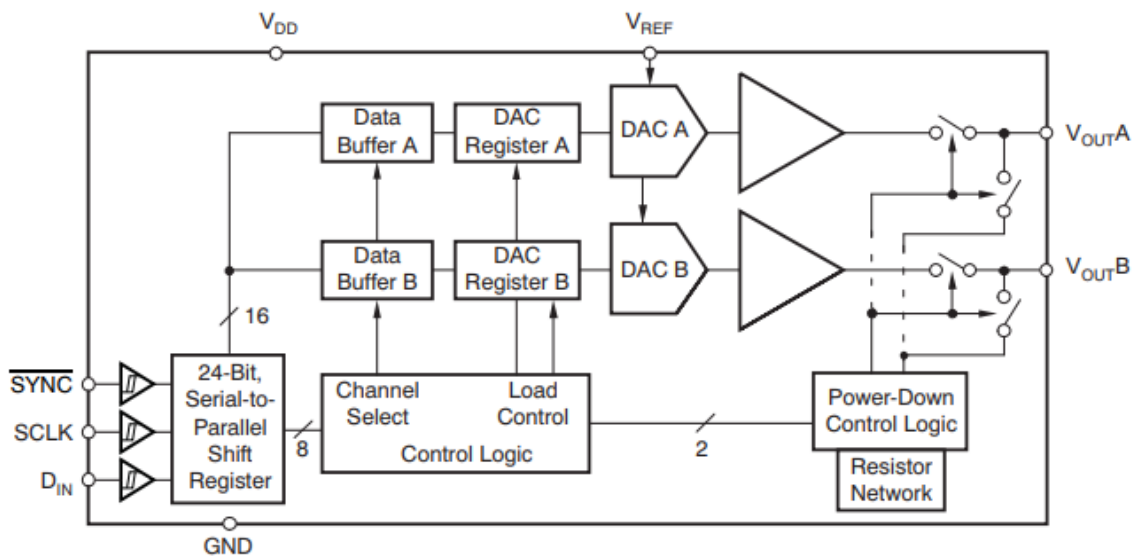


Figure 2.2.15. DAC8552 block diagram [29]

The principle of operation of the DAC8552 is relatively simple, it has three Schmitt trigger circuits that accept the signals from an SPI master device (in this case, the microcontroller), and supply the comparison results to a serial-to parallel 24 bit shift register. The shift register has an eight bit bus (control byte of the 24 bit input word) connected to the control circuit that determines and controls the selected channel, the load signals of the DAC registers, the power-down logic and output resistor network. The shift register also features a 16 bit bus (data word of the 24 bit input word) connected to the data buffers of both channels. The data buffers are connected to the DAC registers, to allow simultaneous load of both DAC channels (A and B). The resistor string DAC (figure 2.2.16) has digital switches controlled by the register values, it performs the conversion of the 16 bit word to a voltage value between 0 and $V_{REF}/2$, by selecting the desired resistor divider output.

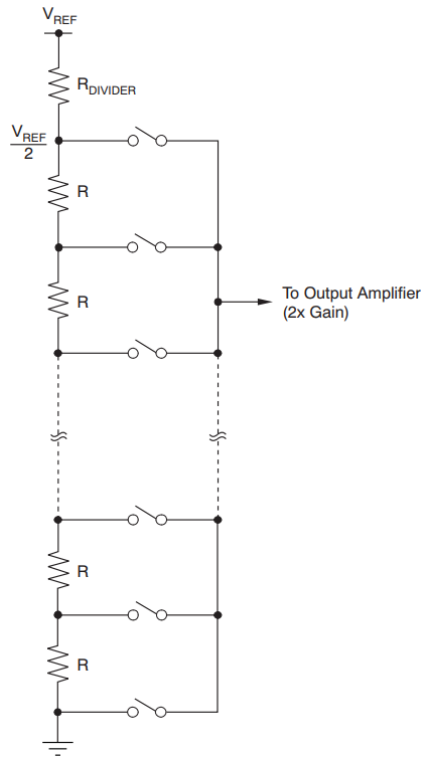


Figure 2.2.16. DAC8552 resistor string [29]

The voltage coming from the resistor string is amplified by a factor of two (voltage amplification), and the output of the amplifier corresponds to the voltage output of the DAC (see figure 2.2.17). This voltage value is given by the following expression, considering $V_{REF} = 4.5\text{ V}$ (resistor string reference voltage) and $V_{DD} = 4.7\text{ V}$ (all DAC circuits except the resistor string):

$$V_{out} = \frac{D}{2^n} \times V_{REF} = \frac{D}{65536} \times 4.5\text{ [V]}$$

In the expression D corresponds to the 16 bit data word (integer value between 0 and 65535), present in the 24 bit word sent to the DAC by the master device, n is the DAC resolution in bits.

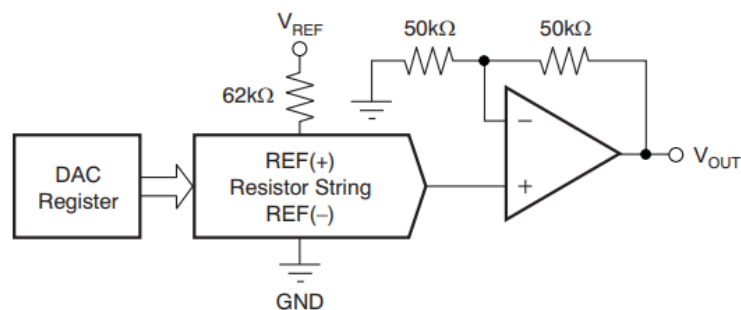


Figure 2.2.17. DAC8552 architecture [29]

SPI Interface Operation

The Serial Peripheral Interface (SPI) is a serial protocol of communication, developed by Motorola Incorporated (now part of Google LLC), which allows communication between a master device (like a microcontroller), and one or more slave devices. It generally comprises a three or four wire connection, depending on the directions of communication, master to slave, slave to master or both. One of the wires is the chip select ($\overline{\text{nCS}}$), an active low signal generated by the master device, which indicates to the slave device that it is the selected device. Another wire is the clock (also called CLK or SCLK), a periodic square wave signal generated by the master device, which defines the communication rate in bits per second (bps), typically, the frequency of this signal is of 1 MHz or more (the DAC8552 can operate at frequencies up to 30 MHz). The other two wires are the master input slave output (MISO) and master output slave input (MOSI), these wires carry the data by generating a digital low or high signal synchronized with the master clock. The data transfer must be completed before the chip select goes high (meaning the slave device is unselected). More about the SPI interface is discussed further in the System's Mode of Operation section in sub-chapter Microcontroller Communication Interfaces and Protocols.

The DAC features chip select, clock and MOSI connections, it does not have the necessity to transmit information to the master device (microcontroller). The timing diagram showing signal synchronization is presented in figure 2.2.18.

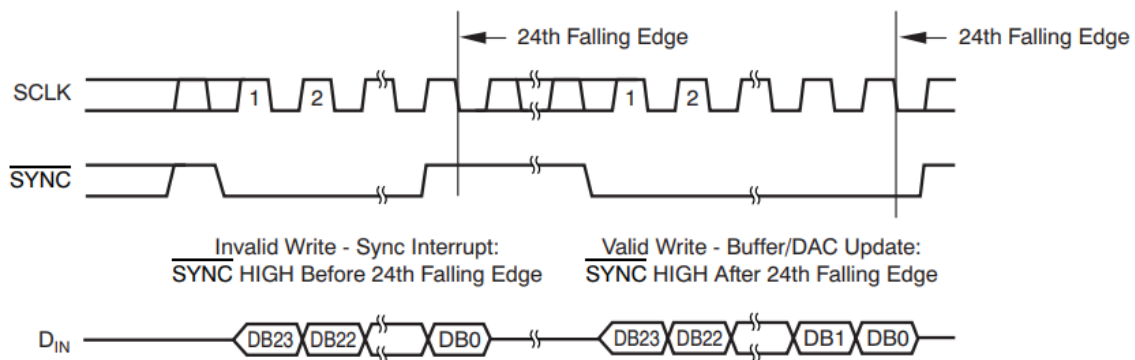


Figure 2.2.18. DAC8552 SPI interface timing diagram [29]

Data must be sent periodically to the DAC registers, via SPI interface, with data bits synchronized with the clock rising edge. The control words must be sent at the desired sampling rate. The words sent to the DAC have 16 bits of data (the signal sample) and 8 control bits. Figure 2.2.18, shows the order the bits must be sent, most significant bit (MSB) first. The data input register format, in other words, the format of the sent word, containing the functions of the control bits is shown in figure 2.2.19.

DB23											DB12	
0	0	LDB	LDA	X	Buffer Select	PD1	PD0	D15	D14	D13	D12	
DB11											DB0	
D11	D10	D9	D8	D7	D6	D5	D5	D3	D2	D1	D0	

Figure 2.2.19. DAC8552 Data Input Register Format [29]

The two most significant bits must be logic zeros (low digital voltage level), the LDB and LDA bits are active high bits, that control data loading from the data buffer to the selected DAC(s) register(s), if the device is not in power down mode, after the word is sent (the 24 bits), and the chip select returns to high level, the output(s) voltage(s) of the selected DAC(s) will change according to the value of the data values loaded in the corresponding buffer (buffer A only loads DAC register A, the same applies to buffer and register B). The bit DB19 is a don't care bit and does not affect the operation of the device, Buffer Select is a bit that defines the destination buffer for the loaded data (bits D15 to D0) or the power down command destination. PD1 and PD0 are the power control bits, for normal operation must be set to zero, there are also, three power down configurations (different output impedance values).

For reliable operation, both SPI devices (master and slave) must have the same logic level 3.3 V or 5 V, in this case the AT91SAM3X8E has 3.3 V logic and the DAC8552 has 5 V logic. Since a MISO connection is absent, there is no data from the DAC being sent to the microcontroller, the problem of overvoltage at the input of the microcontroller is avoided. The DAC8552, detects signals below 0.8 V as digital low and above 2.4 V as digital high, this means that if the devices share the same ground (circuit common), the circuit could be interfaced with 3.3 V drivers from the microcontroller. The magnitude of the input current at the DAC8552 digital pins has a maximum magnitude value of about 1 μ A, which is a very low current, but, in order to provide additional protection to the microcontroller drivers and lower spikes, 100 Ω resistors are connected in series with the digital inputs of the DAC.

2.2.7 Fully Differential Amplifier

A fully differential amplifier is necessary to convert the single ended signals from the DAC into a differential signal. The device of choice is the Texas Instruments Incorporated, THS4521, a fully differential operational amplifier, with negative rail input and rail-to-rail output. The most important features of this device are single power supply operation capability (the device operates with voltages from 2.5 V to 5.5 V), low input noise ($4.6 \text{ nV}/\sqrt{\text{Hz}}$), common-mode voltage input (with low offset), high common-mode rejection ratio (102 dB) and high power supply rejection ratio (100 dB). Other desirable features the device possesses are high bandwidth (145 MHz at unity gain), high slew rate (490 V/ μ s), high open loop gain (119 dB in DC) and low current consumption (1.14 mA typical). The block diagram of the fully differential operational amplifier is shown in figure 2.2.20.

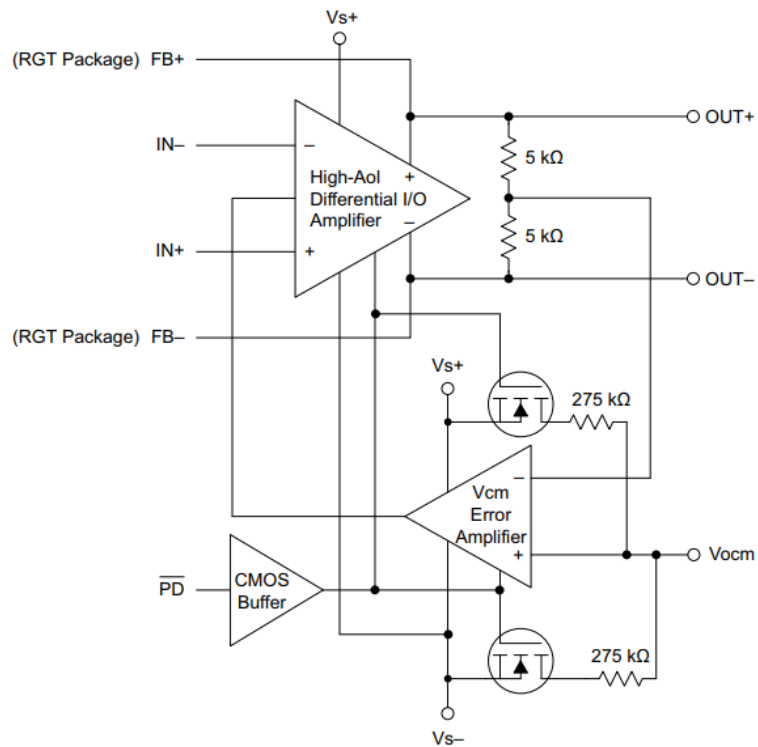


Figure 2.2.20. THS4521 block diagram [30]

The implemented circuit which performs the conversion of the single-ended common-mode and differential signal components, from the DACs into a differential signal is presented in figure 2.2.21.

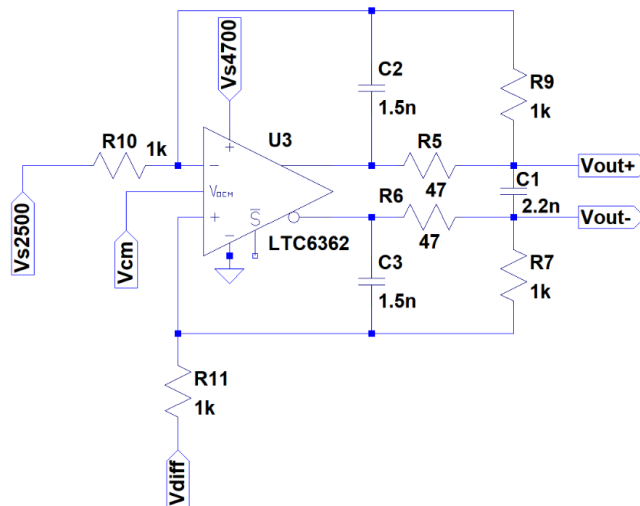


Figure 2.2.21: Schematic of the single ended to differential conversion circuit

One of the most desirable features of a fully differential amplifier is the ability to define a differential signal by setting its common-mode and differential mode components. Like other operational amplifiers, the fully differential amplifiers have a differential input. This input defines the differential component of the signal, for example, if non-inverting operation is desired, the differential component (a signal produced by a single ended DAC, containing the ECG trace, with possible addition of an interfering sinewave signal, centered in the midpoint voltage, V_{s2500} , signal labeled V_{diff} in figure 2.2.21) of the signal is added to the non-inverting input of the amplifier through an input resistor (labeled R11 in figure 2.2.21). The inverting input is connected through an input resistor (labeled R10 in figure 2.2.21) to the midpoint voltage or to ground, in this case, the midpoint voltage (V_{s2500}) is connected to this point. An additional input allows the common-mode component of the signal (a signal from a single ended DAC, containing common-mode interference and adjustable DC offset) to be added directly to the output signal. Without a common-mode input, the signal would have to be added, using a non-inverting summing amplifier, to the differential signal and to the midpoint voltage before the differential input resistors (R10 and R11).

The circuit of figure 2.2.21 has unity gain, the voltage gain is set by resistors R7, R9, R10 and R11, assuming $R7=R9=R_f$ and $R10=R11=R_{in}$ the differential voltage at the output of the amplifier (assuming an ideal opamp) is given by the following expression:

$$V_{outDiff} = V_{out}^+ - V_{out}^- = (V_{diff} - V_{s2500}) \frac{R_f}{R_{in}} = V_{diff} - V_{s2500} [V]$$

The common mode voltage present in both amplifier outputs equals the voltage labeled V_{cm} , the voltage at the V_{OCM} input. A simplified schematic of a fully differential amplifier is shown in figure 2.2.22 to better understand its architecture.

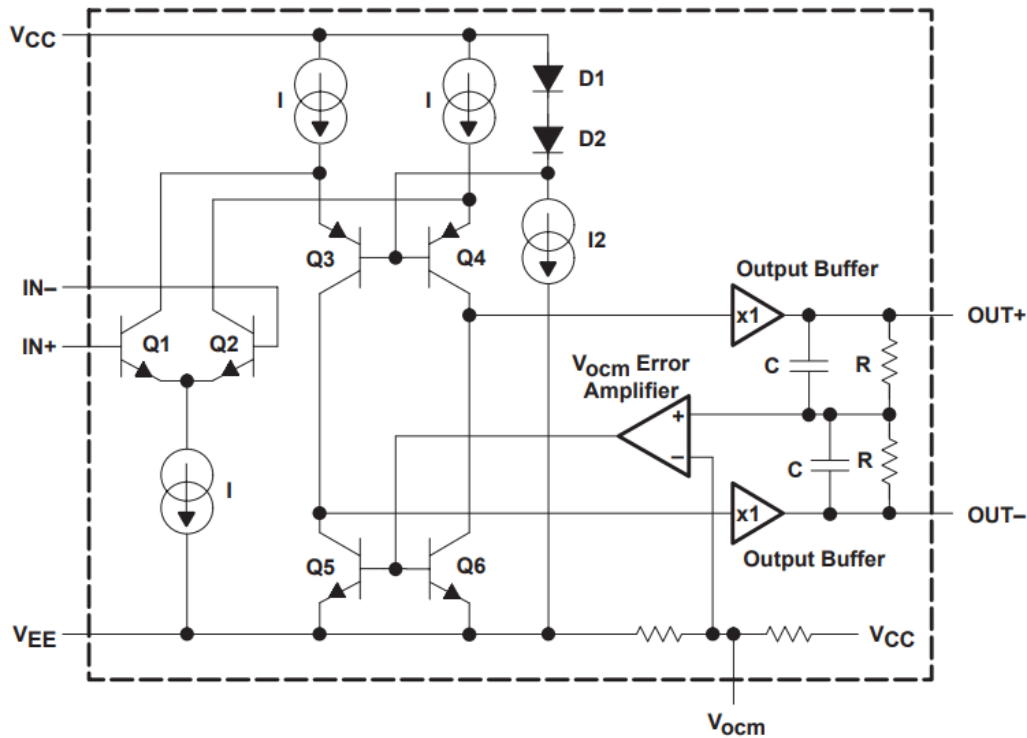


Figure 2.2.22. Fully-differential amplifier simplified schematic [31]

As can be noticed in figure 2.2.22, two amplifiers are incorporated in the design, a fully-differential amplifier (comprising a folded cascode transconductance amplifier, formed by three current sources, labeled I, bipolar transistors Q1, Q2, Q3, Q4 and Q6, a cascode biasing circuit, composed by D1, D2 and I2, and two output buffers) and a common-mode single-ended amplifier that controls the common-mode component in the fully-differential amplifier's output (labeled V_{OCM} Error Amplifier). Generally the main amplifier (fully-differential amplifier) is a more sophisticated and better performing amplifier and the common-mode amplifier is a less capable amplifier, usually this last amplifier has unity voltage gain.

In the case of the THS4521 the common-mode amplifier has a good performance, with a bandwidth of 23 MHz and 55 V/ μ s of slew-rate and unity gain, the only poor performance parameters are the low input resistance (typical value of 46 k Ω when supplied with 5 V) and the relatively high input current with a magnitude of up to 25 μ A (when supplied with 5 V). These poor performance parameters do not constitute a problem in this application, because the DAC output has the ability to drive resistances of about 2 k Ω and its short circuit current (when operated with a supply of 5 V) is typically 50 mA.

Other elements are presented in the circuit (of figure 2.2.21), like for example the capacitors, C1, C2 and C3 and the resistors R5 and R6. The elements, C2 and R5 and C3 and R6, form a type of low-pass filter at both outputs, which is added to improve the stability, by a method called in-the-loop compensation [32]. In this frequency compensation method the loop gain at high frequencies is decreased to increase the phase margin. A pole splitting technique is used, a first pole occurs before the zero introduced by the RC network, this zero minimizes the pole phase shift, so the loop gain crosses 0 dB with a more limited phase shift. The second pole is pushed towards higher frequencies. The zero is introduced by the RC network at the frequency given by the expression (assuming $C2 = C3 = C_{IL}$ and $R5 = R6 = R_{IL}$):

$$f_{zero} = \frac{1}{2\pi R_{IL} C_{IL}} = \frac{1}{2\pi \times 47 \times 1.5 \times 10^{-9}} \approx 2.2575 \text{ MHz}$$

The resistors R5 and R6 and the capacitor C1 form a low-pass filter, designed to minimize high frequency interference at the output of the amplifier. The following expression gives the cut-off frequency (half-power) of this filter:

$$f_{c(-3 \text{ dB})} = \frac{1}{2\pi(R_5 + R_6)C_1} = \frac{1}{2\pi \times (47 + 47) \times 2.2 \times 10^{-9}} \approx 769.6080 \text{ kHz}$$

The amplifier shown in the schematic (of figure 2.2.21) is of a different manufacturer and model due to the absence of the chosen operational amplifier in the software libraries, however its performance for the purposes of the application is similar to the performance of the THS4521, which is incorporated in the circuit. The differential amplifier circuit is supplied by the filtered voltage output of the 5 V regulator, labeled Vs4700 (from 4700 mV).

2.2.8 Signal Attenuator

Biopotential signals, specifically the ECG has peak-to-peak amplitude voltages in the order of the millivolt [2]. A signal attenuator is necessary to provide the low amplitude signals, required at the input of the ECG front-end. A resistive divider, followed by a voltage buffer is used to implement the signal attenuator, the circuit is illustrated in figure 2.2.23, power supply decoupling capacitors were omitted for simplification.

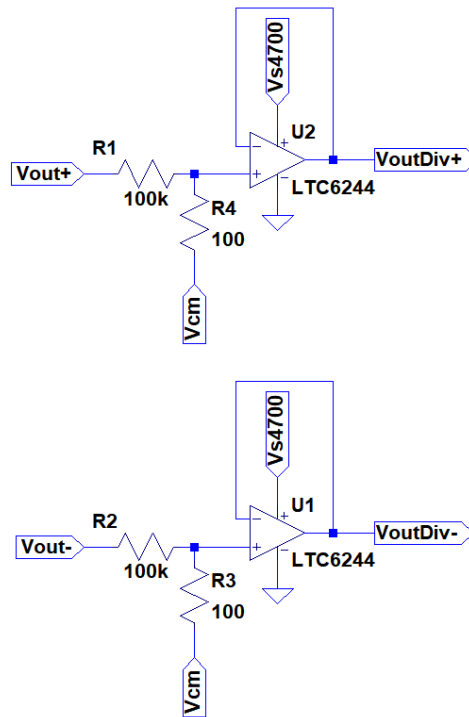


Figure 2.2.23. Signal Attenuator Schematic

The circuit is very simple to analyze and implement, two resistive dividers are incorporated after both outputs of the differential amplifier, and a voltage follower is added to provide a low impedance output. This voltage divider, however, has a particularity, due to the fact that the attenuation of the differential component of the signal is desired, but not the attenuation of the common mode signal, this component must remain unchanged, so the “tail” of the voltage divider is connected to the common mode signal output of the D/A converter, instead of being connected to the power supply midpoint value (usually the ground or half supply voltage), like is usual.

The opamp integrated circuit used to implement the buffers is the OPA2350 (that contains two opamps per package). The reason for using another opamp in the schematic is the absence of models for the OPA2350 in LTSpice library. The integrated circuit is supplied by the filtered output of the 5 V regulator (Vs4700).

2.2.9 Lead-Off Circuit

An important and innovative technique this system features is the ability to perform lead-off (temporarily disconnected or misplaced electrode) tests in one or both electrodes. By analysis of the output signal recorded, the lead-off recovery time can be calculated, giving an idea of the lead-off recovery performance of the tested device.

To perform a lead-off test, the patient simulator (the implemented system) must be electrically disconnected from the DUT, for a determined amount of time (usually a few seconds), and then reconnected. There are at least two low complexity solutions to implement this circuit, by means of a digitally controlled analog relay, or by using a digital switch. The last solution was adopted in the project, because it produces excellent results, and its cost and complexity is much lower when compared with analog relays. These relays, however, perform better in terms of open and closed circuit impedance, having the drawback of larger opening and closing times (that are still small enough to perform lead-off tests).

The integrated circuit used to act as a digital switch is the STMicroelectronics, HCF4066B, that features four digitally controllable (active high) bidirectional switches. The simplified schematic of a digital switch is represented in figure 2.2.24.

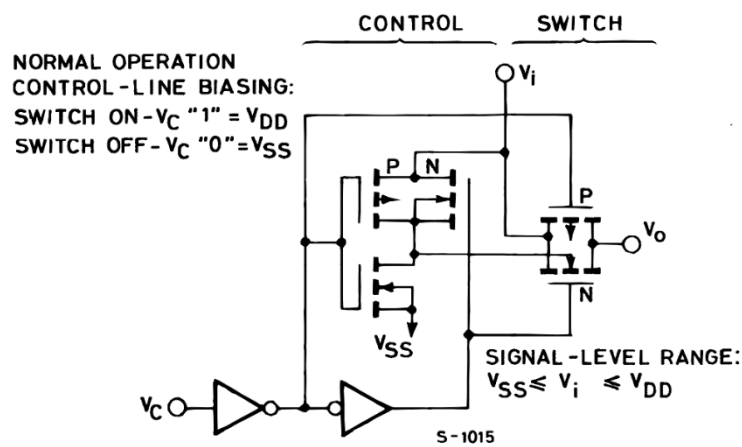


Figure 2.2.24. HCF4066B simplified schematic [33]

This bidirectional digital switch has many desirable features, it could be supplied with voltages ranging from 3 to 20 V, has a high on/off voltage ratio (of 65 dB, which corresponds to a voltage attenuation of about 1778 times), it has a high degree of linearity (low distortion of the signals that flow through the switch), a low switch off leakage current of 10 pA (typical value at ambient temperature).

The switches are digitally controlled by the microcontroller that opens and closes the switches at times specified in the test file.

The voltage supply of the HCF4066 is of 4.7 V (filtered output from 5 V regulator), the high level voltage of the digital switches is about 70 % of the supply value, being in this case of about 3.29 V (very close to the high logic level of the Arduino digital outputs). Since the switches must fail to open, the circuit was tested and it exhibited the expected behavior, with the digital switch opening and closing in 100 % of the times the circuit was tested.

2.2.10 Analog-to-Digital Converter

To convert the analog signal from the ECG front-end to the digital domain, in order to be recorded in the memory card by the microcontroller, an analog-to-digital converter (ADC) has to be incorporated in the system. The device elected is the ADS8339 from Texas Instruments Incorporated. A 16 bit successive-approximation register (SAR) analog-to-digital converter (ADC), with SPI compatible interface. The main features that made it the device of choice was, the low voltage supply capabilities (the device could be operated with voltages between 4.5 and 5.5 for the analog section, 2.25 V to 5.5 V, for the ADC reference input and from 2.375 V to 5.5 V for the digital section, all voltages must not exceed the analog supply voltage), the separated analog, digital and reference supply inputs are also a plus, because a cleaner voltage supply can be used for the reference input, and the analog and digital supplies can be separated in order to reduce digital switching interference. This device also has very good performance, with very high SNR (93.6 dB at 10 kHz), low distortion (-106 dB at 10 kHz), low INL (2 LSB) and DNL (1 LSB), an internal clock for data conversion and a maximum sample of 250 kSPS. The block diagram of the device is shown in figure 2.2.25.

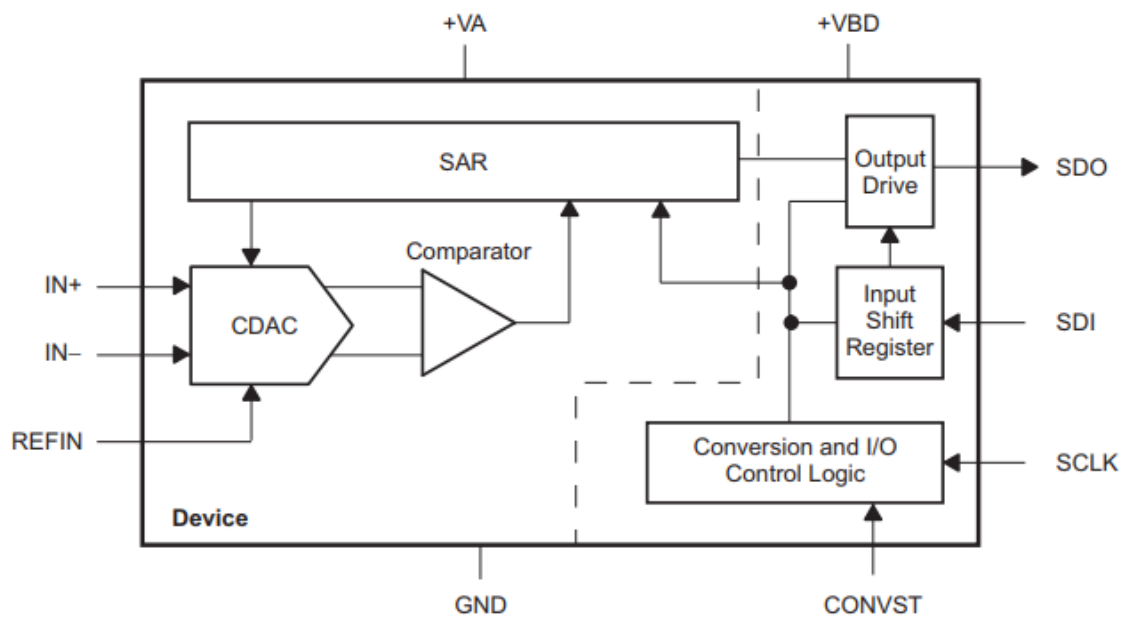


Figure 2.2.25. Block diagram of the ADS8339 SAR analog-to-digital converter [34]

The ADS8339 features a typical successive approximation ADC architecture. The voltage value of the signal present at the pseudo-differential input is sampled inside the CDAC block by a sample and hold (S/H) circuit, whose simplified circuit is shown in figure 2.2.26.

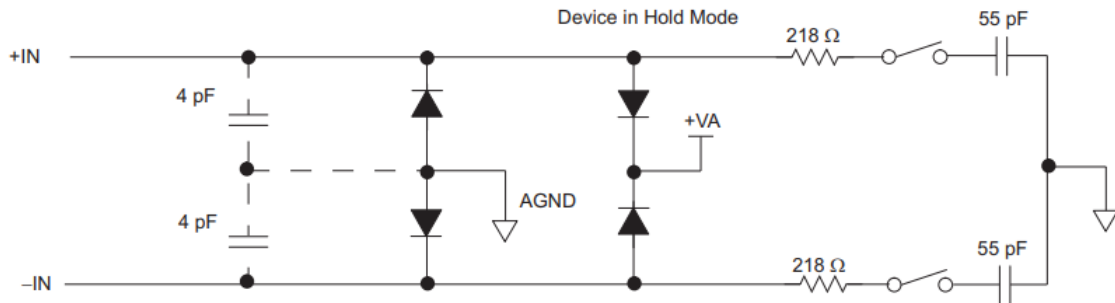


Figure 2.2.26. Simplified schematic of the sample and hold circuit incorporated in the ADS8339 ADC [34]

A sample and hold circuit relies on a digital switch and a sampling capacitor. When the device is in hold mode, the switch is in the open position and the capacitor voltage is applied to a comparator. In sample mode the switch is closed and the voltage from the input(s) is/are sampled by the capacitor(s). Some of the other components present in figure 2.2.26 are protection components, the diodes impose a limit to the maximum and minimum voltages present at the input.

The CDAC of the block diagram (of figure 2.2.25) may also contain a differential amplifier (unity gain difference amplifier), to convert the input voltage to a single-ended voltage, and a DAC. The voltages from the DAC and from the capacitors (possibly after being underwent a single-ended conversion by a differential amplifier), are applied to a comparator, that generates a flag which indicates to the successive-approximation register (SAR) if the voltage representation of its digital value is under or above the sampled voltage.

Generally, the SAR starts with the digital midpoint value, and accordingly to the comparison results, decreases and increases its digital value successively at the defined SAR (internal) clock rate, until the best approximation is obtained, when this happens the result is retained, and transmitted by the digital serial interface, when the master device (microcontroller) is ready to receive data. After the data is received by the SPI master device, the process repeats, the master device must request data at the desired sample rate. The ADC input signal is sampled while the data is being sent to the SPI master, held and converted during the intervals.

SPI Interface Operation

The ADS8339 features a four wire serial peripheral interface, that could also be configured as a three wire interface (for more information refer to the System's Mode Operation SPI section, to the SPI Interface Operation sub-section of the DAC section and to the ADC datasheet [34]). The connection scheme is represented in figure 2.2.27.

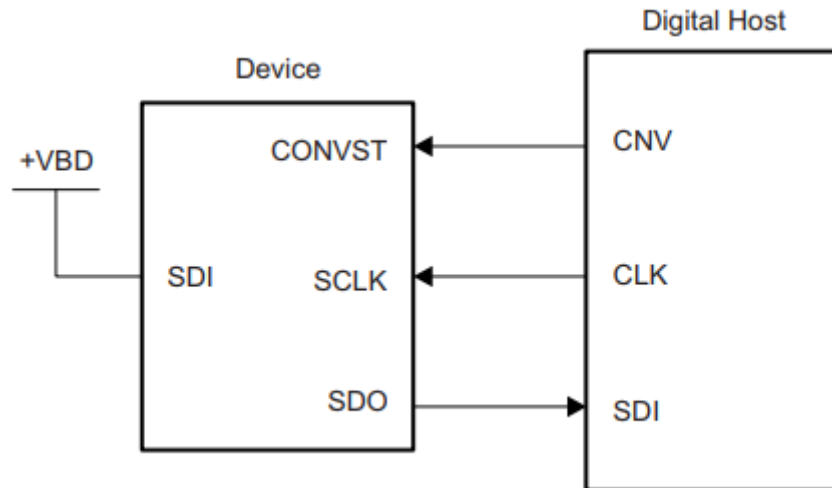


Figure 2.2.27. Connection diagram for three wire SPI operation [34]

In figure 2.2.27, the block labeled Device is the ADS8339 and the block labeled Digital Host is the microcontroller. The signal generated by the master device at the CNV output, connected to the CONVST input has the same function to the SPI interface as the nCS, the active low chip select. The signal that goes from the CLK master output to the SCLK slave input is the SPI clock signal generated by the SPI master (microcontroller), the ADS8339 supports clock frequencies up to 25 MHz. The signal generated by the slave device, SDO output, enters the SDI input of the master device, having the same function as the MISO (master input slave output) data connection, this connection is used to transmit the conversion results from the ADC to the microcontroller. The ADC's SDI input, corresponds to the MOSI (master output slave input) data connection, it is not used and must be tied to the digital supply voltage (in the circuit implementation this value is of about 3.25 V to match the microcontroller high digital level) for 3-wire SPI operation [34].

To ensure reliable operation the SPI protocol conditions must be met, figure 2.2.28, shows the timing diagram of the ADS8339.

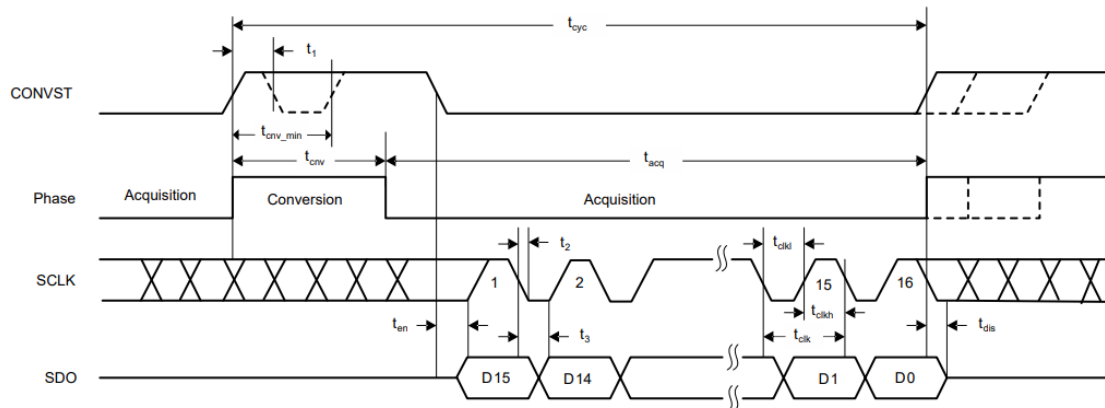


Figure 2.2.28. 3-wire SPI mode timing diagram of the ADS8339 [34]

In 3-wire mode of operation, the master SPI device (the microcontroller) requests a sample from the ADC by setting the CONVST (nCS) signal to the low logic level. Then in the next cycle of the clock, in its rising edge, the first data bit is sent to the SDO (MISO), the bits are sent by the ADC in the rising edge and are received in the falling edge by the microcontroller, the process repeats until the last bit is received (16th bit). After receiving the last bit of the ADC sample, the CONVST signal (nCS) generated by the microcontroller must return to the high logic level. The described process repeats periodically (at a frequency corresponding to the desired sampling rate) while the microcontroller is in acquisition (recording) mode.

ADC Circuit

The input of the ADC is driven by an opamp, OPA2350, in the non-inverting voltage follower configuration, with an input resistance of about 10 k Ω . This opamp is incorporated to drive the antialiasing filter (capacitive load), present at the input of the ADC. Driving the antialiasing filter directly with the DUT (ECG front-end), could cause instabilities (oscillations) on its output, due to the large reactive component of the load. The driver circuit of the ADC input is presented in figure 2.2.29.

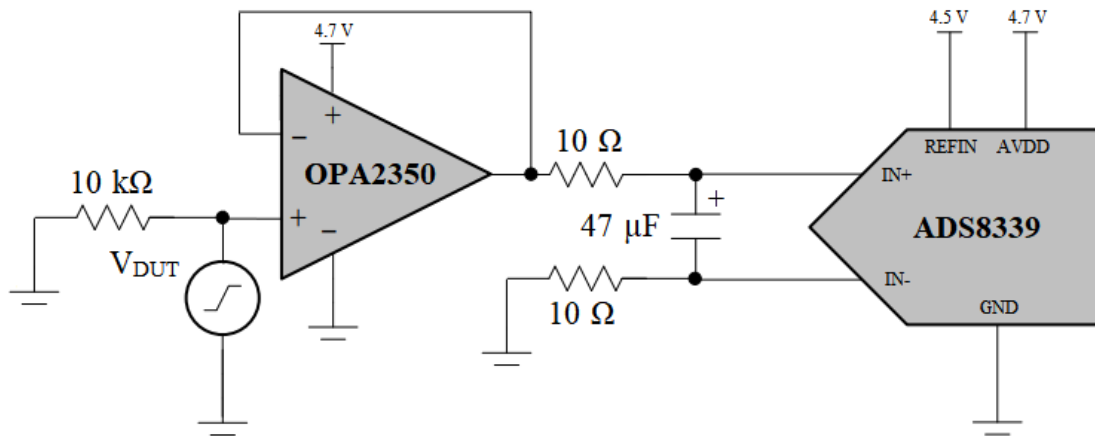


Figure 2.2.29. Schematic of the ADC input driver circuit [adapted from 34]

The antialiasing filter is formed by the 10 Ω resistors and the 47 μF aluminum electrolytic capacitor. The low-pass antialiasing filter cut-off frequency (-3 dB) is given by the following expression:

$$f_{c(-3 \text{ dB})} = \frac{1}{2\pi RC} = \frac{1}{2\pi \times (10 + 10) \times 47 \times 10^{-6}} \approx 169.3138 \text{ Hz}$$

A frequency of approximately 169 Hz is adequate for the antialiasing filter. Ideally the cut-off frequency of this low pass-filter must be set to the value defined by Shannon-Nyquist sampling theorem, which in this case is half of the sample rate (between 250 and 1000 Hz). But, since the filter incorporated is of first order, it has a frequency decrease rate of 6 dB/octave, so a much lower frequency must be set, a frequency between 150 and 200 Hz is adequate, because it has relatively low effect (attenuation of 1 dB or less) in the band of interest of the ECG signal which lies between 0.05 Hz and 100 Hz [2].

2.2.11 ECG Front-End

The ECG front-end corresponds to the device under test (DUT), it is not a part of the test platform, but it is an essential component as it is the reason for its existence. There is a large variety of ECG front-ends commercially available, some feature an analog output and others have an internal analog-to-digital converter, and a serial interface (like for example, SPI or I²C). The system is currently configured to test analog output front-ends only, though it could be modified to accept and acquire signals from digital output front-ends (that communicate with a master device via SPI or I²C), changes to the software programming and additional SPI and/or I²C connections are necessary in order to implement this feature.

The main function of the ECG front-end is biopotential acquisition and signal conditioning. The front-end provides amplification, differential to single ended conversion, filtering and in some cases lead-off detection. It must be capable of providing high quality ECG measurements using non-ideal electrodes (like dry electrodes).

In this section an analog output front-end is analyzed, the Analog Devices, AD8232. This device was the choice during the test phase of the implemented system. Other ECG-front ends will also be introduced, but more superficially, because they were not tested in this project.

Typical Front-End Architecture

The main elements of an ECG front-end architecture are presented in figure 2.2.30.

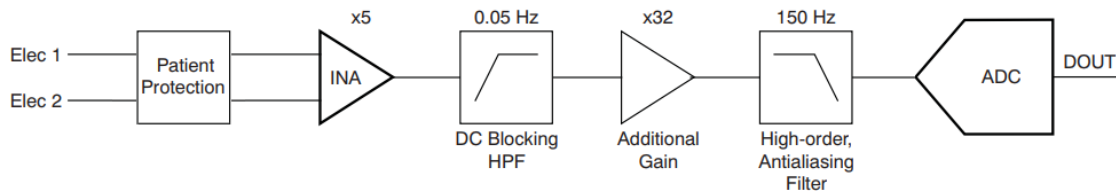


Figure 2.2.30. Schematic of the ADC input driver circuit [adapted from 35]

The biopotential is captured from the body with electrodes, the current flow through the lead wires attached to the electrodes and reaches the patient protection block, which generally comprises high value resistors or in some cases (for example, when the ECG equipment is powered from the mains), a higher degree of protection is more adequate, like optical isolation or galvanic (transformer) isolation. The next stage, labeled INA, is the instrumentation amplifier, an amplifier which provides high common-mode rejection, high input impedance, moderate to high voltage gain and differential to single-ended conversion. After the filter, an additional single-ended gain stage might be added, to increase the amplitude of the signal, this amplifier must have a low noise figure, to avoid degrading the signal-to-noise ratio.

On some front-ends the output signal after the additional amplification corresponds to the output of the system, the low-pass filtering may be performed in previous stages, for example, in the first filter stage (which could be a band-pass filter). Others might have a low-pass filter after the last gain stage to limit the upper band-pass limit to a value typically between 100 and 200 Hz (150 Hz in figure 2.2.30), this block attenuates the interfering signals, with frequency contents above its cut-off frequency, also acting as an antialiasing filter. The last block of figure 2.2.30, an analog-to-digital converter (ADC) and additional serial interface circuitry, may or may not be present in the front-end IC, for example, it is present in the MAX30001 Biopotential and bioimpedance measurement front-end manufactured by Maxim Integrated Products, that features an SPI interface, but it is not present in the AD8232 Heart Rate Monitor ECG front-end, manufactured by Analog Devices.

AD8232 Architecture

The AD8232 is the ECG front-end used in the tests, it is a single lead, heart rate monitor. It has the following features [36]:

- Instrumentation amplifier
- 2-pole adjustable high-pass filter
- Fast restore circuit to improve filter settling time
- Uncommitted opamp (that could be used as an additional gain stage)
- 3-pole adjustable low-pass filter with adjustable gain
- AC and DC lead-off detection
- Integrated reference buffer to generate virtual ground
- Rail-to-rail output
- Internal RFI filter

As can be noticed, the AD8232 has all the elements of the typical architecture of an ECG front end (see figure 2.2.30), with the exception of the analog to digital converter (ADC), and the patient protection circuitry, this front-end features an analog output and is intended for battery operation (off-grid operation). The block diagram of the AD8232 is presented in figure 2.2.31 [36].

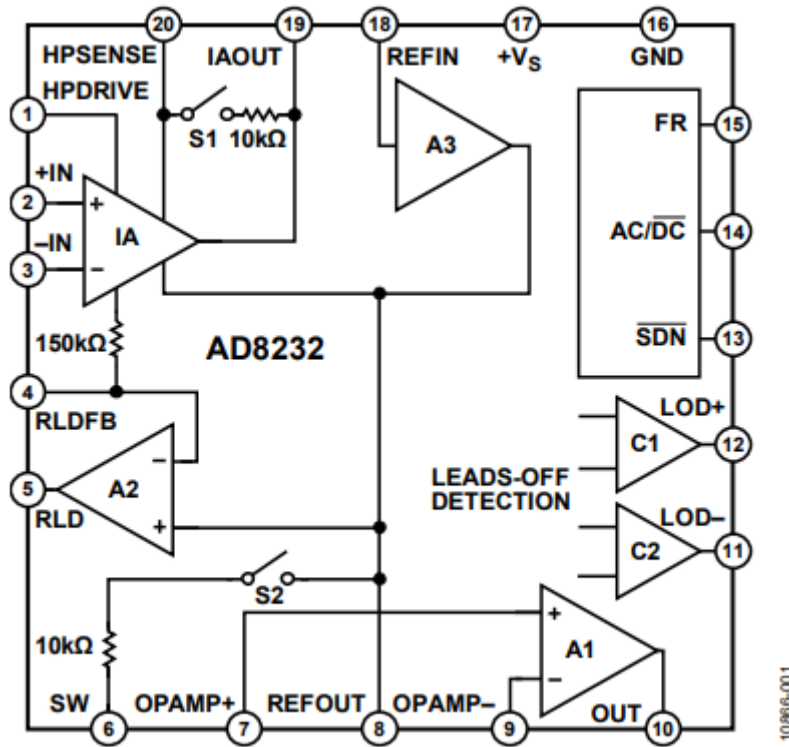


Figure 2.2.31. Block diagram of the AD8232, an analog output ECG front-end [36]

To better understand the mode of operation of the AD8232, a simplified schematic is shown in figure 2.2.32. In this schematic, the architecture of the instrumentation amplifier is shown in more detail. The instrumentation amplifier has two matched transconductance amplifiers (GM1 and GM2), a DC blocking high pass-filter (HPA) and an integrator (C1 and the unlabeled opamp). The GM1 amplifier generates a current proportional to the input signal differential voltage. When feedback is satisfied, an equal voltage will appear across the inputs of GM2, to match the current generated by GM1. The error current is integrated across C1, and the resulting voltage appears at IAOUT. The voltage feedback of the amplifier is applied to GM2, through different paths, the two gain setting resistors (which define the voltage gain to 100, labeled R and 99R), and the high-pass filter, which integrates any deviation from the reference level. An internal charge pump running at a frequency of 500 kHz, boosts the supplies of the transconductance amplifier (GM1 and GM2), to prevent saturation of the instrumentation amplifier in the presence of large common-mode signals, such as mains interference [36].

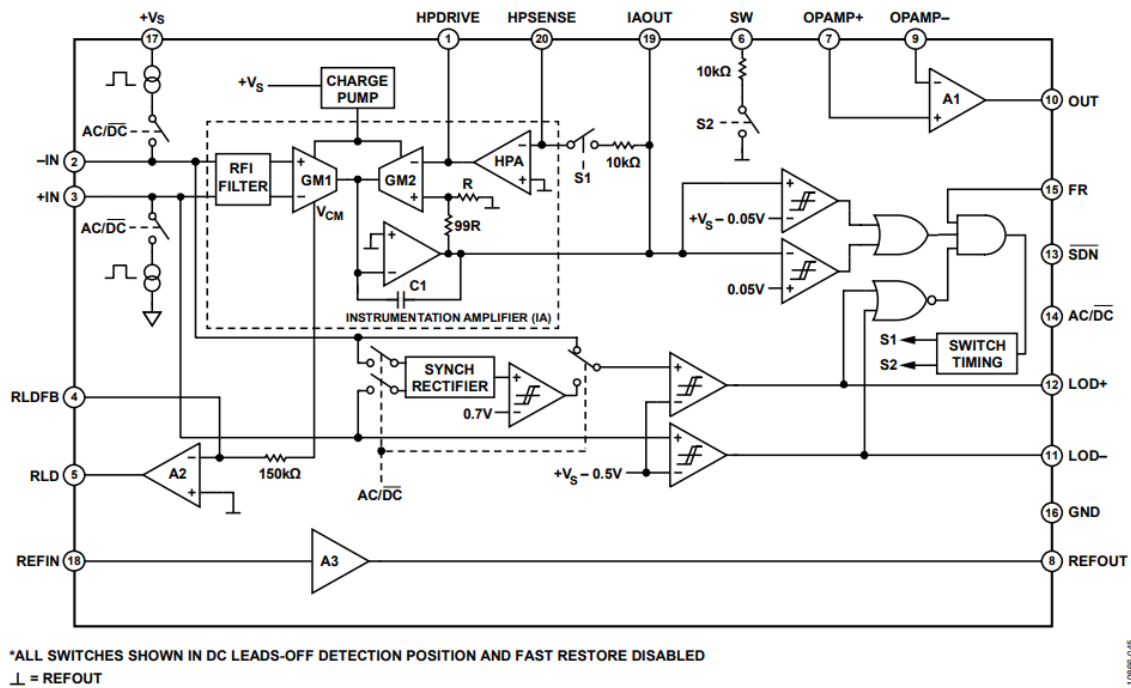


Figure 2.2.32. Simplified schematic of the AD8232 ECG Front-End [36]

AD8232 Fast Restore Circuit

A fast restore circuit is also incorporated in AD8232, its function is to quickly restore normal operation, when a very large DC component at the output of the instrumentation amplifier is detected. A large offset (positive or negative in relation to the supply midpoint) at the output of the IA is normal after electrode connection to the subject, or could signify that a temporary lead-off, electrode misconnection or motion artifact occurred. If this voltage is close to one of the supply rails by less than 50 mV, the switches (S1 and S2) are closed, quickly draining the high pass filter capacitors. If the DC component is lowered to an acceptable value, the switches open and the amplifier resumes its normal operation, otherwise the cycle repeats [36].

AD8232 Lead-Off Detection

The AD8232 features AC and DC lead-off detection, however, the second option only works in three electrode configurations. In DC lead-off detection mode, the leads must be connected to a high value pull-up resistor (usually 10 M Ω), two comparators check if the voltage is 0.5 V under the positive supply voltage, if this condition is not satisfied, the lead off signal of the corresponding input is set high. This configuration needs three electrodes, because the common-mode voltage of the subject must be close to the supply midpoint, and this is achieved by injecting a very small current into the body, using a third electrode.

The AC lead-off detection uses another method, a conduction path between the electrodes must exist, two high impedance resistors (usually 10 M Ω) from each electrode to the right leg drive output (provides better common-mode rejection) or to the reference output (constant voltage set the supply midpoint) are required (see figure 2.2.33), this connection is made to maintain the input voltage within the common-mode range of the instrumentation amplifier. The detection is performed by forcing a small 100 kHz current into the input terminals. The injected current flows through the external resistors and develops a small voltage potential at the inputs, which is synchronously detected and compared to an internal threshold. The impedance of the path formed between the two electrodes must be less than 3 M Ω . In AC lead-off detection, only the LOD+ signal indicates lead-off, LOD- remains in the low logic state, meaning the electrode that lost connection could not be identified. The AC/nDC input must be be connected to ground for DC lead-off detection and to the positive supply rail for AC lead-off detection [36].

AD8232 board

The DUT circuit board used in the project, is a clone of the PCB from Sparkfun [37]. It has, however, a few modifications, which are shown in figure 2.2.23, like for example, the AC lead-off detection configuration and the two-electrode operation modifications. For two-electrode operation, the right-leg drive output must be connected by a high impedance (in this case a 10 M Ω resistor), to each of the lead inputs to maintain the input voltage within the common-mode range of the amplifier.

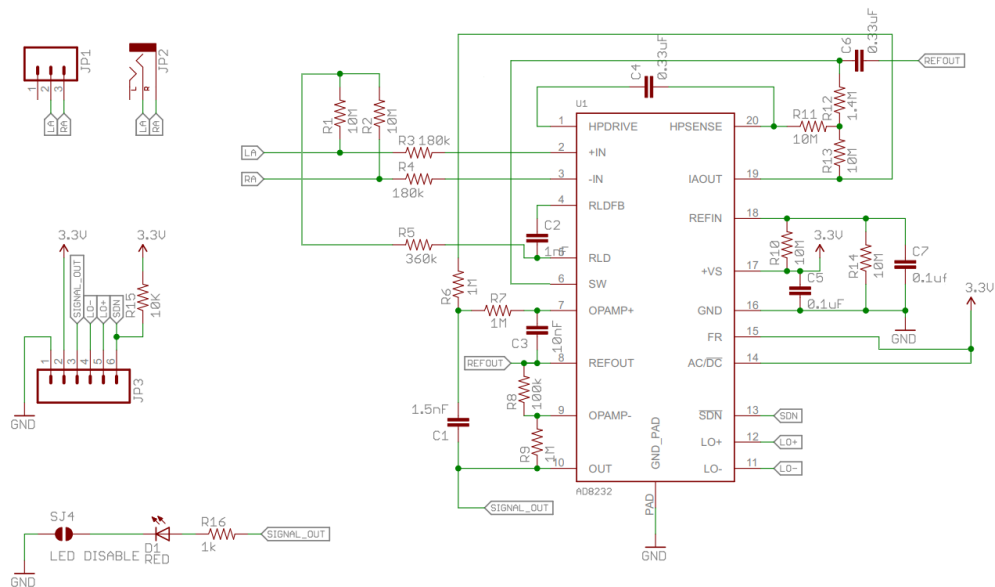


Figure 2.2.33. ECG front-end configuration schematic (printed circuit board schematic) [adapted from 37]

This circuit configuration apart from the modifications mentioned is very similar to an application circuit described in page 25 of the AD8232 datasheet [36]. It is designed for monitoring the shape of the ECG waveform. Since the filtering elements are the same as in the application circuit, the frequency response is illustrated by figure 2.2.34 [36]. The low cut-off frequency is about 0.5 Hz and the high-cut-off frequency is about 40 Hz. The gain defining elements also remain the same, the gain of the instrumentation amplifier is internally defined and is set to 100 (40 dB). The additional gain stage (implemented using the uncommitted opamp) has a voltage gain of 11, a gain of 11 in linear units corresponds to a gain of about 21 dB, giving a total voltage gain of 1100 (or about 61 dB).

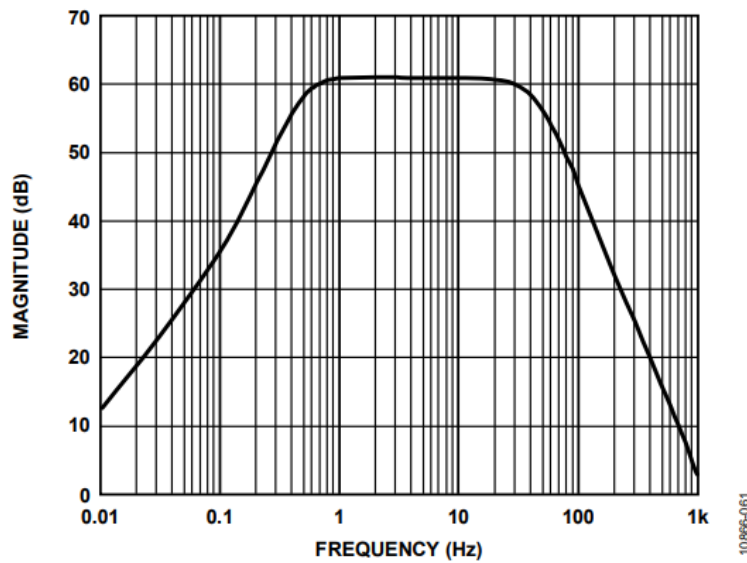


Figure 2.2.34. Frequency response of the AD8232 based circuit used as DUT [36]

The frequency response of the circuit is adequate, but for higher performance the low cut-off frequency should be about 5 to 10 times lower (a value between 0.05 Hz and 0.1 Hz), and the high cut-off frequency should be about 2.5 to 5 times higher (a value in the range of 100 Hz to 200 Hz). This front-end also lacks a mains interference notch filter (though sometimes the use of such filter is avoided because it may increase signal distortion).

Digital Output ECG Front-Ends

There are other ECG front-ends designed for portable applications, the most known are the ADS1291, manufactured by Texas Instruments Incorporated and the MAX30001, MAX30003 and MAX30004, manufactured by Maxim Integrated Products. These devices feature SPI interface and an internal analog-to-digital converter (ADC).

ADS1291

The ADS1291 is a low power, two-channel, analog front-end for biopotential measurement manufactured by Texas Instruments Incorporated. The block diagram is shown in figure 2.2.35.

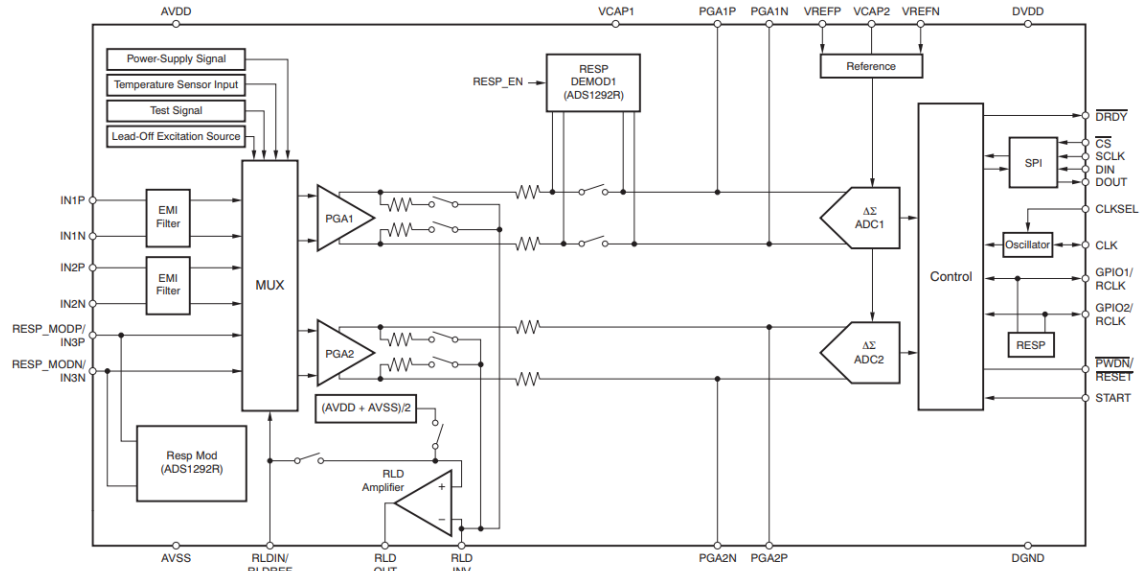


Figure 2.2.35. ADS1291, ADS1292, ADS1292R simplified block diagram [38]

The main features of this ECG front-end are [38]:

- Integrated high resolution ADCs (24 bit)
- Sample rate up to 8 kSPS
- High CMRR (105 dB)
- Low voltage supplies (2.7 to 5.25 for the analog section and 1.7 to 3.6 for the digital section)
- AC and DC lead-off detection
- SPI Compatible Interface

Unlike the AD8232, the ADS1291 does not have analog filters, and only has one (programmable) gain stage. This front-end relies on the high resolution of its sigma-delta ADC to produce an accurate ECG waveform representation.

MAX30003

The MAX30003 is an ultra-low power, single-channel integrated biopotential analog front-end, manufactured by Maxim Integrated Products Incorporated. The block diagram of this front-end is presented in figure 2.2.36.

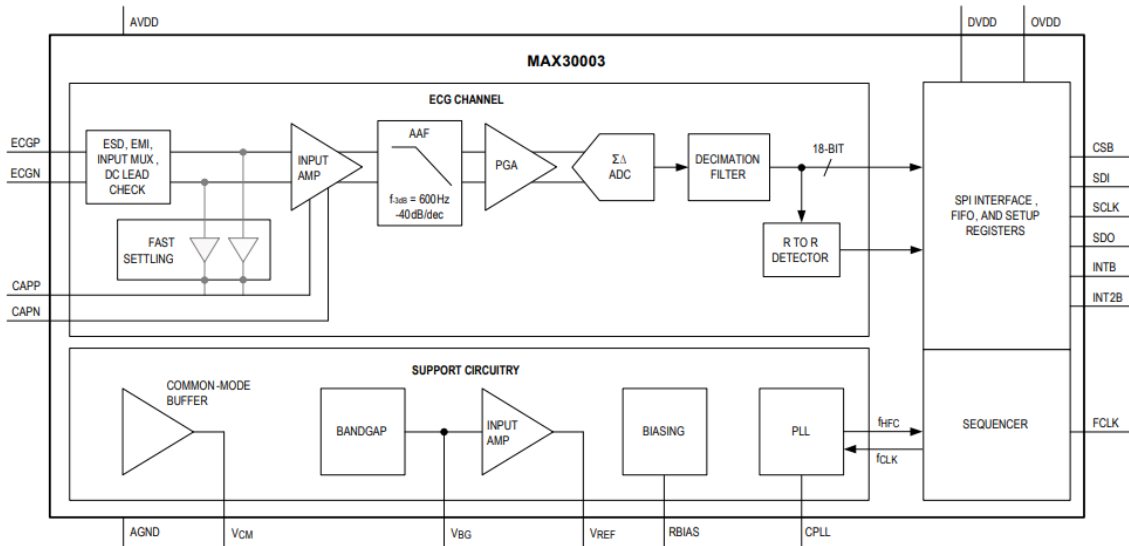


Figure 2.2.36. MAX30003 simplified block diagram [39]

The main features of this ECG acquisition integrated circuit are [39]:

- Internal high resolution (18 bit) sigma-delta analog-to-digital converter (ADC)
- 15.5 bit effective resolution with $5 \mu\text{V}_{\text{P-P}}$ noise
- CMRR greater than 100 dB
- Input Impedance greater than $500 \text{ M}\Omega$
- High-Speed SPI interface
- High-pass and low-pass filter configurations
- Fast recovery mode
- DC lead-off detection

This front-end has more voltage gain (up to 160) when compared to the ADS1291 (maximum PGA gain setting is 12). The ADC has a lower resolution (when compared to the Texas Instruments Incorporated front-end, 18 bit vs 24 bit), compensated by a higher voltage gain. The MAX30003 does not feature AC lead-off detection.

2.3 Skin-Electrode Interface Simulation

The implemented ECG test system features skin-electrode interface simulation, allowing the user to adjust the impedance components (resistive and reactive) of this interface. This innovative functionality allows the simulation of different types of electrodes. The variation of the skin-electrode impedance over time can also be simulated.

The skin-electrode interface is simulated by the system using the single time constant model [40] initially purposed by D. Swanson and J. Webster, consisting of a circuit with a resistor in parallel with a capacitor, and a second resistor in series with the other two elements. The single time constant skin-electrode impedance model is presented in figure 2.3.1, showing the range of values that can be defined in the implemented system.

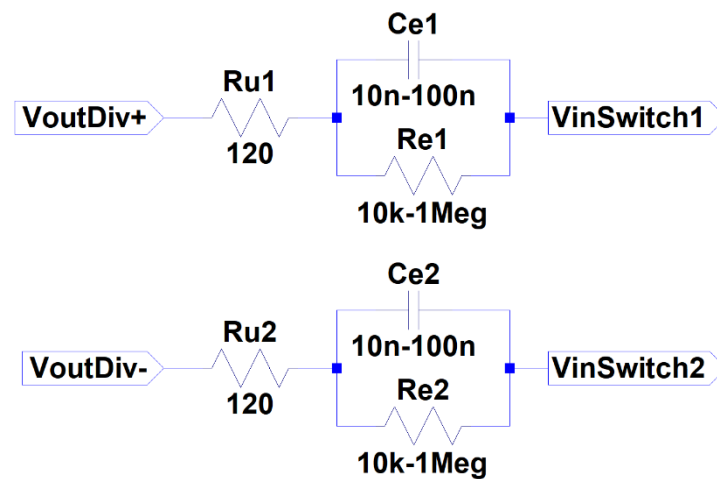


Figure 2.3.1. Single time constant skin-electrode impedance model [40]

The tissue resistance (R_{u1} and R_{u2}) is very low compared to the skin-electrode interface resistive component (R_{e1} and R_{e2}), and has little contribution to the overall impedance, it is simulated by a $120\ \Omega$ resistor (having a value close to the obtained in [41], about $117\ \Omega$). The typical values of resistors R_{e1} and R_{e2} are usually comprised between about $23\ \text{k}\Omega$ and $1\ \text{M}\Omega$ [38, 41, 42, 43 and 44] depending on the type of electrode and the type of skin of the subject.

The typical values for the capacitances, C_{e1} and C_{e2} , are usually between $10\ \text{nF}$ and $47\ \text{nF}$ [38, 41 and 44]. The system is capable of simulating skin-electrode resistance, with values ranging from $10\ \text{k}\Omega$ to $1\ \text{M}\Omega$, and skin-electrode capacitance, with values ranging from $10\ \text{nF}$ to $100\ \text{nF}$.

2.3.1 Variable Capacitance Circuit

The variable capacitance circuit is based on an innovative technique [45], which consists in differentially sampling the voltage drop across a small capacitor, and applying this voltage to an RC network (with a relatively low resistive value). The current that flows through this second capacitor (of a larger value) is sensed in the resistor and converted to a voltage. This electric potential is applied to the inputs of two operational transconductance amplifiers (OTAs), being inverted in one of them. One of the OTAs act as a current source and the other as a current sink (the current at the output of the OTAs has opposite phase). The transconductance amplifiers are connected to the first capacitor, to form a negative feedback loop, the current sink OTA is connected to the positive terminal, and the current source OTA is connected to the negative terminal. OTAs operate as AC current sources, so both OTAs are capable of sourcing and sinking current, the nomenclature used in the text is just to exemplify that the OTAs operate in phase opposition [45].

The described circuit, works as a capacitance booster, if there is sufficient transconductance gain (assuming the gain of the remaining elements of the circuit, is unity, for DC and for the desired frequencies of operation). But it does not provide a variable capacitance *per se*, fortunately, the OTAs provide a current input that can be used to control the transconductance gain. By connecting a resistor to this input, and knowing the voltage drop at the input of the transconductance amplifier, is possible to impose a known current. This current corresponds to the voltage drop in the resistor, a variable voltage source, like, a DAC output, for example, can be used to control the transconductance gain of the OTAs, and, consequently, control the capacitance value, making the implementation of a variable capacitance circuit possible [45].

LT1228

The transconductance amplifier chosen to be part of the variable capacitance circuit is the LT1228. It is a 100 MHz current feedback amplifier with DC gain control from Linear Technology Corporation, this integrated circuit features a transconductance amplifier and a current feedback amplifier. The simplified schematic of the device is presented in figure 2.3.2.

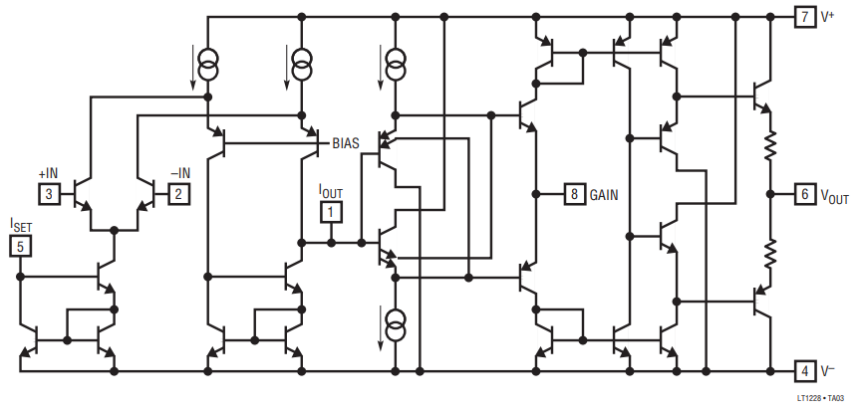


Figure 2.3.2. LT1228 simplified schematic [46]

The transconductance amplifier features current controlled gain, a bandwidth of 75 MHz, low distortion, high CMRR (100 dB typical value) and high PSRR (with a typical value of 100 dB). The integrated circuit can be supplied by a 5 V single power supply (it has a minimum recommended power supply voltage of 4 V) [46].

Circuit Schematic

The schematic showing the implementation of the voltage (current) controlled synthetic capacitance is presented in figures 2.3.3 and 2.3.4. The supply bypassing and decoupling capacitors (0.47 μ F across each integrated circuit supply terminals, and 10 μ F in parallel with 0.47 μ F at the supplies input of the integrated circuit) are omitted in figures 2.3.3 and 2.3.4.

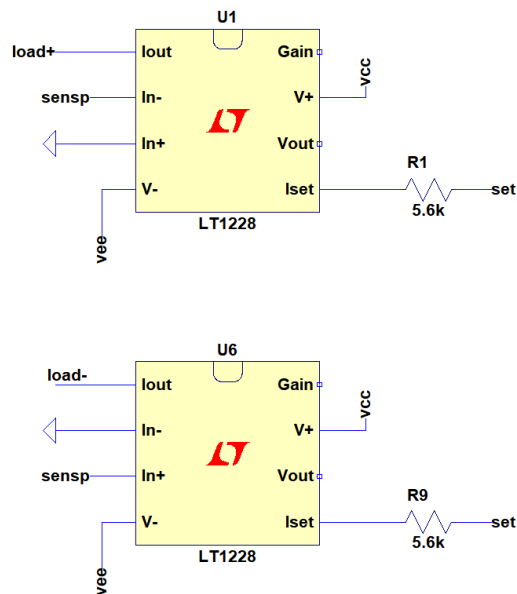


Figure 2.3.3. Schematic showing the configuration of the transconductance amplifiers [45]

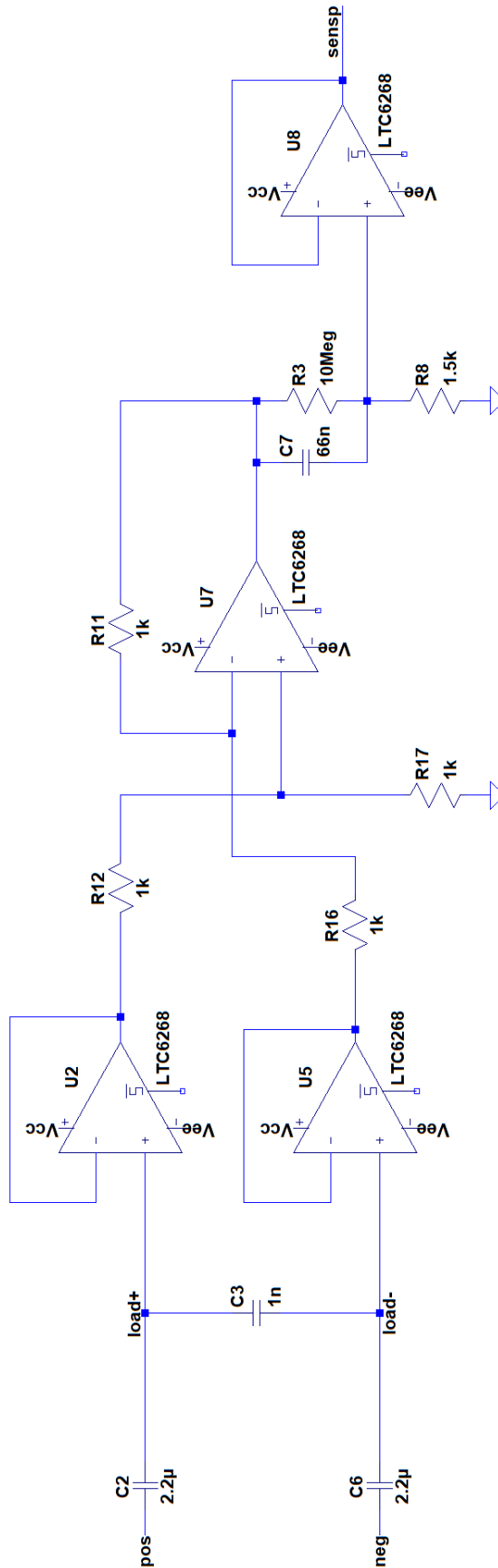


Figure 2.3.4. Schematic of the variable capacitance circuit showing the reference capacitors, the unity gain instrumentation amplifier, the sample resistor and voltage buffer [45]

The circuit presented in figure 2.3.4 features an instrumentation amplifier, composed of three individual opamps (U2, U5 and U7) and a current sensing voltage follower implemented with an opamp (U8). The voltage at the reference capacitor (C3) terminals is differentially measured by the instrumentation amplifier (opamps U2, U5, U7 and resistors R11, R12, R16 and R17), and applied to a network containing another reference capacitor (C7, R3 and R8). Resistor R3 is incorporated to provide input bias current to U8, but since the input could be polarized by R8, this resistor could be omitted. The current sensing resistor (R8), develops a voltage drop at its terminals (according to Ohm's law), this voltage is sampled by the voltage follower (U8). A buffer is required to provide a higher input resistance, which the transconductance amplifier, the LT1228 is unable provide, contributing to lower the error during the voltage measurement. The output of the buffer is connected to the inputs of the transconductance amplifiers (U1 and U6 in figure 2.3.3). It connects to the inverting input of U1 and the noninverting input of U6, in order to shift the current phase by 180 degrees (the currents must have opposite phase). The current output in phase opposition is connected to the node labeled Vload+ and the in-phase current is connected to the node labeled Vload-, forming a negative feedback loop. Resistors R1 and R9 provide the gain adjustment current (I_{set}). A DAC generates the capacitance control voltage (labeled set in figure 2.3.3).

Capacitance Variation

The equivalent load capacitance is given by the following expressions [45]:

$$C_{LOAD} \approx \left(1 + g_m R_{sens} \frac{C_{REF2}}{C_{REF1}}\right) C_{REF1} = \left(1 + g_m R_8 \frac{C_7}{C_3}\right) C_3 \approx 1 \times 10^{-9} + 99 \times 10^{-6} g_m [F]$$

$$g_m \approx 9.86 \times I_{set} [S]$$

$$I_{set} = \frac{V_{set} - 1.25}{R_{set}} = \frac{V_{set} - 1.25}{R_{1,9}} = \frac{V_{set} - 1.25}{5600} [A]$$

The components are numbered like in figures 2.3.3 and 2.3.4. $R_{1,9}$ refers to the I_{set} resistor (with a resistance of 5.6 k Ω), whose current defines the transconductance gain and consequently the capacitance value (V_{set} corresponds to the voltage generated by the control DAC, which is applied to a terminal of the gain setting resistor). The 1.25 V corresponds to the typical voltage drop in two PN silicon semiconductor junctions at ambient temperature, which is part of the I_{set} (gain setting) circuit of the transconductance amplifier (the input differential pair of the LT1228 features a current source implemented with a Wilson current mirror) [45].

The amplifier only functions properly if $I_{set} > 0$, assuming the output voltage of the controlling DAC is software limited to values between 1.3 V and 1.9 V, the maximum and minimum capacitance values can be obtained, using the following expressions [45]:

$$I_{setMin} = \frac{V_{setMin} - 1.25}{R_{set}} = \frac{1.3 - 1.25}{5600} \approx 8.9286 \mu A$$

$$g_{mMin} \approx 9.86 \times I_{setMin} \approx 88.0357 \mu A/V$$

$$C_{LOADMin} \approx 1 \times 10^{-9} + 99 \times 10^{-6} g_{mMin} \approx 9.7155 nF \approx 10 nF$$

$$I_{setMax} = \frac{V_{setMax} - 1.25}{R_{set}} = \frac{1.9 - 1.25}{5600} \approx 116.0714 \mu A$$

$$g_{mMax} \approx 9.86 \times I_{setMax} \approx 1.1445 mA/V$$

$$C_{LOADMax} \approx 1 \times 10^{-9} + 99 \times 10^{-6} g_{mMax} \approx 114.3020 nF \approx 114 nF$$

The maximum output current of the transconductance amplifier is of 100 μA , so attention must be paid, the gain must not be increased too much (V_{set} voltage should be limited), otherwise there is a risk of saturating the output of the OTA, if this happens, the circuit loses linearity and the circuit ceases to behave like a capacitive load [45].

DC blocking capacitors were added in series with the input of the circuit to avoid issues caused by large offsets generated in common-mode offset rejection tests. All components of the circuit correspond to those shown in the figures with the exception of the opamps, which are OPA2350 from Texas Instruments Incorporated, which model is not defined in LTSpice libraries. Vee corresponds to the power supply ground, Vdd to the 5 V supply voltage, and the circuit ground corresponds to the midpoint voltage (2.5 V).

Prototype Printed Circuit Board (PCB)

A variable capacitance printed circuit board was also designed and fabricated. The PCB design is presented in figure 2.3.5.

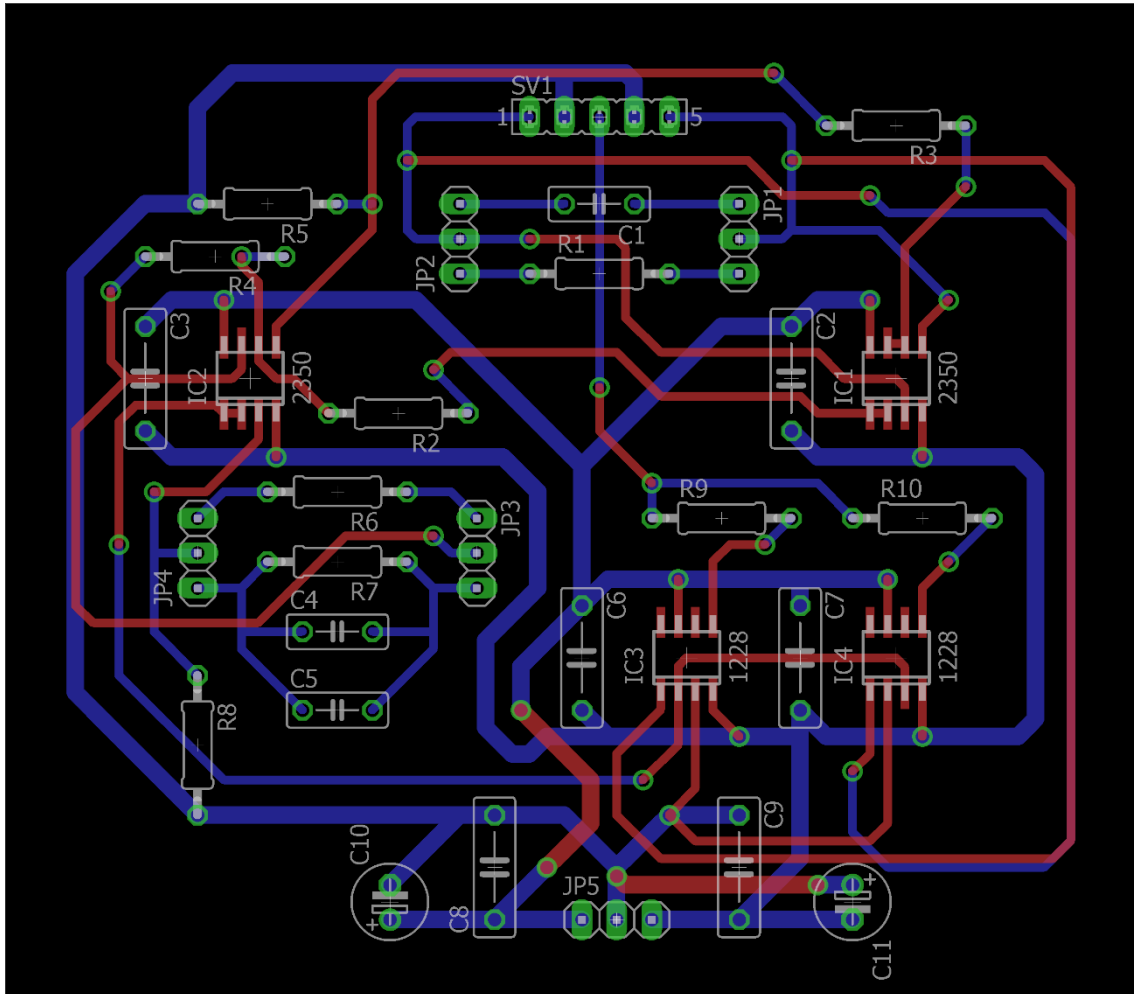


Figure 2.3.5. Variable Capacitance Printed Circuit Board (PCB)

The printed circuit board has four jumpers that allow three possible configurations. If the jumpers JP1 and JP2 are connected from the midpoint to the upper pin (including the capacitor C1 in the circuit) and JP4 and JP2 are connected from the midpoint to the lower pin (including the two capacitors, C4 and C5 and the resistor, R7, in the circuit), the circuit behaves as a variable capacitance circuit (the circuit is the same as the circuit presented in sub-section, Circuit Schematic of this section, please see figures 2.3.3 and 2.3.4). If the jumpers are connected in the other position, including resistors R1 and R6 instead of the capacitors and R7, the circuit behaves as a variable resistance circuit.

A third configuration is possible, in which, jumpers are removed from the board, and wire jumpers are connected from the midpoint of JP1, JP2, JP3 and JP4, allowing the user to define the capacitance and resistance values of the reference elements on an external PCB or breadboard. This feature allows the capacitance and resistance variation range to be modified according to the needs.

The board has two connectors named SV1 and JP5. The connections are made according to table 2.1:

Connector Name	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5
SV1	Variable Impedance Terminal 2 (V_{load}^-)	Midpoint Supply Voltage ($V_s/2$)	Impedance control voltage (V_{set})	Midpoint Supply Voltage ($V_s/2$)	Variable Impedance Terminal 1 (V_{load}^+)
JP5	Positive Power Supply (V_s^+)	Midpoint Supply Voltage ($V_s/2$)	Negative Power Supply (V_s^-)		

Table 2.1. Printed Circuit Board (PCB) headers

JP5 is the power supply connector. SV1, has two midpoint supply voltage outputs, an input for impedance control, and the two floating terminals of the variable impedance load. The DC decoupling capacitors are not included in this board, because it could also be used to simulate a variable resistance.

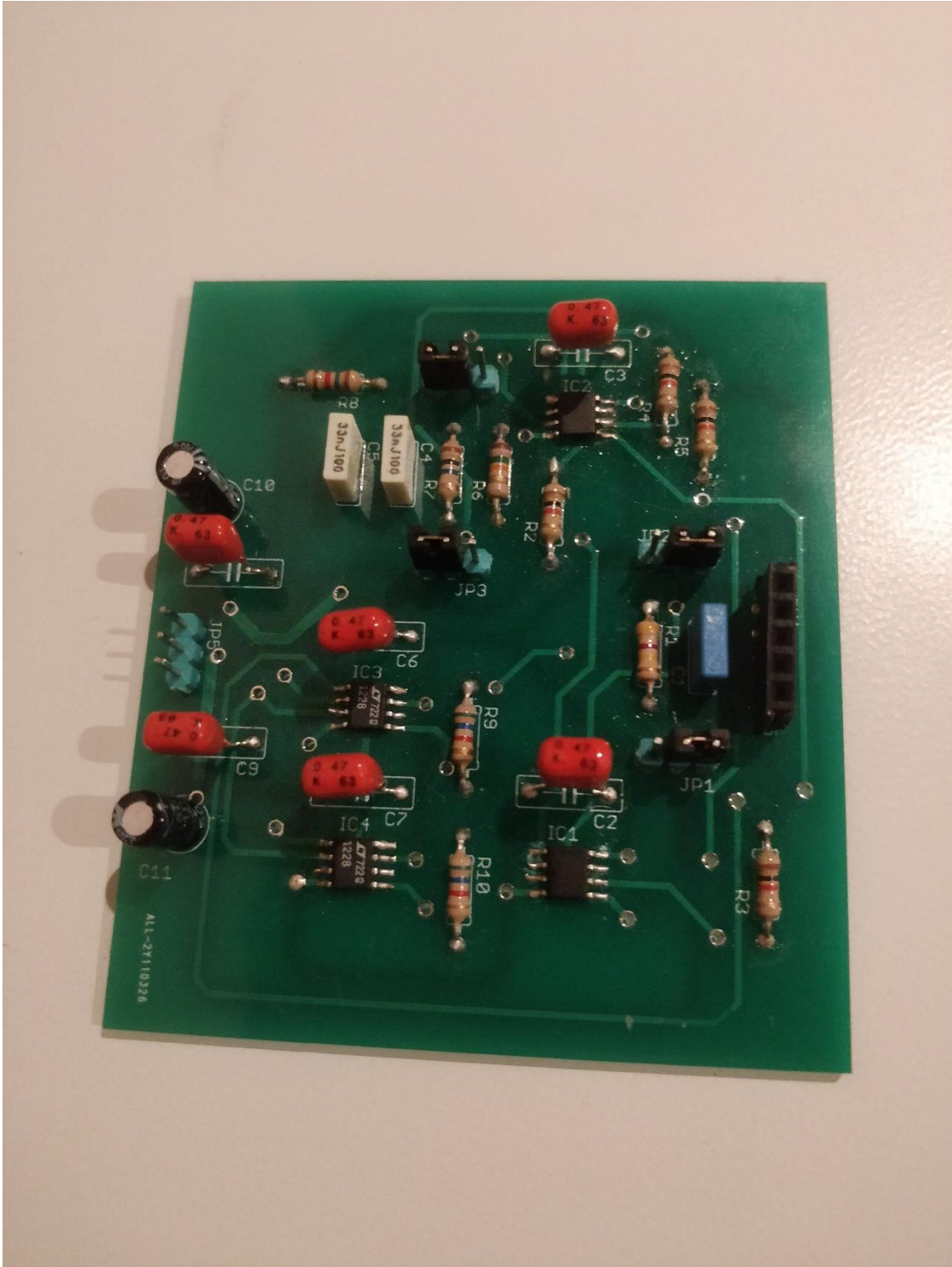


Figure 2.3.7. Variable Impedance PCB, showing the jumpers configured for variable capacitance

Capacitance Control (DAC121C085)

Capacitance control is performed by defining the V_{set} voltage accordingly with the expressions previously mentioned. The variable voltage source corresponds to a digital-to-analog converter, more precisely the DAC121C085 from Texas Instruments Incorporated. This DAC has a 12 bit resolution and I²C compatible interface. The device was chosen due to its extended power supply range (operates with supply voltages between 2.7 V and 5 V), the support of I²C fast-mode (400 kHz) and because it features rail-to-rail voltage output. The equivalent block diagram of the DAC121C085 is presented in figure 2.3.8.

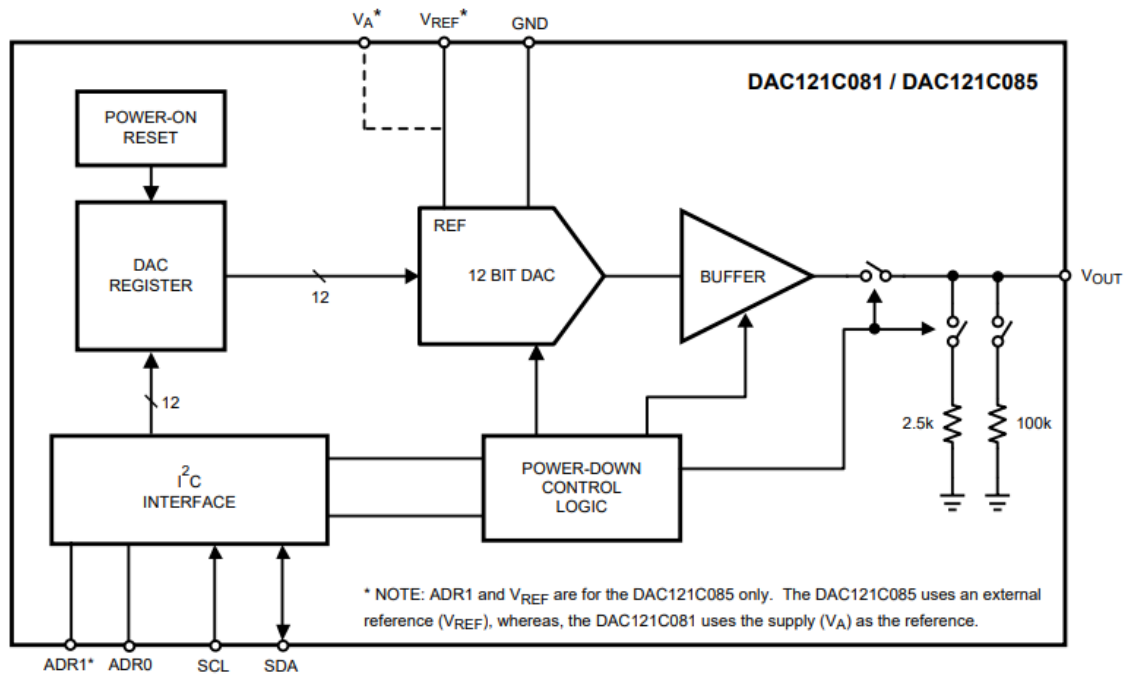


Figure 2.3.8. DAC121C085 simplified block diagram [47]

The DAC121C085 has a mode of operation very similar to the DAC8552 (please refer to the Circuit Description section, Digital-to-Analog Converter sub-section), the major differences are the number of resolution bits (12 bit versus 16 bit) and the serial interface (I²C vs SPI). This DAC (DAC121C085), like the DAC8552 also features a resistor string architecture for conversion, in which a voltage divider with multiple output taps is multiplexed, setting the voltage at the output in accordance with the digital word value present in the DAC register. Unlike the DAC8552 the output voltage of the resistor string is not half of the required at the output, and so, the DAC does not need an output amplifier with a voltage gain of 2, it only requires an output voltage buffer. A simplified schematic of the multiplexed resistor string is represented in figure 2.3.9.

The expression to determine the output voltage is the following, assuming the DAC is supplied with a 3.3 V regulated supply voltage, D corresponds to the digital word value (integer value between 0 and 4095), n is the number of bits of the DAC[47]:

$$V_{OUT} = V_{REF} \frac{D}{2^n} = 3.3 \times \frac{D}{4096} [V]$$

The DAC is supplied by a 3.3 V regulated power supply, because V_{set} takes values only between 1.3 V and 1.9 V, so a higher supply voltage is not required, as it will contribute to more power dissipation (in the DAC).

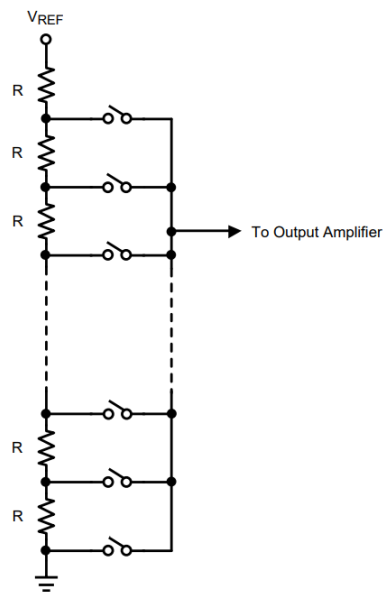


Figure 2.3.9. DAC121C085 multiplexed resistor string [47]

I²C Mode of Operation

The DAC121C085 features an I²C serial interface, capable of operating at frequencies of up to 3.4 MHz (high-speed mode). However the microcontroller (AT91SAM3X8E) only supports I²C frequencies up to 400 kHz (fast mode), so this mode corresponds to the communication mode used in system implementation.

I²C is a serial interface used to communicate between a master device (usually a microcontroller) and one or more digitally controllable integrated circuits. It is a 2-wire interface, one of the connections, SCL, corresponds to the clock provided by the master device (microcontroller) which defines the communication rate, and the other connection, SDA, is an half-duplex (bidirectional) communication channel used by the master device to transmit data to the slave device(s) and/or to receive data from the device(s). Generally, I²C is much slower than SPI, and could not be used when high bitrates are required.

The I²C interface does not have a chip select, the master selects the target device(s) with a seven bit address sent in the beginning of the communication. Some slave devices have one, two, three or more bits of the address configurable by hardware connections (by connecting the address defining pins to the ground, to the supply rail and in some cases left floating). This feature is useful when more than one device is connected to the same I²C bus, and must be individually controlled. Usually different types of devices and different manufacturers have different address starting bits, the last bits could be hardware programmable.

The timing diagram for reliable I²C operation, of the DAC121C085 is shown in picture 2.3.10.

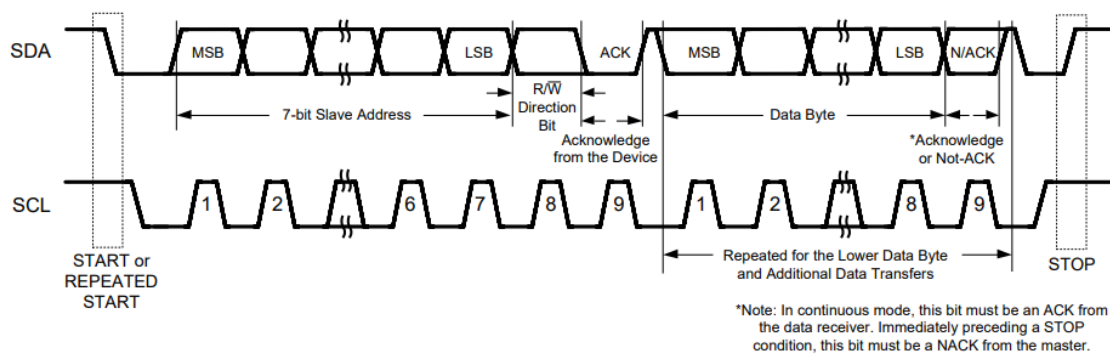


Figure 2.3.10. DAC121C085 I2C interface timing diagram [47]

To start the communication, the master must maintain the clock at high logic level (SCL), and set the SDA to low logic level, then the master device starts generating a square wave clock signal (SCL) at the desired frequency (in the implementation is 400 kHz), and sends the 7 bit slave address (to the SDA), followed by the direction bit (logic high for receiving, and logic low for transmitting), the DAC121C085 acknowledges (or not if the address is not correct or if the communication failed), by setting SDA to the low logic level, and the master starts transmitting or receiving the data bits. After receiving 8 bits (1 byte), the receiver device, acknowledges (or not) the data, by setting the SDA to the low logic level, the process repeats to receive one or more bytes. To stop communicating, the master device sets the SCL (clock) to the high logic level, followed by a low to high logic level transition in the SDA. The sequence of bits that must be sent to the DAC to define its output voltage is presented in figure 2.3.11.

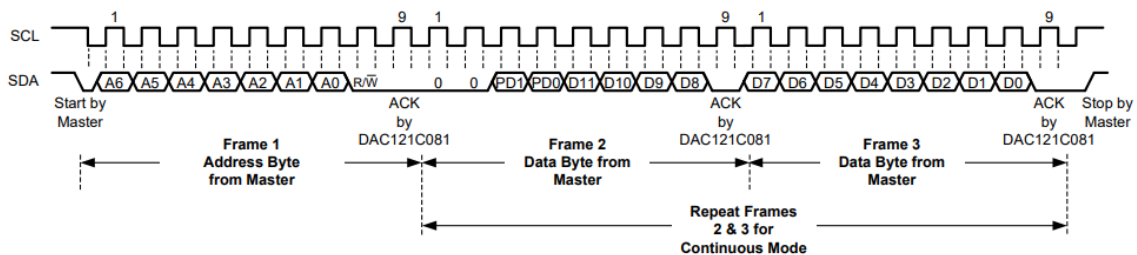


Figure 2.3.11. Data sequence for writing to the DAC121C085 [47]

Three bytes must be sent (24 bits) by the master device (microcontroller), to set the DAC output voltage. All bytes are sent with the most significant bit first.

The first byte contains the seven address bits (A6-A0) and the read not write flag (that in this case, for writing, must be in the low logic level). The second byte contains two bits at low logic level, two power down bits (not used in the implementation, remaining at low logic level) and the four most significant bits of the data word of the DAC (D11-D8). The third and last byte contains the remaining 8 bits of the data word of the DAC (D7-D0).

The DAC also allows reading its internal values, the procedure is the same, but the master sends the first byte with the read not write flag at high logic level and the communication of the following two bytes resumes in the opposite direction, the DAC sends the bytes and the master acknowledge the data. This feature is not currently implemented in the system. It was only used for debugging purposes during the development phase.

Since the system is intended to test one lead ECG systems, two electrodes must be simulated, as well as the corresponding skin-electrode interfaces. Two variable capacitance circuits and two controlling DACs are incorporated in the system, since there is more than one I²C device, the addresses of the two DACs have to be different. Hardware defined address bits need to be set, figure 2.3.12, shows the different possible configurations as well as the configurations used in the implementation of the ECG test system (represented by the green and blue boxes). The chosen slave addresses are the 13 and 14 (decimal values).

Slave Address [A6 - A0]	DAC121C085 (VSSOP)		DAC121C081 (SOT AND WSON) ⁽¹⁾	Do Not Use ⁽²⁾
	ADR1	ADR0	ADR0	
0001100	Floating	Floating	Floating	1000110
0001101	Floating	GND	GND	1000110
0001110	Floating	V _A	V _A	1000111
0001000	GND	Floating	-----	1000100
0001001	GND	GND	-----	1000100
0001010	GND	V _A	-----	1000101
1001100	V _A	Floating	-----	1100110
1001101	V _A	GND	-----	1100110
1001110	V _A	V _A	-----	1100111
1001000	----- Broadcast Address -----			1100100

Figure 2.3.12. Hardware configurable slave addresses (DAC121C085) [47]

The sampling rate of the variable capacitance DACs is of 100 SPS, allowing the generation of time varying capacitance control signals, with acceptable temporal resolution (at least 10 samples), with a frequency of up to 10 Hz (adjustable between 0.01 Hz and 10 Hz).

2.3.2 Variable Resistance Circuit

A variable resistance circuit simulates the resistive component of the skin-electrode interface. During the planning phase, two options existed to implement the circuit, one with the variable impedance circuit (of the previous section) in variable resistance mode, and the other by means of a digital potentiometer. Both solutions have advantages and disadvantages. The variable impedance circuit has the advantage of higher resolution, because it uses a 12 bit DAC, but has the disadvantage of higher power consumption (about 40 mA per variable resistance, 80 mA in total) when compared to a dual digital potentiometer (that has a current consumption of less than 0.1 mA). But, the main disadvantage of the variable impedance circuit, is the limited range of resistance values it can provide, by varying the V_{set} voltage between 1.2 V and 2.0 V (referenced to power supply ground), the resistance varied between 109 k Ω and 9 k Ω in the linear region (measured with an Agilent Technologies 34405A digital multimeter), with a reference resistance of 470 k Ω . This variation, though expressive, does not occur in the desired range (10 k Ω to 1 M Ω), and only allows the simulation of some types of electrodes. Being so, the resistance variation, was implemented in the system by means of an 8 bit dual 1 M Ω potentiometer.

AD5242BRZ1M Dual Digital Potentiometer

To implement the variable resistance circuit, the AD5242BRZ1M, an 8 bit dual digital 1 M Ω potentiometer, from Analog Devices Incorporated is incorporated in the system. This potentiometer operates with supply voltages in the range of 2.7 V to 5.5 V and features an I²C compatible serial interface. The block diagram of the AD5242 is presented in figure 2.3.13.

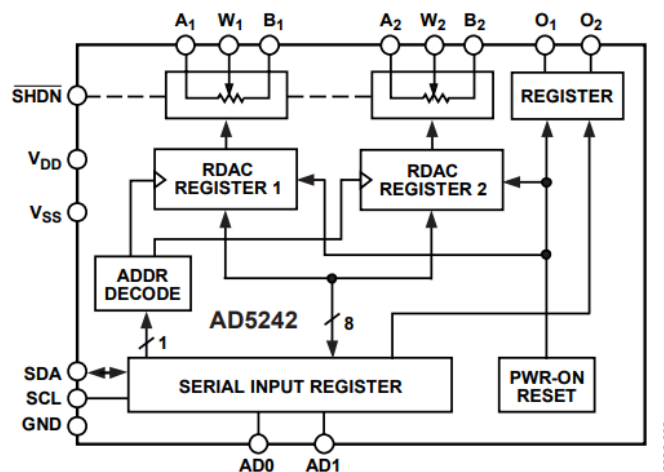


Figure 2.3.13. AD5242 dual digital potentiometer simplified block diagram [48]

The principle of operation of the AD5242 is relatively simple. The circuit features a serial interface, which receives data from a master device, the received word contains a set of control bits and data bits (which define the potentiometer setting).

Two registers exist, one per resistor string (figure 2.3.13), its function is to control the resistor string multiplexers (wiper tap) in accordance with the data and control bits sent by the master. Since I²C allows bidirectional communication, the values from the registers can also be read and send to the master device (the microcontroller). This last functionality is not used in the implemented system.

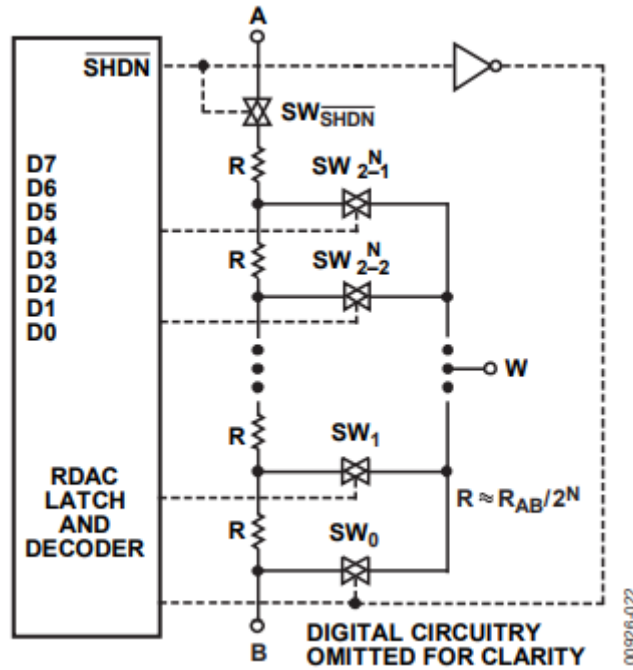


Figure 2.3.14. Simplified schematic of the AD5242 resistor string DAC [48]

The wiper (W) and the B terminals correspond to the variable resistor terminals in the implemented circuit. The not shutdown input is tied to the positive supply rail, terminal A is left open (floating). Digital outputs O₁ and O₂ are not used and left floating. Address inputs are tied to ground. The supply voltage of the circuit is provided by the 3.3 V regulator (the same voltage as the microcontroller and the other I²C devices).

The expression that gives the resistance between the terminals W and B is the following:

$$R_{WB} = \frac{D}{2^n} R_{AB} + R_W$$

The typical wiper resistance (R_W) is of about 60 Ω , R_{AB} is total string resistance, 1 M Ω , D is an 8 bit positive integer value and n is the resolution of the potentiometer in bits. Substituting the values, and ignoring the contribution of R_W , due to the fact that $R_{AB} \gg R_W$:

$$R_{WB} \cong \frac{D}{2^n} R_{AB} \cong \frac{D}{256} \times 1000 [k\Omega]$$

I²C Mode of Operation

The microcontroller communicates with the AD5242 via I²C serial interface. Fast mode of operation (400 kHz), is supported by both master and slave device, being used in the implemented circuit. The timing diagram of the AD5242 is presented in figure 2.3.15.

The master device starts communicating with the digital potentiometer by making a high to low logic transition in the SDA bus, the clock starts at the high logic level. After the start signal is sent, the master device starts the clock, and sends a seven bit address (in the case of the implemented system, the hardware defined address bits, AD1 and AD0 are logic zeros, so the address of the device is 44, representation in decimal base). Then the master device sets the read not write flag (low for writing the potentiometer register and high to read it). If the address bits are correct the AD5242 acknowledges the reception by pulling the SDA bus to the low logic level.

The next byte is the instruction byte, which contains the potentiometer register bit (B not A), that must be set low to write to the register of potentiometer B and high to write the potentiometer A register. RS is the midpoint reset flag, which resets the selected potentiometer register to the midpoint resistance value, SD is the shutdown flag (active high). O₁ and O₂ are two digital bits that can be used to implement logic functions or control other devices, not used in the implemented system. The next three bits of the instruction byte are don't care bits. After receiving the 8 instruction bits, the AD5242 acknowledges the transmission, by setting the SDA bus to the low logic level. The next byte (bits D7 to D0), the data byte is the digital value (to be stored in the potentiometer register), which controls the selected potentiometer wiper position. After receiving the last byte, the AD5242 acknowledges the reception, and the master stop the communication by setting the clock signal (SCL) to the logic high value and by making a low to high transition in the SDA bus. If in the slave address byte the read not write flag is set to logic high, the data byte from the last addressed potentiometer register is sent by the AD5242 to the master device (microcontroller). This last function is not implemented and was only used for debugging purposes during development phase.



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Figure 2.3.15. AD5242 timing diagram [48]

2.4 System's Mode of Operation

In the previous sections a more hardware oriented analysis is made, in this section the software-hardware interaction is explained. The device that has the main role in this section is the microcontroller, it acts “like a conductor in the orchestra”. Is this device that is responsible for performing tests following the operator's specifications.

Another important aspect covered in this section is the human-machine interface. How an ECG test is specified, which parameters and files are needed to perform a test? Those questions are answered in this chapter at the User Interface section. This section is intended to provide important information about how the operator must use this system, and act a bit like a simplified user manual or guide.

2.4.1 User Interface

The system does not need a computer to be operated, because it is powered by two powerbanks, it runs the test from files stored in a microSD memory card (test file and waveform) and records the results in the same support. However, a computer is needed to create and specify the test file, to provide the sample waveform and to analyze the results after test completion.

Test File

The test file need to have “.ect” extension, and to be named “test”, the full filename plus extension should be “test.ect”. The file is a normal text file with a different extension that should be encoded in the UTF-8 format. The file has to be defined with a test duration and should also have an initial definition of test parameters. The parameters can be changed over time, a maximum of 23 parameter changes is accepted, if this value is not respected the subsequent parameter changes will not have any effect. The maximum test duration is 240 seconds (4 minutes) and the minimum test duration is 10 seconds.

The test file should be specified as follows (the initial parameter definition should be made, changes over time are optional):

```
<0>  
test duration in seconds  
OT(output type)  
ECG(amplitude factor, wave type)  
CM(DC value [V], amplitude [V], frequency [Hz])  
Diff(DC value [mV], amplitude [mV], frequency [Hz])  
Ce1(DC value or min. voltage [V], amplitude or max. voltage [V], frequency [Hz], variation type)  
Ce2(DC value or min. voltage [V], amplitude or max. voltage [V], frequency [Hz], variation type)  
Re1(med. or min. resistance [kΩ], amplitude or max. resistance [kΩ], frequency [Hz], variation type)  
Re2(med. or min. resistance [kΩ], amplitude or max. resistance [kΩ], frequency [Hz], variation type)  
LOff(left lead off, right lead off)  
<\0>
```

<1>
 timestamp 1 in seconds
 ECG(amplitude factor, wave type (ignored))
 CM(DC value [V], amplitude [V], frequency [Hz])
 Diff(DC value [mV], amplitude [mV], frequency [Hz])
 Ce1(DC value or min. voltage [V], amplitude or max. voltage [V], frequency [Hz], variation type)
 Ce2(DC value or min. voltage [V], amplitude or max. voltage [V], frequency [Hz], variation type)
 Re1(med. or min. resistance [kΩ], amplitude or max. resistance [kΩ], frequency [Hz], variation type)
 Re2(med. or min. resistance [kΩ], amplitude or max. resistance [kΩ], frequency [Hz], variation type)
 LOff(left lead off, right lead off)
 <\1>

<2>
 timestamp 2 in seconds
 Ce1(DC value or min. voltage [V], amplitude or max. voltage [V], frequency [Hz], variation type)
 Ce2(DC value or min. voltage [V], amplitude or max. voltage [V], frequency [Hz], variation type)
 Re1(med. or min. resistance [kΩ], amplitude or max. resistance [kΩ], frequency [Hz], variation type)
 Re2(med. or min. resistance [kΩ], amplitude or max. resistance [kΩ], frequency [Hz], variation type)
 LOff(left lead off, right lead off)
 <\2>

(...)

<10>
 Timestamp 10 in seconds
 LOff(lpositive lead off, negative lead off)
 <\10>

Description of Test File Parameters

<n> - n is called test index, a positive integer number, taking values from 0 to 23, 0 corresponds to the initial parameter definition and has to be present in order for the test to run, each parameter definition must have the index incremented by one in relation to the previous parameter definition, otherwise the test execution will be aborted. The user should interpret this number as *parameter change number n*. This character sequence also act as a delimiter, defining the starting point of a parameter definition section.

test duration in seconds - is a positive integer number, that corresponds to the total test duration in seconds, a test must have a minimum duration of 10 seconds and a maximum duration of 240 seconds (4 minutes). Without this parameter defined, or with a value outside the specified range, the test will not be executed.

OT (output type)

output type - corresponds to a positive integer value, for a functionality that is currently not implemented in software, allows the usage of ECG front-ends with various types of outputs and interfaces (for example, 0 corresponds to an analog output front-end, 1 corresponds to a SPI interface of a device from Maxim Integrated Products Incorporated, 2 corresponds to a SPI interface of a device from Texas Instruments Incorporated, and so on). Though the functionality is not implemented the parameter is read and the test would not run if the parameter is not set to 0 (analog output).

ECG(amplitude factor, wave type)

amplitude factor - corresponds to a positive floating point value, taking values between 0.001 and 1.0, which allows the user to attenuate (divide) the ECG signal, by a factor of 1 to 1000. If not defined defaults to 1.0.

wave type - corresponds to a positive integer for a feature not currently implemented, which allows the user to choose different ECG waveform files, for example (1 corresponds to ecg1.wav, 2 to ecg2.wav, and so on). The ECG waveform could not be changed during the test, must be defined only at index 0 (startup), changes during the test will be ignored, this parameter defaults to 1.

CM(DC value [V], amplitude [V], frequency [Hz])

DC value - corresponds to a floating point value, which defines the DC component of the common-mode component (measured in reference to the supply voltage midpoint, 2.5 V) of the ECG signal in Volt. The accepted range of values is from -2.5 to 0.5. The default value is 0.0 (meaning no offset)

amplitude - corresponds to a positive floating point value, which defines the amplitude (in Volt), of the interference sine wave signal added to the common-mode component of the ECG signal. The accepted value range is between 0.001 and 1.0. The default value is 0.001.

frequency - is a positive floating point value, which defines the frequency in Hertz, of the sine interference signal added to the common-mode component of the ECG signal. This parameter accepts values between 0.02 and 500. The default value is 50.

Diff(DC value [mV], amplitude [mV], frequency [Hz])

DC value - corresponds to a floating point value, which defines the DC component of the differential component (measured in reference to the supply voltage midpoint, 2.5 V) of the ECG signal in miliVolt. The accepted range of values is from -2.5 to 0.5. The default value is 0.0 (meaning no offset)

amplitude - corresponds to a positive floating point value, which defines the amplitude (in miliVolt), of the interference sine wave signal added to the differential component of the ECG signal. The accepted value range is between 0.001 and 1.0. The default value is 0.001.

frequency - is a positive floating point value, which defines the frequency in Hertz, of the sine interference signal added to the differential component of the ECG signal. This parameter accepts values between 0.02 and 500. The default value is 50.

CeN(DC value or min. voltage [V], amplitude or max. voltage [V], frequency [Hz], variation type)

N - a positive integer, could be 1 or 2, 1 corresponds to the variable capacitance circuit of the positive electrode, and 2 to the variable capacitance circuit of the negative electrode.

DC value or min. voltage - corresponds to a positive floating point value, this parameter defines the DC component or minimum value of the capacitor control voltage in Volt (referenced to the power supply ground). It is the DC value for the sinewave and the constant, the minimum value of the square, triangle and sawtooth waves. The parameter accepts values between 0.0 and 3.0. The default value is 1.5 for the DC value and 1.3 for the minimum voltage.

amplitude or max. voltage - corresponds to a positive floating point value, this parameter defines the amplitude or maximum value of the capacitor control voltage in Volt (referenced to the power supply ground). It is the amplitude for the sinewave, the maximum value of the square, triangle and sawtooth waves. The parameter accepts values between 0.0 and 3.0 for the maximum voltage and between 0.0 and 1.5 for the amplitude. The default value is 0.3 for the amplitude and 1.9 for the maximum voltage.

frequency - corresponds to a positive floating point value, this parameter defines the frequency in Hertz of the time varying signals, square, triangle, sawtooth and sine waves. The parameter accepts values in range of 0.01 to 50 Hz. The default value is 0.1 Hz.

variation type - corresponds to a non-negative integer value, used to select the variation type. 0 corresponds to no variation or a constant control voltage, 1 corresponds to a square wave variation, 2 corresponds to a positive slope sawtooth wave, 3 corresponds to a negative slope sawtooth wave, 4 corresponds to a triangle wave and 5 corresponds to a sinewave. Signals of type 0 will have constant voltage defined in “DC value or min. voltage”. Signals of types 1, 2, 3 and 4 will vary between the values defined in “DC value or min. voltage” and “amplitude or max. voltage”. Signals of type 5 will have a signal with an amplitude of “amplitude or max. voltage” and will vary around a medium value of “DC value or min. voltage”. The parameter only accepts values between 0 and 5, though a 6th user defined variation type (loaded from a .WAV file) option could be added, but is not currently implemented in software. The parameter defaults to variation type 0 (constant voltage).

ReN(med. or min. resistance [kΩ], amplitude or max. resistance [kΩ], frequency [Hz], variation type)

N - a positive integer, could be 1 or 2, 1 corresponds to the variable resistance circuit of the positive electrode, and 2 to the variable resistance circuit of the negative electrode.

med. or min. resistance - corresponds to a positive floating point value, this parameter defines the medium or minimum value of resistance in kiloOhm. It is the medium resistance value for the sinewave and the constant, the minimum value of the square, triangle and sawtooth waves. The parameter accepts values between 0.0 and 999.0. The default value is 500.0 for the medium resistance in the sinewave and 100.0 for the remaining waves and constant.

amplitude or max. resistance - corresponds to a positive floating point value, this parameter defines the amplitude or maximum value of the resistance in kiloOhm. It is the amplitude for the sinewave, the maximum value of the square, triangle and sawtooth waves. The parameter accepts values between 0.0 and 999.0 for the maximum resistance and between 0.0 and 500.0 for the amplitude. The default value is 400.0 for the amplitude and 900.0 for the maximum resistance.

frequency - corresponds to a positive floating point value, this parameter defines the frequency in Hertz of the time varying signals, square, triangle, sawtooth and sine waves. The parameter accepts values in range of 0.01 to 50 Hz. The default value is 0.1 Hz.

variation type - corresponds to a non-negative integer value, used to select the variation type. 0 corresponds to no variation or a constant resistance, 1 corresponds to a square wave variation, 2 corresponds to a positive slope sawtooth wave, 3 corresponds to a negative slope sawtooth wave, 4 corresponds to a triangle wave and 5 corresponds to a sinewave. Signals of type 0 will have constant resistance defined in “med. or min resistance”. Signals of types 1, 2, 3 and 4 will vary between the values defined in “med. or min resistance” and “amplitude or max. resistance”. Signals of type 5 will exhibit a resistance variation with an amplitude of “amplitude or max resistance” that will vary around a medium value of “med. or min. resistance”. The parameter only accepts values between 0 and 5, though a 6th user defined variation type (loaded from a .WAV file) option could be added, but is not currently implemented in software. The parameter defaults to variation type 0 (constant resistance).

LOff(left lead off, right lead off)

left lead off - corresponds to an integer that must have binary value (0 or 1). 1 enables the left electrode lead off functionality, 0 disables it. If a different value is set, the system defaults to lead off disabled.

right lead off - corresponds to an integer that must have binary value (0 or 1). 1 enables the right electrode lead off functionality, 0 disables it. If a different value is set, the system defaults to lead off disabled.

timestamp n in seconds - is a positive integer value, that corresponds to the elapsed time in seconds between the start of the test and the current parameter modification. The timestamp has to be lower than the test duration, higher than the previous timestamp (if there is any) and higher than zero.

<n> - n is the current parameter modification test index. This character sequence ends a parameter definition section. The user should interpret this sequence as *end of parameter change number n*.

Test File Example

In the initial test section (index 0), it is advisable to define all parameters, to perform a parameter change during the test, the directive syntax has to be respected, for example, if the test starts with (constant skin-electrode resistance of the positive electrode equal to 100 k Ω):

Re1(100.0, 500.0, 0.1, 0)

And the user wants to change the skin-electrode resistance variation of the positive electrode to type 2 (positive slope sawtooth wave varying between 100 k Ω and 500 k Ω with a frequency of 0.1 Hz):

Re1(100.0, 500.0, 0.1, 2)

The system does not accept,

Re1(...,2)

or a similar syntax and ignores the parameter change.

Of course, if only this change is intended to be made, for example, after 30 seconds of test (in a test with a duration of, for example, 120 seconds), not all specifications (ECG, common-mode, differential mode, variable capacitance, lead-off) need to be written to perform the parameter change. The user must write, assuming it is the first parameter change:

<1>

30

Re1(100.0, 500.0, 0.1, 2)

<\1>

The user can perform a second parameter change, after 60 seconds of test time elapsed, for example, to change the variation type to sinewave, with 100 k Ω of amplitude and 200 k Ω of offset. The parameter change should be performed as follows:

<2>

60

Re1(200.0, 100.0, 0.1, 5)

<\2>

A negative electrode lead-off performance test, after 70 seconds, can be performed has follows (in the first instruction the lead-off is activated):

<3>

70

LOff(0,1)

<\3>

In the second instruction, the lead-off is deactivated, after 80 seconds of test, for example:

<4>

80

LOff(0,1)

<\4>

The remaining time could be used to perform other parameter changes or to better evaluate lead-off performance.

Example of a Complete Test File

An example of a lead-off performance test with total duration of 120 seconds, with positive lead-off activated at 30 seconds, deactivated at 40 seconds, and negative lead-off activated at 70 seconds and deactivated at 80 seconds. The initial parameter definition is also present. The file is defined as follows:

<0>

120

OT(0)

ECG(0.5,1)

CM(0.0,0.001,50.0)

Diff(0.0,0.001,50.0)

Ce1(1.3,2.00,0.1,0)

Re1(100.0,900.0,0.1,0)

Ce2(1.3,2.00,0.1,0)

Re2(100.0,900.0,0.1,0)

LOff(0,0)

<\0>

<1>

30

LOff(1,0)

<\1>

<2>

40

LOff(0,0)

<\2>

<3>

70

LOff(0,1)

<\3>

<4>

80

LOff(0,0)

<\4>

ECG Waveform File

The ECG waveform file is WAVE (Waveform Audio File Format), with “.wav” or “.WAV” extension. The name of the file should be “ecg1”, the complete filename with extension is “ecg1.wav”. The file must contain uncompressed data in the LPCM (linear pulse code modulation) format, only one channel and a sample rate of 1 kHz (1kSPS), other sample rates are accepted, the range of sample rate values accepted is from 500 SPS to 2 kSPS. Each sample has a resolution of 16 bit (signed). If some file parameter(s) is/are different the test would not be performed.

The file must contain one waveform period of samples, and a maximum size of 10 KiB (10240 bytes). The waveform should be repeatable, it should not show deformations or spikes when periodically represented. The graphical representation of an ECG waveform file (sampled at 1 kSPS) is shown in figure 2.4.1.

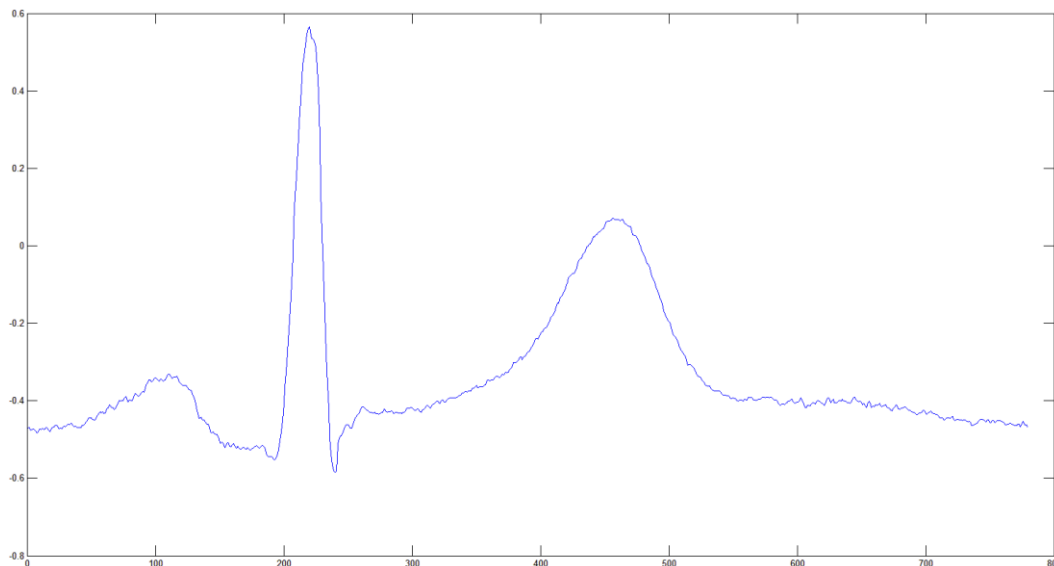


Figure 2.4.1. Graphical representation of the samples from a waveform file

In the graph, the horizontal axis corresponds to the sample number and the vertical axis correspond to the normalized amplitude (a value that varies in the range of -1.0 to 1.0). This waveform contains has 780 samples (0.78 seconds) and an amplitude (peak-to-peak) of about 1.2 normalized amplitude units. The heart rate of this ECG waveform is about 77 BPM. This is the waveform currently in use, during the ECG performance tests.

Test Result File

The result file is a file with “.WAV” extension, with WAVE format. It is recorded with 16 bit (signed) samples in the LPCM format, the sample rate is defined by the waveform file (for example, if a waveform file of 1 kSPS is used, the test result file will be sampled at 1 kSPS) and has one channel only.

A file denominated “REC.WAV” will appear at the memory card after a successfully completed test. If a previously recorded file is present in the memory card it is overwritten, so the user must save the desired results on another storage device or change the filenames after test completion. This file has the duration defined in the specification of the test file.

Memory Card

A microSD memory card is required to store the waveform and test files and to record the test result. The test will not run if the memory card is not inserted or incorrectly inserted. The memory card must have the required storage space to store the result file (please refer to the WAVE Files subsection for more details). The following files must be present in the SD card, in order for the test to be performed:

- test.ect
- ecg1.wav

The memory card must be formatted with the FAT filesystem. NTFS, FAT32 or exFAT filesystems are not supported by the system.

2.4.2 Device under Test (DUT) connection

Before starting the tests the device under test (ECG front-end) must be properly connected to the system, in order for the tests to be correctly performed. At first, the system must be off, the powerbanks must be disconnected from the system. The power supplies of the test system and the DUT must be connected to the power supply ground, and supply voltage usually 3.3 V, 2.5 V or 5 V accordingly to the datasheet of the manufacturer (attention must be paid because some DUTs might be damaged by using supply voltages higher than a certain value or if supplies are inverted). The system’s differential output must be connected to the differential input of the DUT, the grey (negative) wire from the system connects to the DUT’s negative input, the orange (positive) wire from the system connects to the DUT’s positive input. The ADC input of the system is connected to the DUT’s analog output (in the case of an analog output DUT). In some cases more connections must have to be performed, like, for example, the connection of shutdown or power down pins to ground or positive rail thru a pull-up resistor, a pull-down resistor or a resistive voltage divider (attention must also be paid in order to avoid over current or over voltage at the inputs, the documentation of the DUT must be consulted).

The system also supports digital output DUTs, this function, however, is not currently implemented in software. These devices must be connected in the place of the ADC in case of SPI interface devices, or to the I²C bus in the case of I²C devices. System connection to a Sparkfun board [49], similar to the board tested are represented in figure 2.4.2. Some modifications (two electrode configuration and AC lead-off detection) had to be made to the board (refer to Circuit Description section, ECG Front End).

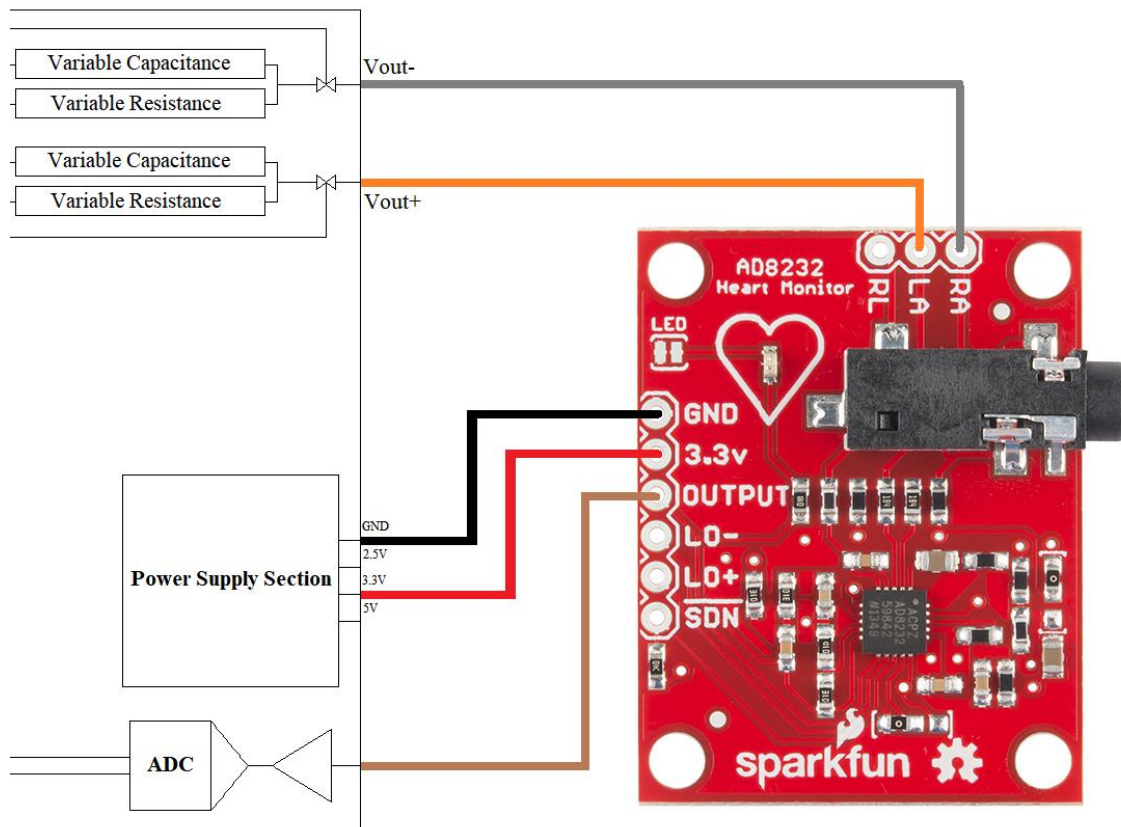


Figure 2.4.2. Analog front-end connection [adapted from 49]

2.4.3 Microcontroller Communication Interfaces and Protocols

Serial Peripheral Interface (SPI)

The serial peripheral interface is a synchronous serial data protocol developed by Motorola Incorporated. This interface allows a master device (like, for, example, a microcontroller) to communicate over short distances with one or more slave devices. It may also be used to communicate between microcontrollers [50].

Usually there are three communication lines common to all devices, these lines are the following:

- **MISO (Master Input Slave Output)** - this line allows the slave device(s) to transmit data to the master device (the slave device(s) is/ are the transmitter(s) and the master device is the receiver)
- **MOSI (Master Output Slave Input)** - this communication line is used by the master device to transmit data to one or more slave devices (the master device acts as a transmitter and the slave device(s) as the receiver(s)).
- **SCK (Serial Clock)** - synchronization signal (square wave) generated by the master device to synchronize data transmission, this signal defines the communication data rate (bit rate).

A specific communication line that is connected to every device, generally called **SS** (Slave Select) or **CS** (Chip Select) is also necessary. This line (active low) allows the master to enable or disable the communication to each device, because only one device is able to communicate with the microcontroller at a time. When the chip select signal of a device is low, it is able to communicate with the master. When this signal is high the device is unable to communicate with the master. This signal allows multiple SPI devices to be connected in the same bus (MISO, MOSI and SCK) [50].

SPI Modes of Operation

The SPI interface has four modes of operation, the modes control the clock polarity and clock phase. The clock polarity defines the level of the SCK line when the clock is idle (not varying over time), that could be the high logic level or the low logic level, polarities 1 and 0 respectively. Clock phase defines the clock variation in which data is changed (at the transmitter) and captured (in the receiver) [50].

Table 2.2 shows the different SPI modes of operation and respective clock phase and polarity. In figure 2.4.3, the timing diagram for the different SPI modes is illustrated.

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1

Table 2.2. SPI modes [51]

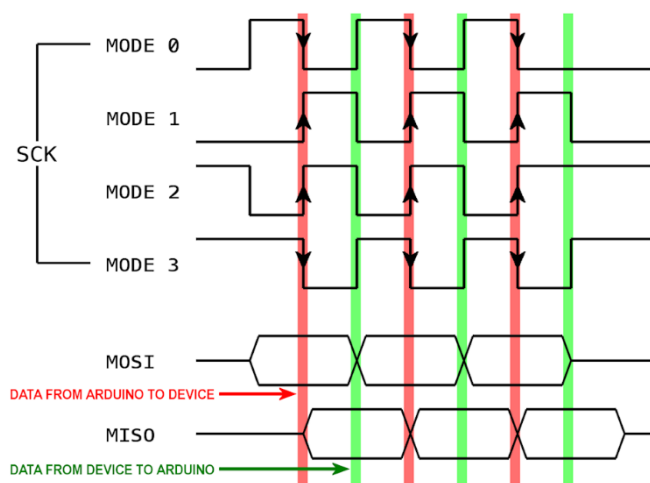


Figure 2.4.3. Timing diagram of the SPI modes [52]

Inter-Integrated Circuit (I²C)

Inter-Integrated Circuit, I²C or I²C is a serial communication protocol developed by Philips Semiconductor (now NXP semiconductors). Used in short-distance communications between a master device (in some cases there is more than one master device) and one or more slave devices. In this project the communication is between the microcontroller (master device) and the slave devices (DACs and digital potentiometer).

I²C is a two wire interface, that features a bidirectional data line (SDA) and a data synchronization signal (clock) generated by the master device (SCL). This interface does not have a chip select like SPI, the slave devices have different addresses and the master device selects the desired device by writing a 7 bit address, followed by a read not write bit, to define which device acts as the transmitter, if the bit sent is 0, the master is the transmitter, if it is 1 the slave is the transmitter. The last one, two, three or four address bits of the slave device are usually configurable by means of digital inputs of the integrated circuit, which could be connected to the ground, to the supply rail or left floating [adapted from 53].

After receiving the first byte, the corresponding slave device acknowledges the master device, by pulling the SDA line to low level. Then in accordance with the read not write bit, the master or the slave transmit a byte of data, and the receiver device acknowledges, by pulling the SDA line to low level. The process repeats until all data is transferred. Usually, when the slave device is a DAC or a potentiometer it needs three bytes. The first byte, called the address byte, contains the address and the direction bit (read not write). The second byte is called the instruction or control byte, and usually defines the addresses of the registers on the slave devices, and/or is responsible for setting control flags, it may also contain some data bits. The third and last byte, generally is a data byte. After the last byte is sent, the master device stops the communication, until other value is ready to be sent [adapted from 53].

The I²C interface operates with frequencies of 100 kHz in standard mode and 400 kHz in fast mode (mode used in this project). There are also high speed (HS) modes that allow frequencies greater than 1 MHz, these are not supported by the microcontroller used in this project.

The start condition is given by the master by pulling the SDA line to low level, while SCL remains at idle in high level. The master gives the stop condition, by setting SDA low, putting the SCL at idle in high level and then setting the SDA to high level. A timing diagram of the I²C communication protocol is presented in figure 2.4.4 [adapted from 53].

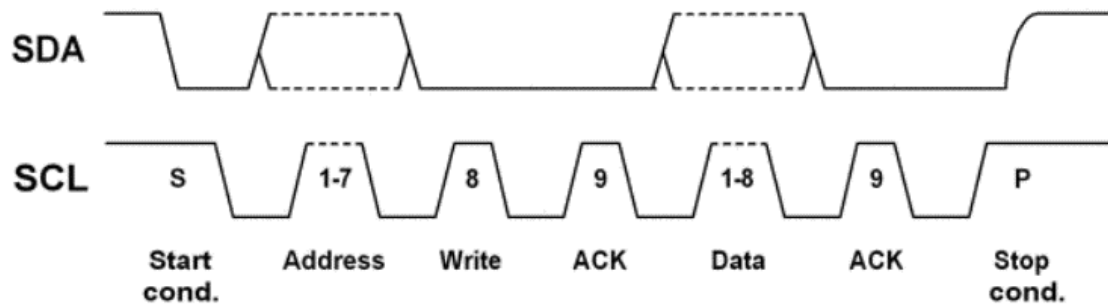


Figure 2.4.4. I2C timing diagram [53]

2.4.4 Microcontroller-Peripheral Connections

Several peripheral devices are connected to the microcontroller, a storage device (memory card), digital-to-analog converters (ECG signal generation and variable capacitance control), analog-to-digital converter (to sample the output voltage of the DUT), digital potentiometer and digital switches.

The microcontroller is responsible for file reading and writing, it has to read and interpret the test sequence of the test file as well as the waveform file (stored in the SD card). Provide the samples at the required sampling intervals to the DACs, request samples from the ADC at the required sampling interval, control the digital potentiometer and lead-off test digital switches. In sum, the microcontroller, must read the files from the SD card, and control the peripherals in order to perform the specified test and record the result.

A schematic showing all microcontroller connections is presented in figure 2.4.5. The memory card reader (micro SD module) is connected to the microcontroller's SPI interface, being supplied by the 5 V regulator of the Arduino board. The ECG signal generation DAC (DAC8552 from Texas Instruments Incorporated), communicates with the microcontroller using USART1 (configured as SPI), and features a software defined chip select (connected to pin 7 of Arduino Due board). The ADC (ADS8339 from Texas Instruments Incorporated) which records the signal output of the device under test, communicates with the microcontroller using USART0 (configured as SPI), and features a software defined chip select (connected to pin 8 of Arduino Due). The DACs (DAC121C085 from Texas Instruments), which generate the capacitance control voltage, communicate with the microcontroller using an I2C interface, the two devices are configured to have different addresses (13 and 14). Another device that communicates using an I2C interface is the dual digital potentiometer (the AD5242BRZ1M produced by Analog Devices Incorporated), that is represented by two separated blocks in figure 2.4.5 (Variable Resistance Control and Variable Resistance), this device has a different address, 44.

The Arduino Due board is powered with the barrel connector, having a supply voltage of about 10 V. The lead-off circuits (digital bidirectional switches) are controlled by two digital outputs of the microcontroller (pin 10, for the positive electrode and pin 9 for the negative electrode), when the logic level is high the switch is closed (lead-off feature disabled), when the logic level is low the switch opens (to perform the lead off test).

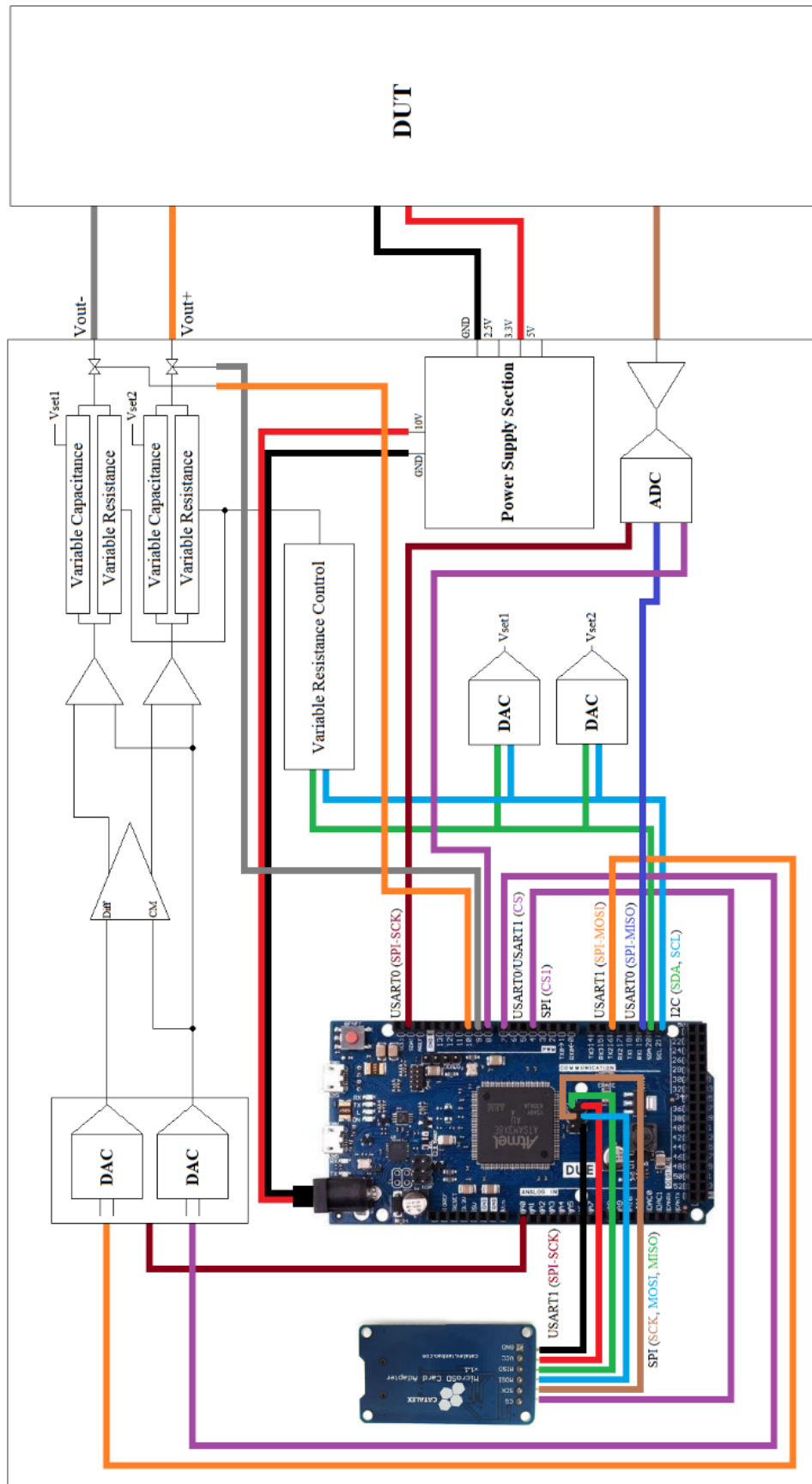


Figure 2.4.5. Schematic representation of the ECG test system, showing microcontroller connections [adapted from 22 and 54]

2.5 Software Programming

In this section, an overview of the software programming developed in this project is performed. Since this project has a significant amount of code, only the most important aspects of software programming are covered.

2.5.1 Timers

The timers, also called timer counters, are used in software programming wherever periodically execution of a function is required. From the hardware perspective, a timer is usually implemented has a counter, which is loaded with an initial value (that could be zero or another value) and then is decremented or incremented periodically (generally at the master clock rate or a divider in the case of microcontrollers) until it reaches a certain value. When the counter reaches the desired value (corresponding to the desired timer period), the initial value is loaded again and the process repeats, a timer interrupt signal is generated. The processor leaves the main cycle and enters the interrupt routine, executing a specific stretch of code (during this time, typically, the other interrupts are disabled, however, sometimes, other interrupts might have priority, like certain hardware interrupts, depending on the hardware and software microcontroller implementation).

In this project, five timers are required for four purposes. A timer with a frequency of 1 Hz (period of 1 second) is used to count the test time elapsed (in seconds) and to check if the timestamp of the test struct (stores the parameters defined in the test file) of the current test index, matches the time elapsed. Two timers are used to supply samples to the DACs at the desired sampling rate, one of the timers (associated with the capacitance control DACs) have a fixed frequency (defined in a constant) of 100 Hz (for a sample rate of 100 SPS). The timer used to supply samples to the ECG signal generation DACs, have a typical frequency of 1 kHz (1 kSPS), but, in accordance with the waveform file this frequency could be in the range of 500 Hz (for a sample rate of 500 SPS) to 2 kHz (for a sample rate of 2 kSPS) (the ECG signal generation DACs have the same sample rate as the ECG waveform file).

A timer is required to periodically define the resistance values of the dual digital potentiometer (that could be varied over time), having the same frequency as the capacitance control DACs' timer, 100 Hz (the resistance values can be varied 100 times per second).

And, to conclude, a timer is used to request samples from the ADC at the desired sample rate, its frequency is the same as the signal generation DAC, usually 1 kHz (for a sampling rate of 1 kSPS), defined by the ECG waveform file's sampling rate (that can be between 500 SPS and 2 kSPS).

It is very important to keep the code inside the timer interrupt with as few instructions as possible, avoid loops (like for example, “while” or “for”), and avoid instructions that take much time to execute (the code should be short and of quick execution). If the code is too slow to execute during the timer interrupt routine, ADC or DAC samples might be lost, due to microcontroller timing issues.

2.5.2 Test Struct

A test struct stores the test parameters read from the file. The test struct avoids simultaneous access of the test file and the recording file, during the test execution. The simultaneous access of the files could lead to file corruption and/or timing issues, so it is better to keep the whole test in an array of structs, which is stored in RAM (Random Access Memory). The size of the array is 24, allowing the user to perform parameter changes every 10 seconds in a 240 seconds file (the initial parameter definition plus 23 posterior parameter changes, executed every 10 seconds). Some parameters are converted to integer in order to accelerate the code execution inside the timer interrupt routines.

The test struct is defined as follows:

```
//Test struct
typedef struct {
    //Timestamp variable
    uint16_t timeStamp = 0;

    //ECG (Differential Mode)
    uint16_t ecgAtt = 10;
    uint8_t ecgType = 1;
    bool ecgChange = false;

    //Common-mode
    uint16_t cmDC = 32768;
    uint16_t cmAmp = 146;
    double cmFreq = 50.0;
    bool cmChange = false;

    //Differential Mode
    uint16_t diffDC = 32768;
    uint16_t diffAmp = 146;
    double diffFreq = 50.0;
    bool diffChange = false;

    //C1 Variation
    uint16_t c1DCMin = 2048;
    uint16_t c1AmpMax = 0;
    double c1Freq = 0.0;
    uint8_t c1VarType = 0;
    bool c1Change = false;

    //C2 Variation
    uint16_t c2DCMin = 2048;
    uint16_t c2AmpMax = 0;
    double c2Freq = 0.0;
    uint8_t c2VarType = 0;
    bool c2Change = false;

    //R1 Variation
    uint8_t r1DCMin = 26;
    uint8_t r1AmpMax = 0;
    double r1Freq = 0.0;
    uint8_t r1VarType = 0;
    bool r1Change = false;

    //R2 Variation
    uint8_t r2DCMin = 26;
    uint8_t r2AmpMax = 0;
    double r2Freq = 0.0;
    uint8_t r2VarType = 0;
    bool r2Change = false;

    //Lead-Off
    bool L1Off = false;
    bool L2Off = false;
    bool lOffChange = false;
} Test;
```

As can be noticed there are additional parameters (variables of the boolean type, with the word “Change” in the name) in the test structure’s definition, this variables indicate, which parameter group(s) suffered modifications from the previous value (which parameter line(s) are defined in the test file for the actual test index). Some sample defining parameters like, the ECG amplitude factor, the maximum, minimum, amplitude and medium values, of the capacitance control voltage and variable resistances are converted to integer to optimize processing time. The frequency cannot be converted to integer because the sine wave samples are generated in “real time” and the sine function’s argument is a floating point value (double). Lead-off test variables are of the boolean type, a false value closes the lead-off switch and true opens the switch. The maximum and minimum test duration values are written in constants, and are of 240 seconds (4 minutes) and 10 seconds, respectively.

2.5.3 WAVE Files

The WAVE (Waveform Audio File Format) is a subset of Microsoft Corporation’s RIFF specification for the storage of multimedia files. The RIFF file starts with a header followed by a series of data chunks. Commonly the WAVE file is a RIFF file with a single “WAVE” chunk, which consists of two sub-chunks (a format chunk specifying the type of data and a data chunk containing the waveform samples). The data organization of a WAVE file is shown in figure 2.5.1 [89].

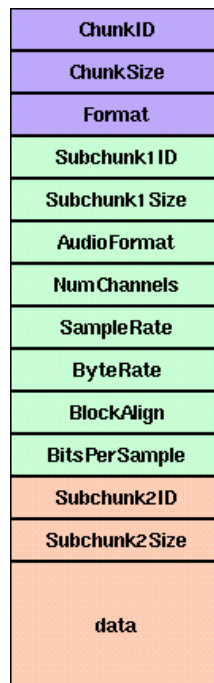


Figure 2.5.1. Data organization of a typical WAVE file [55]

Description of WAVE file data sections (figure 2.5.1) [55]:

- **ChunkID** - occupies 4 bytes and contains 4 characters, corresponding to the ASCII representation of the word “RIFF” (0x52494646 in hexadecimal).
- **ChunkSize** - occupies 4 bytes, and represents the size of all file in bytes, excluding the size of fields ChunkSize and ChunkID (8 bytes).
- **Format** - occupies 4 bytes and contains the ASCII representation of the word “WAVE” (0x57415645 in hexadecimal).
- **Subchunk1ID** - occupies 4 bytes and contains the ASCII representation of the word “fmt “ (0x666d7420 in hexadecimal).
- **Subchunk1Size** - occupies 4 bytes, and represents the size in bytes of Subchunk1 (green section in figure 2.5.1), excluding the size of fields Subchunk1Size and Subchunk1Size. Subchunk1 could have more fields than those presented in figure 2.5.1, although that is not the case of the files used in the implemented system.
- **AudioFormat** - occupies 2 bytes, indicates if the data is compressed or uncompressed (PCM), usually this field has a value of 1, indicating uncompressed LPCM encoding, values different from 1 indicate data compression. The implemented system only handles uncompressed data (LPCM), so the value of this variable is always 1.
- **NumChannels** - occupies 2 bytes and indicates the number of data channels the file has, usually 1 or 2 channels (a file with 1 channel is used, for example, for monophonic audio or single lead ECG, a file with 2 channels could be used for stereophonic audio or two lead ECG). The implemented system is a single lead ECG tester, so it accepts and creates files with 1 channel.
- **SampleRate** - occupies 4 bytes, and, as the name suggests, corresponds to the sample rate of the signal. In the implemented system this value is between 500 and 2000 (SPS), typically has a value of 1000 SPS.
- **ByteRate** - occupies 4 bytes and is given by the following expression:

$$ByteRate = SampleRate \times NumChannels \times \frac{BitsPerSample}{8} [byte/s]$$

- **BlockAlign** - occupies 2 bytes, represents the number of bytes per sample, including all channels, is given by the following expression:

$$BlockAlign = NumChannels \times \frac{BitsPerSample}{8} [byte/sample]$$

- **BitsPerSample** - occupies 2 bytes, and has the number suggests is the number of bits per sample (for one channel). The number of bits per sample in the WAVE files used on this system must be 16 bit, otherwise the test will not be performed.

- **Subchunk2ID** - occupies 4 bytes, and, usually, corresponds to the identifier of the data section (samples section), in this case the field contains the bytes corresponding to the ASCII representation of the word “data” (0x64617461 in hexadecimal).
- **Subchunk2Size** - occupies 4 bytes, and corresponds to the size of the file occupied by the waveform samples. It is given by the following formula, *NumSamples*, corresponds to the total number of samples the file contains and *FileDuration* corresponds to the total duration of the file in seconds:

$$\begin{aligned}
 \text{subChunk2Size} &= \text{NumSamples} \times \text{NumChannels} \times \frac{\text{BitsPerSample}}{8} = \\
 &= \text{FileDuration} \times \text{SampleRate} \times \text{NumChannels} \times \frac{\text{BitsPerSample}}{8} \text{ [byte]}
 \end{aligned}$$

- **data** - occupies Subchunk2Size bytes, and correspond to the waveform samples.

The byte ordering of RIFF files is little endian, except for the words represented in ASCII code, which have big endian byte ordering. The samples are stored as 2’s-complement signed integers, ranging from -32768 to 32767, in files with 16 bit (2 byte) samples. More than two subchunks might exist on some WAVE files, though this feature is not supported by the system. RIFF means *Resource Interchange File Format*. In figure 2.5.2, the first 64 bytes of the ECG waveform file (“ecg1.wav”), used for testing, are represented in hexadecimal [55].

```

52 49 46 46 3c 06 00 00 57 41 56 45 66 6d 74 20
10 00 00 00 01 00 01 00 e8 03 00 00 d0 07 00 00
02 00 10 00 64 61 74 61 18 06 00 00 b5 c3 e9 c3
19 c3 4d c3 81 c3 19 c3 b0 c2 14 c2 7c c2 81 c3

```

Figure 2.5.2. First 64 bytes of "ecg1.wav", ECG waveform file (obtained using Hex Editor Neo from HDD Software Limited)

Apart from the chunk and subchunk sizes, sample rate and byte rate, all ECG waveform files used in the implemented system must have a header similar to the one of “ecg1.wav”.

The total size of the ECG waveform file must not exceed 10 KB plus header (10284 bytes) and the total duration of the waveform must not exceed 2 seconds.

The WAVE ECG waveform files to be used in the implemented system should present the following header parameters (some parameters are intentionally omitted, like the parameters related to file size):

- **ChunkID** - "RIFF" (0x52494646)
- **Format** - "WAVE" (0x57415645).
- **Subchunk1ID** - "fmt " (0x666d7420).
- **AudioFormat** - 1 (0x0001)
- **NumChannels** - 1 (0x0001)
- **SampleRate** - from 500 to 2000 (0x000001F4 to 0x000007D0)
- **ByteRate** - from 1000 to 4000 (0x000003E8 to 0x00000FA0)
- **BlockAlign** - 2 (0x0002)
- **BitsPerSample** - 16 (0x0010)
- **Subchunk2ID** - "data" (0x64617461)

The WAVE file recorded by the system has a similar header, the only difference is in the subchunk and chunk sizes. The file has a maximum duration of 4 minutes, which corresponds to the maximum test duration.

2.5.4 USART Configuration

The microcontroller has to communicate with three devices using an SPI interface, the SD card, the signal generation integrated circuit (containing two DACs) and the ADC. The microcontroller (AT91SAM3X8E) features one SPI controller (with 4 hardware chip selects) and three USARTs with SPI mode.

The memory card is connected to the SPI controller, because it allows faster bitrates (in the case of the SD card, up to 21 MHz) and also because two open source libraries exist that allow SD card file operations using the SPI controller (SdFat and SPI). Due to the fact that the SD card operates in a different SPI mode, and the Arduino SPI library only allows the definition of the mode of operation once at the startup, only one of the devices operate properly, the SD card, the DAC or the ADC. Tests were performed, with two devices on the SPI bus, the DAC IC and the SD card, with different chip select signals and the two devices cannot operate at the same time, with some modifications in the code, the DAC does not operate, with others the SD card does not operate. To solve this problem, all devices feature an independent SPI interface, since the microcontroller only has one SPI controller, the USARTs are configured as SPI and a software defined chip select was implemented.

The **USART** (Universal Synchronous Asynchronous Receiver Transmitter) is a full-duplex universal synchronous and asynchronous serial interface. It is able to operate in SPI mode in the microcontroller used (AT91SAM3X8E), in master or slave mode, allowing mode selection and clock frequencies of up to $MCK/6$ (the master clock of the processor is 84 MHz, so the maximum frequency is 14 MHz), however, a hardware chip select must be implemented if the transfer of more than one byte is desired (the hardware chip select goes high every time a byte is sent). A block diagram of the USART is shown in figure 2.5.3 [56].

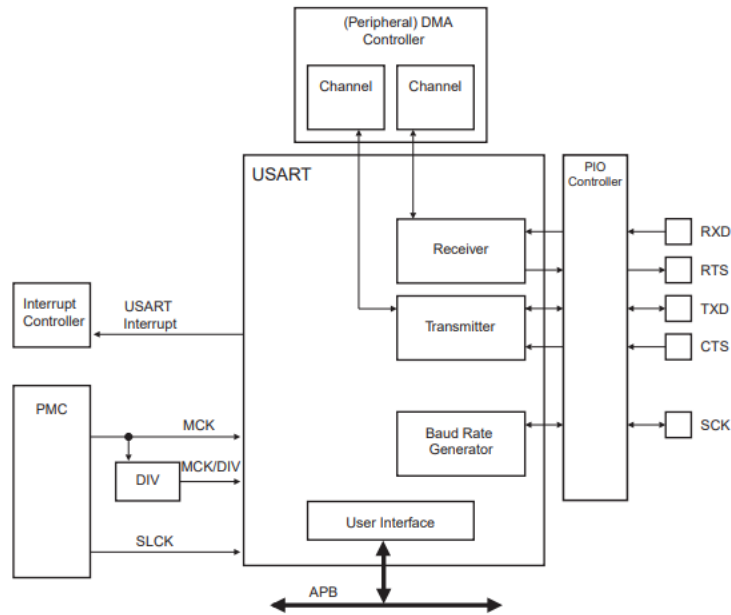


Figure 2.5.3. USART block diagram [56]

The input labeled RXD in figure 2.5.3 is connected to the receiver and in SPI mode (master mode) acts as the MISO, the output labeled RTS functions as chip select in SPI mode (master mode), the bidirectional pin TXD is connected to the transmitter and acts as the MOSI. The CTS input corresponds to the chip select in SPI slave mode. The bidirectional pin SCK is connected to the baud rate generator (which acts as clock generator), in SPI mode (master mode) performs the function the name suggests, corresponds to the slave clock [56].

The interface pins of the USART are multiplexed within the PIO (Peripheral Input Output) lines. The PIO must be programmed in order to assign the USART pins to their peripheral function. In table 2.3 the correspondence between USART and SPI signals are made, as well as the correspondence between the PIO I/O lines and the Arduino Due board pins, only the SPI master mode signals are shown.

Instance	USART Signal	SPI Signal	I/O line	Board Pin
USART0	RTS0	CS	PB25	2
USART0	RXD0	MISO	PA10	19 (RX1)
USART0	TXD0	MOSI	PA11	18 (TX1)
USART0	SCK0	SCK	PA17	70 (SDA1)
USART1	RTS1	CS	PA14	23
USART1	RXD1	MISO	PA12	17 (RX2)
USART1	TXD1	MOSI	PA13	16 (TX2)
USART1	SCK1	SCK	PA16	54 (A0)

Table 2.3. USART PIO I/O lines [adapted from 56 and 57]

The SPI devices which communicate with the USART, are connected to corresponding board pins (please refer to System's Mode of Operation for a schematic representation of USART-SPI connections). As previously mentioned the hardware chip select is not used. The ADC (operates in USART0) does not need a MOSI connection and the DAC IC does not need a MISO connection (operates in USART1), so these pins are left open.

The USART is not continuously clocked, the USART clock must be enabled in the Power Management Controller (PMC), before the USART can be used [56]. In order to enable the USART clock, Serial1 (USART0) and Serial2 (USART1) are initialized, as follows:

```
Serial1.begin(9600);
while (!Serial1);
Serial2.begin(9600);
while (!Serial2);
```

In order to define the desired SPI clock rate, the CD (clock divider) field of a USART register called US_BRGR (USART baud rate generator), must be defined [56]. The fields of this register are presented in figure 2.5.4. The FP field is called fractional part and is not necessary in SPI mode.

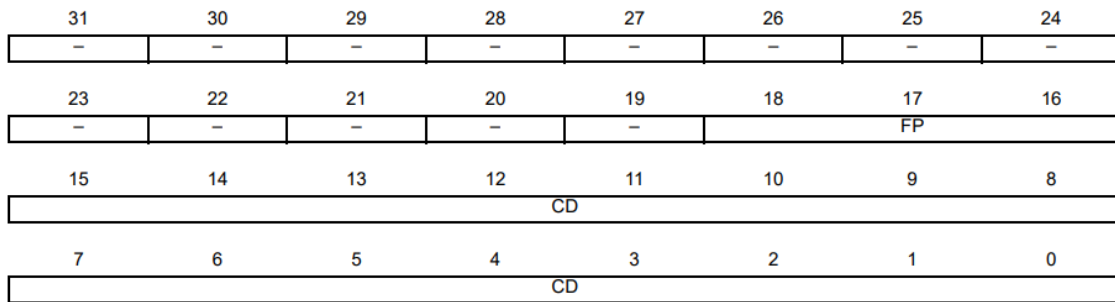


Figure 2.5.4. US_BRGR register fields [56]

When the USART operates in synchronous mode, like happens with SPI, the selected clock is divided by the field CD (clock divider) present in the US_BRGR (USART baud rate generator) register. The expression of the clock frequency is the following, the selected clock is $USCLKS = 0$, meaning $SelectedClock = MCK = 84\text{ MHz}$, CD is 10 [56]:

$$f_{SCK} = \frac{SelectedClock}{CD} = \frac{84 \times 10^6}{10} = 8.4\text{ MHz}$$

The clock frequency of the slave devices, ADC and DAC is 8.4 MHz (divider of 10). The maximum SPI clock in USART mode is 14 MHz. A block diagram of the baud rate generator is presented in figure 2.5.5.

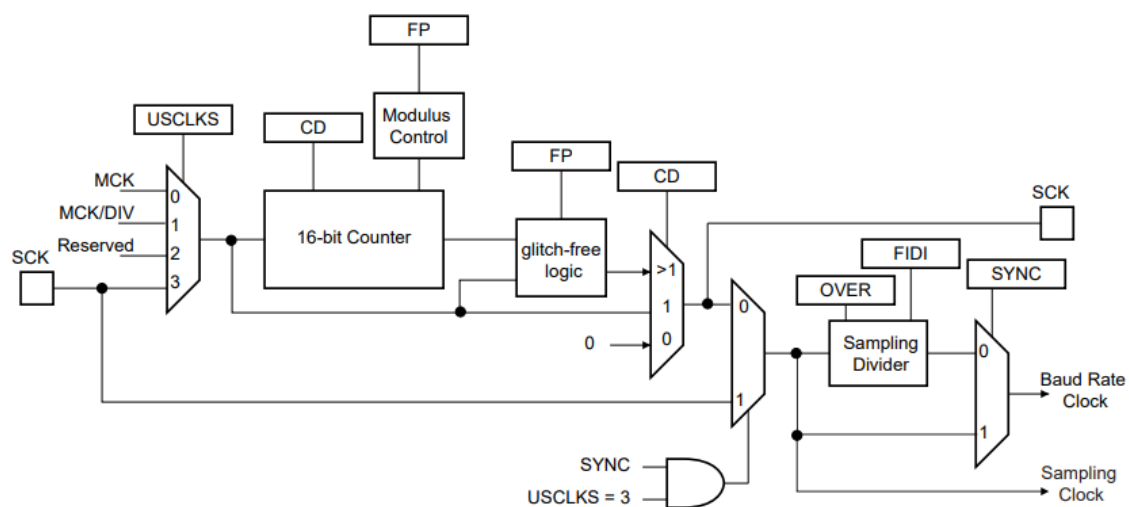


Figure 2.5.5. Block diagram of the USART baud rate generator (clock generator) [56]

In order to define the mode of operation of the USART as an SPI interface, the fields of a register called US_MR (USART Mode Register), must be set in accordance and the SPI mode must be defined. The fields of the US_MR register are presented in figure 2.5.6.

31	30	29	28	27	26	25	24
ONEBIT	MODSYNC	MAN	FILTER	–	MAX_ITERATION		
23	22	21	20	19	18	17	16
INVDATA	VAR_SYNC	DSNACK	INACK	OVER	CLKO	MODE9	MSBF/CPOL
15	14	13	12	11	10	9	8
CHMODE		NBSTOP			PAR		SYNC/CPHA
7	6	5	4	3	2	1	0
CHRL		USCLKS			USART_MODE		

Figure 2.5.6. US_MR register fields [56]

The fields are defined as follows, hexadecimal value between parentheses:

- USART_MODE - SPI master mode (0xE)
- USCLKS - Clock source MCK, master clock (0x0)
- CHRL - Character length 8 bits (0x3)
- SYNC/CPHA - SPI clock phase, 0 for modes 0 and 2, 1 for modes 1 and 3
- PAR - Parity type, none (0x4)
- NBSTOP - Number of stop bits, don't care, defined as 1 bit (0x0)
- CHMODE - Channel mode, normal (0x0)
- MSBF/CPOL - SPI clock polarity, 0 for modes 0 and 1, and 1 for modes 2 and 3
- MODE9 - 9 bit character length, value defined in CHRL (0x0)
- CLKO - Clock output select, the USART drives the SCK pin (0x1)
- OVER - Oversampling, don't care, defined as 16x (0x0)
- INACK - Inhibit non acknowledge, the NACK is generated (0x0)
- DSNACK - Disable successive NACK, defined as 0 (0x0)
- VAR_SYNC - don't care, defined as 0 (0x0)
- INVDATA - Inverted data, voltage polarity of data is inverted, disabled (0x0)
- MAX_ITERATION - don't care, defined as 0 (0x0)
- FILTER - Infrared receiver line filter, disabled (0x0)
- MAN - Manchester encoder/decoder, disabled (0x0)
- MODSYNC - Manchester synchronization mode, don't care, defined as 0 (0x0)
- ONEBIT - Start frame delimiter selector, don't care, defined as 0 (0x0)

Before writing to the US_MR (USART mode register), the write protection of this register must be removed by writing the WPKEY (Write Protect Key), its value is 0x555341 (“USA” in ASCII code), to the US_WPMR (USART Write Protect Mode Register), while setting the WPEN (Write Protect Enable) to 0 [56]. The fields of the US_WPMR are presented in figure 2.5.7.

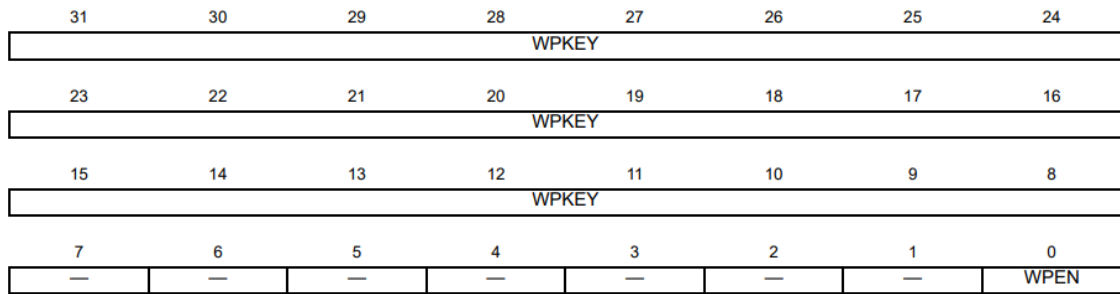


Figure 2.5.7. US_WPMR register fields [56]

The output pins must now be defined, this is performed by assigning the I/O lines to the peripheral functions, this action is performed by writing to the PIO_ABSR (PIO Peripheral AB select register). All I/O lines of USART0 and USART1 are assigned to peripheral A functions, with exception for SCK0 (USART0) that are assigned to a peripheral B function. The corresponding I/O line register field (that corresponds to an output pin on the board), is written with a 0 to assign a peripheral A function and 1 to assign a peripheral B function. The fields of PIO_ABSR (I/O lines) are shown in figure 2.5.8. The PIOA and PIOB I/O lines corresponding to the SPI pins must be assigned to the respective peripheral functions.

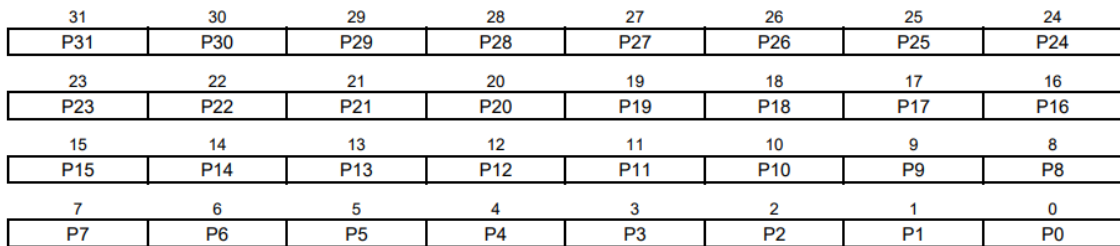


Figure 2.5.8. PIO_ABSR register fields [56]

After assigning the peripheral function, the PIO control must be disabled in order to enable peripheral control of the selected pin. To perform this action, the fields of PIO_PDR (PIO Controller PIO Disable Register) register must be written. To disable the PIO control (and enable peripheral control) of a pin, a 1 must be written in the corresponding field, writing a 0 will have no effect. After this action, the SPI pins are configured and ready for SPI operation. The fields of the PIO_PDR register are presented in figure 2.5.9. The PIOA and PIOB I/O lines corresponding to the SPI pins must have the PIO control disable (and consequently the peripheral control enabled, USART controls these pins).

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

Figure 2.5.9. PIO_PDR register fields [56]

In order to write to the PIO registers, the write protection must be removed. To remove write protection the field WPKEY (Write Protect Key) of PIO_WPMR (PIO Write Protect Mode Register) must be written with the value 0x50494F (“PIO” in ASCII code), and the WPEN (Write Protect Enable) flag must be set to 0. The fields of the PIO_WPMR register are shown in figure 2.5.10.

31	30	29	28	27	26	25	24
WPKEY							
23	22	21	20	19	18	17	16
WPKEY							
15	14	13	12	11	10	9	8
WPKEY							
7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	WPEN

Figure 2.5.10. PIO_WPMR register fields [56]

The sketch of code which configures USART as SPI is defined as follows (this code defines USART0 as SPI, the definition of USART1 is identical, only the variable name changes to USART1 and the I/O pin names are changed accordingly, the divider variable contains the value that is written to the CD field of the US_BRGR register, corresponding to the clock divider):

```

USART0->US_WPMR = 0x55534100; // Unlock the USART Mode register

if (mode == 1)
    USART0->US_MR |= 0x409CE;
else if (mode == 2)
    USART0->US_MR |= 0x508CE;
else if (mode == 3)
    USART0->US_MR |= 0x509CE;
else
    USART0->US_MR |= 0x408CE;
if (divider < 6)
    USART0->US_BRGR = 6;
else
    USART0->US_BRGR = divider;

PIOA->PIO_WPMR = 0x50494F00; // Unlock PIOA Write Protect Mode Register
PIOB->PIO_WPMR = 0x50494F00; // Unlock PIOB Write Protect Mode Register
PIOB->PIO_ABSR |= (0u << 25); // CS: Assign B25 I/O to the Peripheral A function
PIOB->PIO_PDR |= (1u << 25); // CS: Disable PIO control, enable peripheral control
PIOA->PIO_ABSR |= (1u << 17); // SCK: Assign PA17 I/O to the Peripheral B function
PIOA->PIO_PDR |= (1u << 17); // SCK: Disable PIO control, enable peripheral control
PIOA->PIO_ABSR |= (0u << 10); // MISO: Assign PA10 I/O to the Peripheral A function
PIOA->PIO_PDR |= (1u << 10); // MISO: Disable PIO control, enable peripheral control
PIOA->PIO_ABSR |= (0u << 11); // MOSI: Assign PA11 I/O to the Peripheral A function
PIOA->PIO_PDR |= (1u << 11); // MOSI: Disable PIO control, enable peripheral control

```

Software Defined Chip Select (CS)

The USART when configured as SPI generates a chip select signal (CS), however, in the way the signal is generated it only allows the transfer of one byte. The signal goes high after eight bits are sent, devices that require the CS to remain low during larger transfers (for example 2, 3 or 4 bytes) would not operate. To counteract this problem a software defined chip selected was implemented, but, due to the fact that the digital write function of Arduino library is slow (takes about 4 to 5 microseconds to complete) and the interrupt routines (used in signal generation) must be as quick as possible, a faster digital write was implemented (this version of digital write takes less than 1 microsecond to complete).

In order to perform a fast digital, at first the registers must be functioning properly and the write protection must be disabled, in order to do so, the pin is defined as a digital output and the logic level is set to high (the value CS presents in idle) by performing a “normal” digital write, like presented in the code (the CS variable corresponds to the pin number in Arduino Due board assigned for the CS function):

```
pinMode(CS, OUTPUT);
digitalWrite(CS, HIGH);
```

After the desired I/O is initialized, the digital values can be assigned during the execution of DAC and ADC routines. In order to set a pin to the low logic level, the corresponding field of PIO_CODR (PIO Controller Clear Output Data Register) register must be set to 1. The remaining bit fields are set to 0. The fields of PIO_CODR are shown in figure 2.5.11.

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

Figure 2.5.11. PIO_CODR register fields [56]

In order to set a pin to the high logic level, the corresponding field of a register called PIO_SODR (PIO Controller Set Output Data Register) must be set to 1. The remaining fields are set to 0. The fields of PIO_SODR register are identical to the fields of PIO_CODR represented in figure 2.5.11. The function to implement the fast digital write is defined as follows:

```
inline void fastDigitalWrite(int pin, boolean val) {
    if (val) g_APinDescription[pin].pPort -> PIO_SODR = g_APinDescription[pin].ulPin;
    else g_APinDescription[pin].pPort -> PIO_CODR = g_APinDescription[pin].ulPin;
}
```

In the digital write function, pin corresponds to the Arduino Due board pin number, val corresponds to the logic level of the pin, false means low, true means high, g_APinDescription[pin].pPort is a struct array parameter which returns the corresponding PIO (for example PIOA, PIOB, ...) of the Arduino Due board, g_APinDescription[pin].ulPin is a struct array parameter which returns the corresponding microcontroller pin number.

Write Samples to the DAC

In order to provide samples to the ECG signal generation DAC integrated circuit (DAC8552), the SPI timing characteristics of the device must be respected. First the chip select signal (CS) must be set low, then three bytes of data are sent consecutively (24 bits) by the microcontroller, containing a control byte (which, for example, defines if the samples are intended to DACA or DACB) and two data (sample) bytes (16 bits). After the transfer is completed the microcontroller releases the DAC by setting the CS high.

The data that is transferred to the MOSI line must be written in a register called US_THR (USART Transmit Holding Register). This register has two fields, TXCHR (character to be transmitted), that has 9 bits (only 8 bits are used in the mode defined), and holds the data to be transmitted to the MOSI line, and TXSYNH (synch field to be transmitted) that are not used and set to zero. In order to send the three bytes required by the DAC, this register is written three times, each time a sample is transferred. The fields of US_THR are shown in figure 2.5.12.

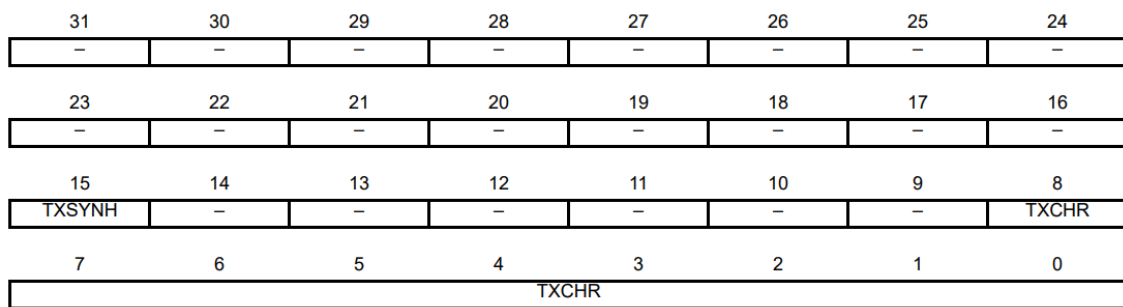


Figure 2.5.12. US_THR register fields [56]

To guarantee all data is sent in the appropriate timing, to avoid data corruption, it is necessary to check if the byte in the transmitter register as already been sent. A register called US_CSR (USART Channel Status Register) holds the flags which indicate the current transmission state. Two fields must be checked, the fields TXRDY (Transmitter Ready) and TXEMPTY (Transmitter Empty). The TXRDY flag, when active (1) indicates there is no character in US_THR. The TXEMPTY flag, when active (1) indicates there are no characters in US_THR, nor in the Transmit Shift Register. TXRDY is read from US_CSR and is needed to check if US_THR can be written (is used to check transmitter availability before the second and third byte transfers). TXEMPTY is checked after the last transfer to verify if the Transmit Shift Register is empty (if the DAC received all data), when this flag sets to one, the CS line is set to high level. The US_CSR register fields are shown in figure 2.5.13.

31	30	29	28	27	26	25	24
–	–	LINSNRE	LINCE	LINPE	LINISFE	LINBE	MANERR
23	22	21	20	19	18	17	16
CTS/LINBLS	–	–	–	CTSIC	–	–	–
15	14	13	12	11	10	9	8
LINTC	LINID	NACK/LINBK	RXBUFF	TXBUFE	ITER/UNRE	TXEMPTY	TIMEOUT
7	6	5	4	3	2	1	0
PARE	FRAME	OVRE	ENDTX	ENDRX	RXBRK	TXRDY	RXRDY

Figure 2.5.13. US_CSR register fields [56]

The (simplified) DAC write function has the following code (value corresponds to the sample, a 16 bit unsigned integer, nDAC corresponds to the selected DAC within the DAC IC, 0 is A and 1 is B, and CS corresponds to the chip select, a digital output pin on the Arduino Due board):

```
volatile byte msg3 = byte(value); // least significant byte of value
volatile byte msg2 = byte(value >> 8); // most significant byte of value
volatile byte msg1 = 0x00; // command
if (nDAC == 1) // nDAC selection
    msg1 = 0x24; // Command for nDAC = 1
else if (nDAC == 0)
    msg1 = 0x10; // Command for nDAC = 0
fastDigitalWrite(CS, LOW); // set CS pin LOW (begin SPI transfer)
USART1->US_THR = msg1; // send first byte
while (!(USART1->US_CSR & 0x2)); // check txrdy before sending the second byte
USART1->US_THR = msg2; // send second byte
while (!(USART1->US_CSR & 0x2)); // check txrdy before sending the third byte
USART1->US_THR = msg3; // send third byte
while (!(USART1->US_CSR & 0x200)); // check txempty before setting CS HIGH
fastDigitalWrite(CS, HIGH); // set CS pin HIGH (end SPI transfer)
```

Read Samples from the ADC

To read samples from the ADC (ADS8339), an USART SPI interface is used. The ADC sends two bytes (16 bits) containing the sample. In order to request data from the ADC, the microcontroller sets the chip select signal (CS) low (also activating ADC's sample acquisition mode). Then a dummy write is performed to generate the necessary clocks to receive a byte of data from the ADC, the procedure is repeated two times more in order to receive the second and last byte of samples. After receiving all bits, the microcontroller sets the CS high (to put the ADC in conversion mode and to end the SPI transfer).

The dummy data is written to the US_THR register, and its value is not important (defined as 0xFF). The ADC data is received in a register called US_RHR (USART Receive Holding Register), the fields of this register are RXCHR (Received Character) and RXSYNH (Received Synch). RXCHR contains the received byte (from the ADC) and RXSYNH value is not important (reads as 0). The field of the US_RHR register are presented in figure 2.5.14.

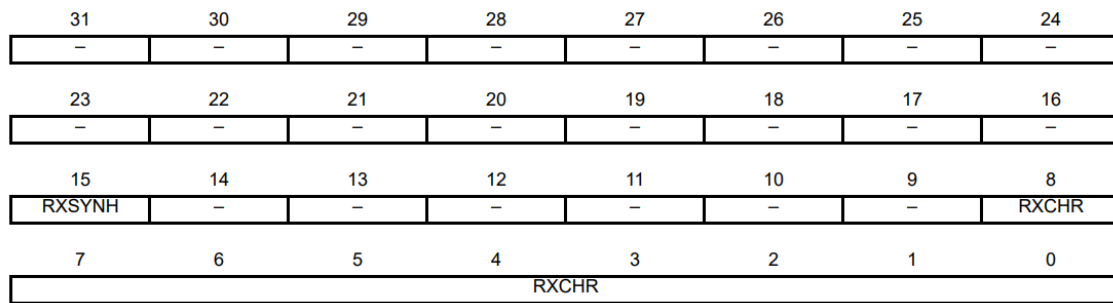


Figure 2.5.14. US_RHR register fields [56]

To guarantee all data is received in the appropriate timing, and to avoid data corruption, it is necessary to check if a complete character has been received, and if the dummy character as completed its transmission, providing all necessary clocks. The US_CSR (USART Channel Status Register) register (figure 2.5.13) has two important flags, RXRDY (Receiver Ready) and TXRDY (transmitter ready). RXRDY, when active (1), indicates at least one complete character (byte) has been received and US_RHR has not yet been read. TXRDY, when active (1), indicates US_THR is empty. The first flag (RXRDY) is read from US_CSR and checked before US_RHR is read, to check if the byte from the ADC has already been written in the register (US_RHR). The second flag (TXRDY) is read from US_CSR and checked before each dummy transmitter hold register (US_THR) write is performed.

The (simplified) ADC read function has the following code (returnValue corresponds to the sample received from the DAC, the return value of ADC read function and CS corresponds to the digital output pin of the Arduino Due board which provides the chip select signal to the ADC):

```
volatile uint16_t returnValue = 0;
volatile byte msg1 = 0;
volatile byte msg2 = 0;
fastDigitalWrite(CS, LOW); // set CS pin LOW (begin SPI transfer)
while (!(USART0->US_CSR & 0x2)); // check txrdy before sending a byte
USART0->US_THR = 0xFF; // send a byte
while (!(USART0->US_CSR & 0x1)); // check rxrdy before receiving a byte
msg1 = USART0->US_RHR; // receive a byte
while (!(USART0->US_CSR & 0x2)); // check txrdy before sending a byte
USART0->US_THR = 0xFF; // send a byte
while (!(USART0->US_CSR & 0x1)); // check rxrdy before receiving a byte
msg2 = USART0->US_RHR; // receive a byte
fastDigitalWrite(CS, HIGH); // set CS pin HIGH (end SPI transfer)
returnValue = (msg1 << 8) | msg2;
```

2.5.5 Signal Generation

The implemented system features two methods of signal generation, sample based and real time. The only sample based signal the system generates is the ECG signal, and even this signal has other signals added. The real time signals are generated using mathematic expressions or functions (sinewave, triangle wave, sawtooth wave and square wave) and are composed of samples generated in real time (there is no buffer or file to contain predefined samples). The real time signals are used to control the variable impedance circuits (resistance and capacitance) and to add common-mode and differential interference to the ECG signal (sinewaves only).

ECG Signal Generation

The ECG signal is generated with samples contained in the data section of the waveform (WAVE) file stored in the memory card. At startup the microcontroller reads the waveform file (containing one period of the ECG signal) and loads the samples to a buffer (stored in RAM), it also reads the test file and sets the parameters of the test array of structs.

During the test, the buffer is read at the sample rate defined in the waveform file, inside a timer interrupt routine associated with the DAC, the buffer is circular, when it reaches the end, it starts again from the beginning. Inside the interrupt routine the samples for the two ECG components, differential and common mode, are generated. The differential mode corresponds to the sample from the buffer (ECG waveform) added to an offset and a sinewave interference signal. The common-mode corresponds to a DC component (offset) added to a sinewave interference signal. The code to generate the ECG samples (inside the timer interrupt routine) is defined as follows:

```
dac0Value = sineCMGenerator();
dac1Value = (*runningPTR) / ecgAtt + sineDiffGenerator();
writeToDAC0_USART1(CS1, dac0Value);
writeToDAC1_USART1(CS1, dac1Value);
++runningPTR;
if (runningPTR >= lastPTR)
    runningPTR = bufferPTR;
```

sineCMGenerator() and sineDiffGenerator() are the interference plus DC component, generation functions, of the ECG common-mode and differential mode components, respectively. The DAC writing functions are modified versions, which write directly to DAC 0 (A) or DAC 1 (B), through USART1, these functions are optimized for faster execution. runningPTR is the pointer to the current position of the buffer, lastPTR corresponds to the first position of the buffer added to the size of the buffer, bufferPTR (or buffer pointer) is a pointer to the first position (address) of the buffer.

The sinewave interference signals and offset added to the common-mode and differential components of the ECG signal are defined in the functions sineCMGenerator() and sineDiffGenerator(). The sineCMGenerator function is defined as follows:

```
uint16_t sineCMGenerator() {
    volatile double sineCMWaveDouble = sineCMOffsetInt + sineCMAmpInt * sin(2.0 * 3.1416 *
sineCMFreq * (double(sineCMSampleCounter++) / double(sampleRate)));
    if (sineCMSampleCounter >= NCM)
        sineCMSampleCounter = 0;
    return uint16_t(sineCMWaveDouble);
}
```

sineCMOffsetInt corresponds to the DC component (offset) of the common-mode component of the ECG signal (in the DAC unsigned integer format), sineCMAmp corresponds to the sinewave amplitude (in the DAC unsigned integer format), sineCMFreq is a floating point value (double) which defines the sinewave frequency (in Hertz). sampleRate corresponds to the sampleRate of the ECG waveform signal (in samples per second), NCM is the number of samples required to define one period of the sinewave signal. The sineDiffGenerator() function is identical and uses independent parameters (for example, sineDiffOffsetInt, sineDiffAmpInt, sineDiffFreq, NDiff,...).

Variable Impedance Signal Generation

The variable impedance circuits, for capacitance and resistance simulation, can be controlled by a constant value, a square wave, a sawtooth wave, a sinewave or a triangle wave. The sampling frequency of the variable impedance signals is 100 Hz. The sinewave generation is performed by functions identical to sineCMGenerator() (for more information, please refer to the previous subsection, entitled ECG Signal Generation), the only difference lies in the fact that the value is written to the DAC or digital potentiometer inside the function. The constant value is very simple to generate, because it can be directly loaded to the DAC (variable capacitance) or digital potentiometer (variable resistance). The function to set a constant value to the capacitance C1 is defined as follows:

```
void constGenC1() {
    dac0ValueC = constValueC1Int;
    I2CDACWrite(dac0AddrC, dac0ValueC);
}
```

constValueC1Int is the constant value in the unsigned integer DAC format, dac0AddrC is the address of the capacitance control DAC 0 (13). The C2 function is similar, but with a different DAC address (dac1AddrC, 14) and independent parameters (for example, dac1ValueC and constValueC2Int).

To generate a constant resistance value, the function is similar, only the function to write the value differs:

```
void constGenR1() {
    pot0Value = constValueR1Int;
    setResValue(pot0Value, false);
}
```

The function to set the potentiometer value has two parameters, the potentiometer value (pot0Value for potentiometer 1, pot1Value, for potentiometer 2), an unsigned integer with one byte (8 bits) which defines the resistance value, and a second parameter, a boolean variable, that indicates the destination of the value (false, potentiometer 1, true, potentiometer 2).

Square wave signals may also be generated, to define this signals, the maximum and minimum values must be defined, as well as the frequency (or in this case the number of samples per period). The signal holds the maximum value for half period, than minimum value for another half period. After a complete period the sample counter is reset and the process repeats. To generate a square wave the following function is defined:

```
void squareWaveGenC1() {
    if (xC1 < (NC1 >> 1) - 1) {
        dac0ValueC = maxValueC1Int;
        I2CDACWrite(dac0AddrC, dac0ValueC);
    }
    else {
        dac0ValueC = minValueC1Int;
        I2CDACWrite(dac0AddrC, dac0ValueC);
    }
    ++xC1;
    if (xC1 >= NC1)
        xC1 = 0;
}
```

maxValueC1Int is the maximum value (in the unsigned integer DAC format), minValueC1Int is the minimum value (in the unsigned integer DAC format), xC1 is the sample count, NC1 is the number of samples per period. The functions to generate a square wave for C2 variable capacitance is similar, but with independent variables. The functions to generate a square wave for variable resistance control are similar but with independent variables and a different write function (setResValue). This applies to the other time varying functions, triangular, sawtooth and sinewave.

In order to generate a sawtooth wave, a different approach must be taken, the sawtooth consists of a line with a positive or a negative slope, that returns abruptly (ideally with infinite slope), to its maximum or minimum value (it had initially), in the end of a period. The slope-intercept form could be used to determine the line expression:

$$y = mx + b = \frac{max - min}{N - 1} \times x + min$$

In the expression *max* corresponds to the maximum value of the sawtooth wave, *min* is the minimum value of the sawtooth wave, *N* is the number of samples per period and *x* is the sample count. For a negative slope the expression must be modified to:

$$y = mx + b = \frac{min - max}{N - 1} \times x + max$$

The sample counter must be reset each time a period of signal samples are generated (to make the abrupt transition of the function to its initial value).

The following function was defined for sawtooth wave generation:

```
void sawtoothWaveGenC1(bool posSlope) {
    if (posSlope) {
        yC1 = (maxValueC1Int - minValueC1Int) * (double(xC1) / double(NC1 - 1)) +
minValueC1Int;
        dac0ValueC = uint16_t(yC1);
        I2CDACWrite(dac0AddrC, dac0ValueC);
        ++xC1;
        if (xC1 >= NC1)
            xC1 = 0;
    }
    else {
        yC1 = double(minValueC1Int - maxValueC1Int) * (double(xC1) / double(NC1 - 1)) +
maxValueC1Int;
        dac0ValueC = uint16_t(yC1);
        I2CDACWrite(dac0AddrC, dac0ValueC);
        ++xC1;
        if (xC1 >= NC1)
            xC1 = 0;
    }
}
```

posSlope a boolean variable which indicates the slope sign of the sawtooth wave, if true, the slope is positive, otherwise, the slope is negative. The other parameters have the same meaning as in the square wave function (covered in the previous page).

A triangle wave consists of a sloped line, which changes the slope sign each time a maximum or minimum value is reached. In the time (horizontal) axis the distance between consecutive maximum and minimum values corresponds to half period of the wave, and the distance between consecutive maximums or minimums corresponds to the period of the wave.

After each half period the slope is inverted, by inverting the direction of the count, for example, if x is being incremented, it is now decremented, and vice-versa. The slope expression is modified, assuming that after half period of decrementation, x is set to 1, and is defined to $\frac{N}{2} - 2$, after half a period of incrementation:

$$y = mx + b = \frac{\max - \min}{\frac{N}{2} - 1} \times x + \min$$

The function to generate a triangle wave is defined as follows:

```
void triangleWaveGenC1() {
    yC1 = (maxValueC1Int - minValueC1Int) * (double(xC1) / double((NC1 >> 1) - 1)) +
    minValueC1Int;
    dac0ValueC = uint16_t(yC1);
    I2CDACWrite(dac0AddrC, dac0ValueC);
    if (up_n_downC1) {
        ++xC1;
        if (xC1 >= (NC1 >> 1)) {
            xC1 = (NC1 >> 1) - 2;
            up_n_downC1 = false;
        }
    }
    else {
        --xC1;
        if (xC1 < 0) {
            xC1 = 1;
            up_n_downC1 = true;
        }
    }
}
```

The parameters are all the same as in the sawtooth and square wave functions, except for $xC1$, that is a increment/decrement counter that counts half a period instead of a period, like happens with other wave types. up_n_downC1 is a boolean variable, which indicates the counting direction (false means decrementing, true means incrementing).

All impedance variation functions, have a similar definition, the only differences are in the name of the global variables that instead of having C1, have C2, R1 or R2 (and are fully independent of each other). The address parameter of the I2CDACWrite function is different for C1 and C2 (dac0AddrC, 13, dac1AddrC, 14), as well as the DAC voltage global variable dac0ValueC (C1) and dac1ValueC (C2), because the signal is generated by two independent (I2C) DACs.

The function to define resistance, as previously mentioned, is different, as it accepts an eight bit value (unsigned integer with 8 bits) which defines the resistance (and not the voltage output of a DAC) between the wiper and the other potentiometer terminal.

The global variables that hold the potentiometer values are pot0Value (R1) and pot1Value (R2). Another parameter of this function exists, a boolean variable which defines the destination of the value, potentiometer 1 (R1) or 2 (R2) (both are part of the same IC, so a parameter for an I2C address is unnecessary).

2.5.6 Signal Recording

To record the signal samples from the ADC, a WAVE file is created at the startup, the file is stored in the memory card, and its filename plus extension is “REC.WAV”. If a previous recording file is present, the existing file is overwritten. The header of the file is similar to the header of the waveform file (covered in the WAVE Files subsection), though it is generated in an independent code section.

During the test, the voltage output of the ECG Front End (DUT) is recorded in the test file with samples provided by the ADC (ADS8339). A timer interrupt guarantees the ADC samples are requested at the required sample rate (the same as defined in the ECG waveform file). The samples from the ADC (16 bit unsigned integer) are converted to the appropriate WAVE file format (16 bit signed integer) and stored in a buffer (RAM), this buffer is transferred to the SD card in a loop (in the normal code routine, outside the interrupt cycle). The recording loop controls the test duration, when the required amount of samples is achieved (subchunk2Size, refer to the WAVE Files subsection), the recording file is closed, the timers are stopped and the test ends. The code of the ADC interrupt routine is defined as follows:

```
void wavWriteADC() {
    adcValue = readADC(CS_ADC, usart_adc);
    sample = adcValue - adc_midpoint;
    *recRunningPTR = sample;
    ++recRunningPTR;

    if (recRunningPTR >= recLastPTR)
        recRunningPTR = recBufferPTR;
}
```

readADC(CS_ADC, usart_adc) is the ADC read function, CS_ADC is an unsigned integer that corresponds to the Arduino Due board pin, which generates the ADC chip select signal. usart_adc, corresponds to the number of the USART the microcontroller uses to communicate with the ADC, in this case the value is 0 (USART0). adc_midpoint corresponds to the midpoint value of the ADCs voltage sampling range (has a value of 32768 in a 16 bit DAC). recRunningPTR is the pointer to the current recording buffer position, recLastPTR corresponds to the first position of the recording buffer plus the size of the recording buffer, recBufferPTR corresponds to the first position of the recording buffer. When recRunningPTR reaches the last position it is set to the first position again (circular buffer).

The cycle which writes the ADC samples in the recording file is defined as follows:

```
void writeWavADC() {
    recCounter = 0;
    while (recCounter < recSubChunk2Size) {
        if (recRunningPTR != recNextPTR) {
            recSamplesBuffer[0] = byte(*recNextPTR);
            recSamplesBuffer[1] = byte(*recNextPTR >> 8);
            recDataFile.write(recSamplesBuffer, 2);
            ++recNextPTR;
            recCounter += 2;
            if (recNextPTR >= recLastPTR)
                recNextPTR = recBufferPTR;
        }
    }
    recDataFile.close();
    Timer0.stop();
    Timer1.stop();
    Timer2.stop();
    Timer3.stop();
    Timer4.stop();
    free(recBufferPTR);
    free(bufferPTR);
}
```

recCounter is a long which corresponds to the byte counter of the recording file, recSubChunk2Size is the total size of the recording file (for the configured test duration). recDataFile.write(recSamplesBuffer, 2) is a function from SdFat library, in this example the function writes two bytes of samples (a 16 bit sample), from the auxiliary array (recSamplesBuffer) to the recording file. The current position of the recording buffer is set to the beginning when it reaches the end. The last eight lines of code, correspond to the file close (recDataFile.close()), stop the timers (and respective interrupt generation, Timer0.stop(), Timer1.stop(), ...) and free the memory buffers for reading and recording (free(recBufferPTR), free(bufferPTR)).

2.5.7 Test Read

The test array of structs stores the parameter changes over time. A timer interrupt is associated with test changes, this timer as a frequency of 1 Hz. The test time elapsed is counted and compared with the timestamp of the current index of test struct array, when this time matches, the changes are performed in a separate function. The parameter change function, checks the “Change” boolean variables for each test function and then performs the changes by assigning the values to the global test variables from the test struct. The lead-off test does not require a global variable, since the digital output pin values can be assigned inside the parameter change function.

The interrupt function associated with the test timer is defined as follows (executes every 1 second during the test):

```
void runTest() {
    if (tCounter < testDuration) {
        if (tCounter == testArray[testIndex].timeStamp) {
            readTestSequence();
            ++testIndex;
        }
        ++tCounter;
    }
    else {
        Timer0.stop();
        Timer1.stop();
        Timer2.stop();
        Timer3.stop();
        Timer4.stop();
        free(recBufferPTR);
        free(bufferPTR);
        recDataFile.close();
    }
}
```

testDuration is an unsigned integer which corresponds to the total test duration in seconds, tCounter is the variable that counts the elapsed test time in seconds, readTestSequence() is a void function which reads the test struct in the current test array position and performs the necessary changes to the global (test) variables. testIndex is the index of the array of structs. The “else” condition is included to interrupt the test at the defined time in the case of an SD card malfunction, which can hold the recording loop, or cause a significant amount of sample loss.

2.5.8 Main Sequence

At system startup, the output digital pins are assigned to their initial values, the SD card is initialized and the waveform and recording files are opened, for reading and writing, respectively. The header of the waveform file is read to check if the parameters are in accordance with the specifications, if the verification fails the execution of code is ended, if the file passes the verification the execution continues. The test file is read and verified, if the file passes the verification, the code resumes execution, otherwise, halts it. In the next step, all interfaces and devices are initialized, the waveform file data section is read, and the samples transferred to the reading buffer (in RAM), the waveform file is closed. If the file is properly read and closed, the test resumes, otherwise, it halts. The Arduino board LED turns on (test recording LED), the header of the recording file is written, the recording buffer initialized, the timers start, starting the test, and the samples from the ADC begin being recorded.

The test runs until the time elapsed reaches the test duration, the test ends and the LED is turned off. If something is wrong with the SD card, the waveform or test file(s), the test is aborted and LED does not turn on. To start the test the user must check all connections and if the SD card is properly inserted, connect the powerbanks, and press the Arduino Due board reset button (red round button),.

2.6 Simulations

The SPICE (Simulation Program with Integrated Circuit Emphasis) is of vital importance in an electronics project, because it provides the designer a platform to design and simulate electronic circuits and assess its performance and functionality, without the need of a physical circuit, reducing the development costs. SPICE also includes an accurate integrated circuit and electronic components library that allows the realization of a vast set of analysis, some may even be impractical to perform with real circuits while others may require very expensive test equipment.

During the development phase of the project a vast set of SPICE simulations was performed, some may have been omitted. The most relevant simulation results are presented in this section.

2.6.1 Fully Differential Amplifier and Signal Attenuator

The fully differential amplifier is the element of the circuit responsible for the conversion of the single-ended components of the ECG signal (common-mode and differential) into a differential ECG signal. In figure 2.6.1, the schematic of the circuit used in the fully differential amplifier simulations is presented.

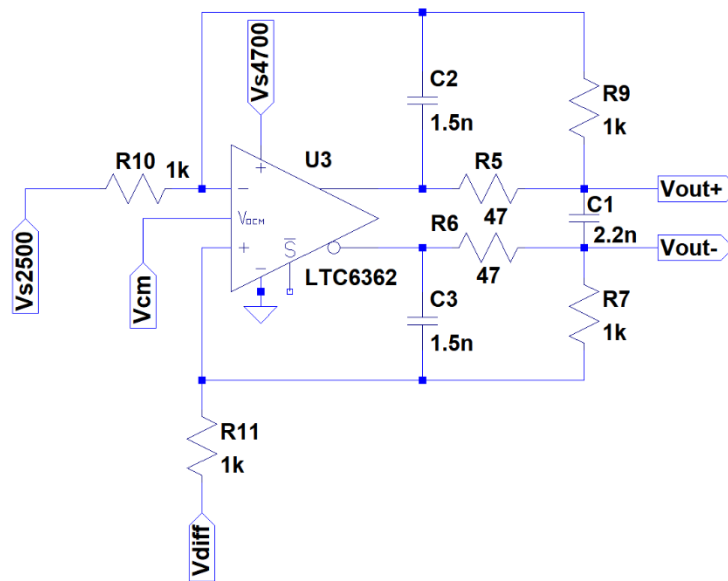


Figure 2.6.1. Schematic of the fully differential amplifier circuit used in simulations

The signal attenuator is the element of the circuit responsible for the attenuation of the signal from the fully differential amplifier. The signal is attenuated because the ECG front end accepts differential signals, with amplitudes in the order of hundreds of microvolt (μV) or millivolt (1-5 mV), and will saturate with higher amplitude signals.

Only the differential component of the ECG signal is attenuated, the common-mode remains at the same level. The schematic of the circuit used in the simulations is shown in figure 2.6.2.

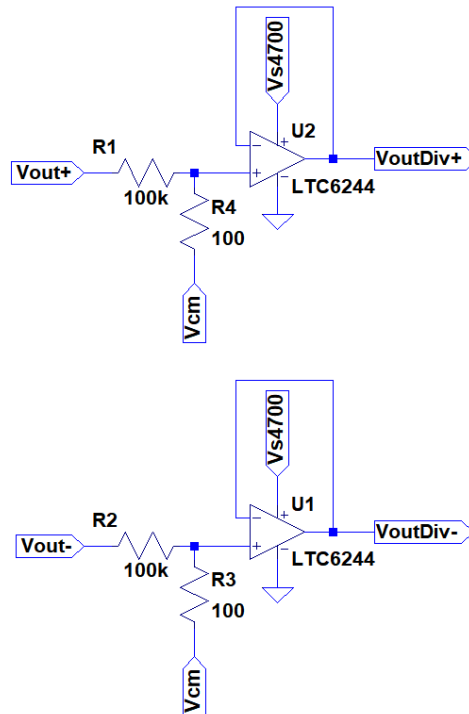


Figure 2.6.2. Schematic of the attenuator circuit used in simulations

AC Analysis

An AC analysis was performed to obtain the frequency response of the fully differential amplifier. This analysis is also useful to check for signs of high frequency instabilities that could lead to oscillations and unpredictable behavior of the amplifier.

The attenuator circuit's AC analysis was not performed, because the operational amplifier used (OPA2350) is unity gain stable and also because the amplifier is a simple unity gain voltage follower, and does not have any filter circuits. And also, because LTSPice, the SPICE used, does not have the model of the opamp incorporated in the circuit.

The frequency response of the differential amplifier (Bode plot) is presented in figure 2.6.3.

The circuit is simulated with an AC source with unity amplitude and zero phase connected to the node labeled Vdiff (see figure 2.6.1), the other terminal of the source is connected to the potential labeled Vs2500 (supply midpoint).

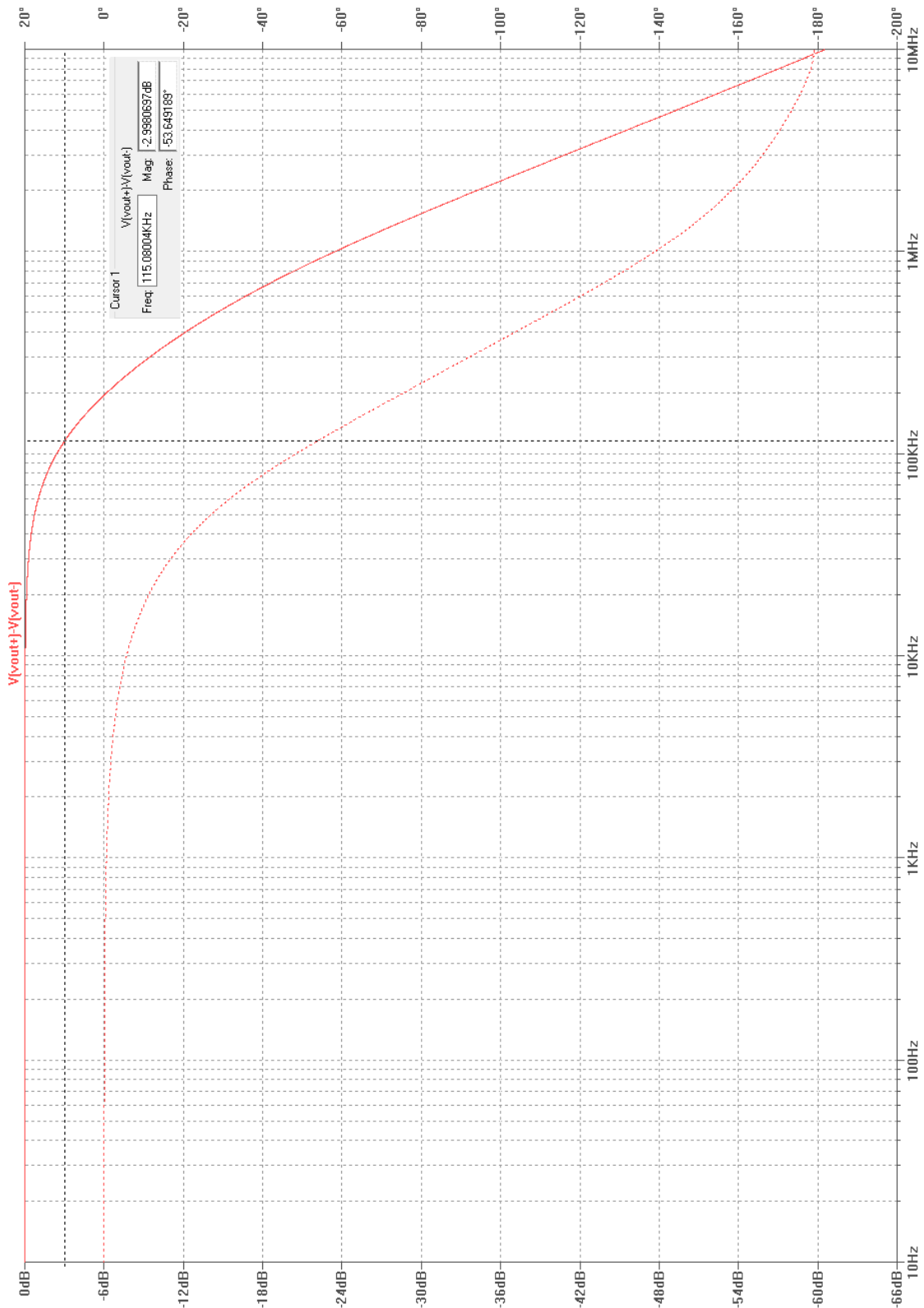


Figure 2.6.3. Frequency response of the fully differential amplifier

The fully differential amplifier circuit behaves as a low pass filter with a cut-off frequency of about 115 kHz. The bandwidth of the circuit is adequate for the application, the frequencies of interest of the signal (0.01 Hz to 100 Hz) do not suffer attenuation, and the phase shift is close to zero.

Transient Analysis

Time domain analysis were also performed, in order to check if the signals are generated as required. Two analysis were performed, common-mode analysis and differential analysis.

In common mode analysis a signal generator is connected to the common-mode input of the differential amplifier (labeled V_{cm} in figure 2.6.1). The signal used in the common-mode analysis is a 50 Hz sinewave with an amplitude of 0.1 V (simulating the mains interference signal, added to the common mode component of the ECG signal, with exaggerated amplitude) with a DC component of about 2.505 V (approximately the supply midpoint, the “virtual ground”). The common-mode signal should appear at both outputs of the attenuator with the same characteristics as in the input (with the same DC component, amplitude, frequency and phase).

To perform a differential analysis a signal generator is connected to the differential input of the amplifier, labeled V_{diff} (figure 2.6.1), the other terminal of the generator is connected to the supply midpoint, labeled V_{s2500} (figure 2.6.1). The signal used to test the differential component of the signal is similar to the signals generated by ECG test equipment to test QRS (or R wave) detection. It consists of a triangular pulse with an amplitude of 1 V, a width of 0.1 seconds and a frequency of 1 Hz (60 BPM). The differential signal should be present at the differential output of the attenuator with an amplitude a thousand times inferior.

The results of the transient analysis are presented in figures 2.6.4 and 2.6.5. Figure 2.6.4 represents the common-mode signal at the positive output of the attenuator (the negative output of the attenuator has the same common-mode signal, so, it was omitted in the analysis), figure 2.6.5 represents the differential signal at the output of the attenuator.

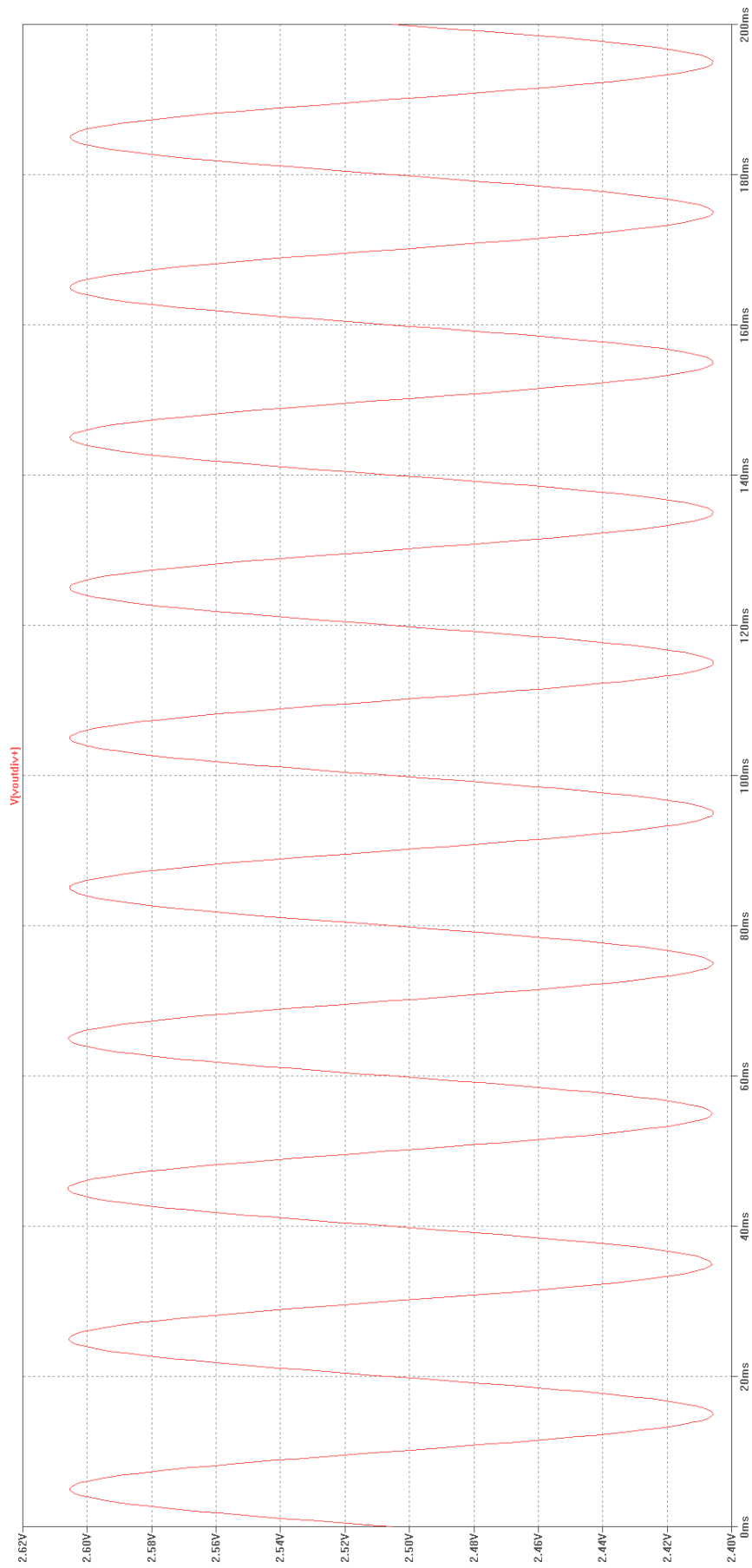


Figure 2.6.4. Common-mode signal at the output of the attenuator

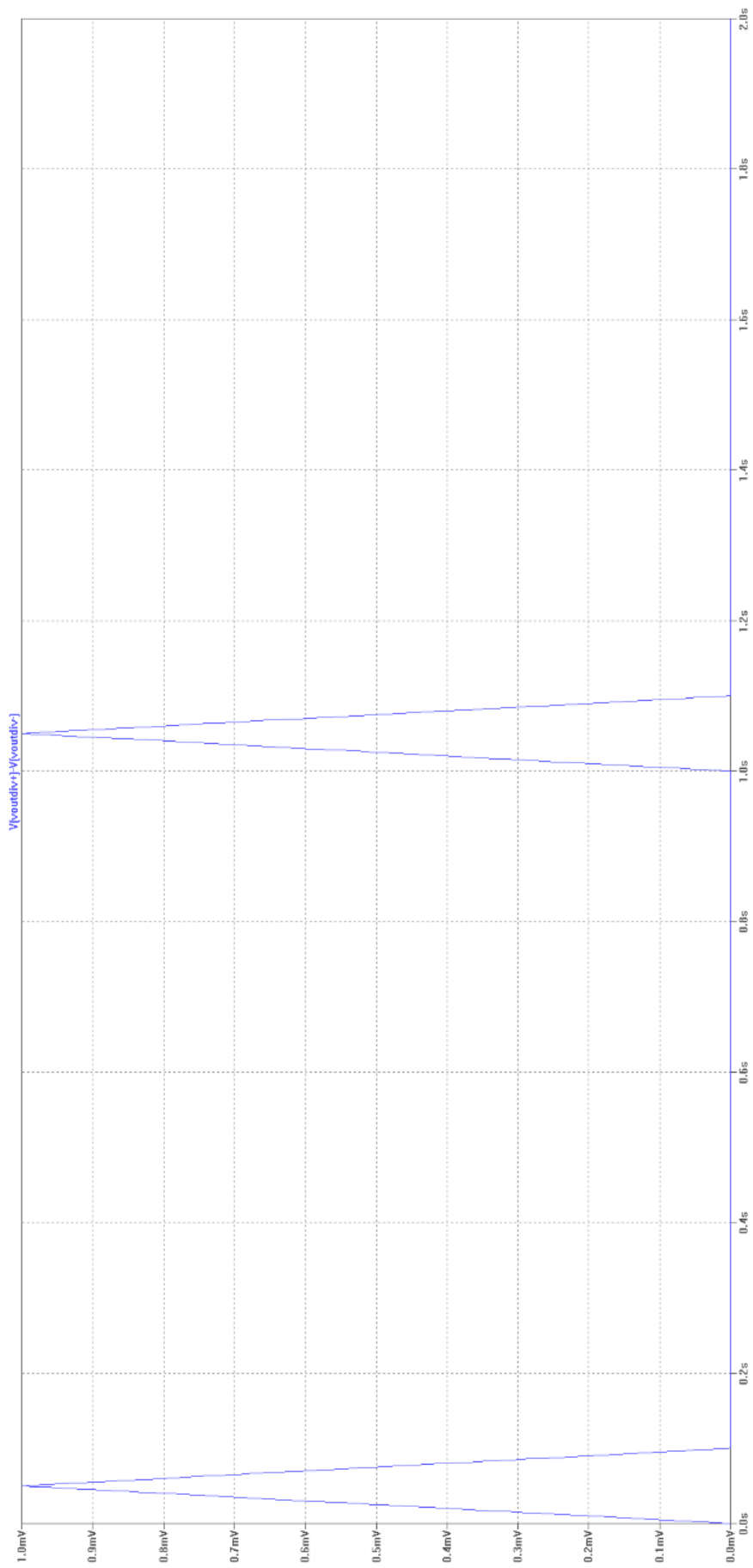


Figure 2.6.5. Differential signal at the output of the attenuator

In figure 2.6.4, the results are the desired, at one of the attenuator outputs, a sinewave, centered at the mid supply voltage with an amplitude of 0.1 V and a frequency of 50 Hz is present, corresponding to the signal exactly (or almost) as it was when injected in the common-mode input of the fully differential amplifier. In figure 2.6.5, the results are also the desired, at the differential output of the attenuator, the differential signal injected in the differential input of the fully differential amplifier is present with an amplitude of 1 mV (attenuated a thousand times).

2.6.2 Variable Capacitance Circuit

The variable capacitance circuit uses an innovative technique, and so, performance tests had to be performed before the system could be implemented. The stability and functionality of the circuit was tested, and the results are presented in this section.

Stability Test

The stability test is performed using the technique developed by Michael Tian, V. Visvanathan, Jeffrey Hantgan, and Kenneth Kundert, sometimes referred as *Tian probe*. This technique is employed in negative feedback circuits to check if the phase margin is adequate. “This technique is an improvement because it accounts for reverse feedback” [58], meaning the probe can be reversed and the results are the same. The *Tian probe* allows for the representation of the open loop frequency response. The probe circuits which inject the signals to measure the open loop response from the closed loop system are shown in figure 2.6.6.

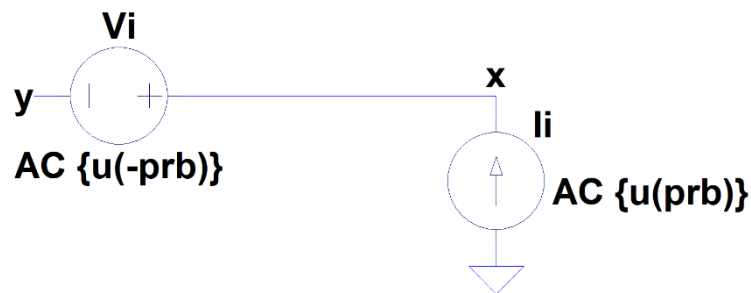


Figure 2.6.6. Probe circuit elements, used to inject the test signals [58]

The variable capacitance circuit used in the stability test is represented in figure 2.6.7. The values of the schematic components are defined in variables (using the LTSpice .param directive). Cref1 has a capacitance value of 1 nF, Cref2 has a capacitance value of 66 nF. Rd and Rf has a resistance value of 1 k Ω , Rsens has a value of 1.5 k Ω and Rset has a value of 5.6 k Ω .

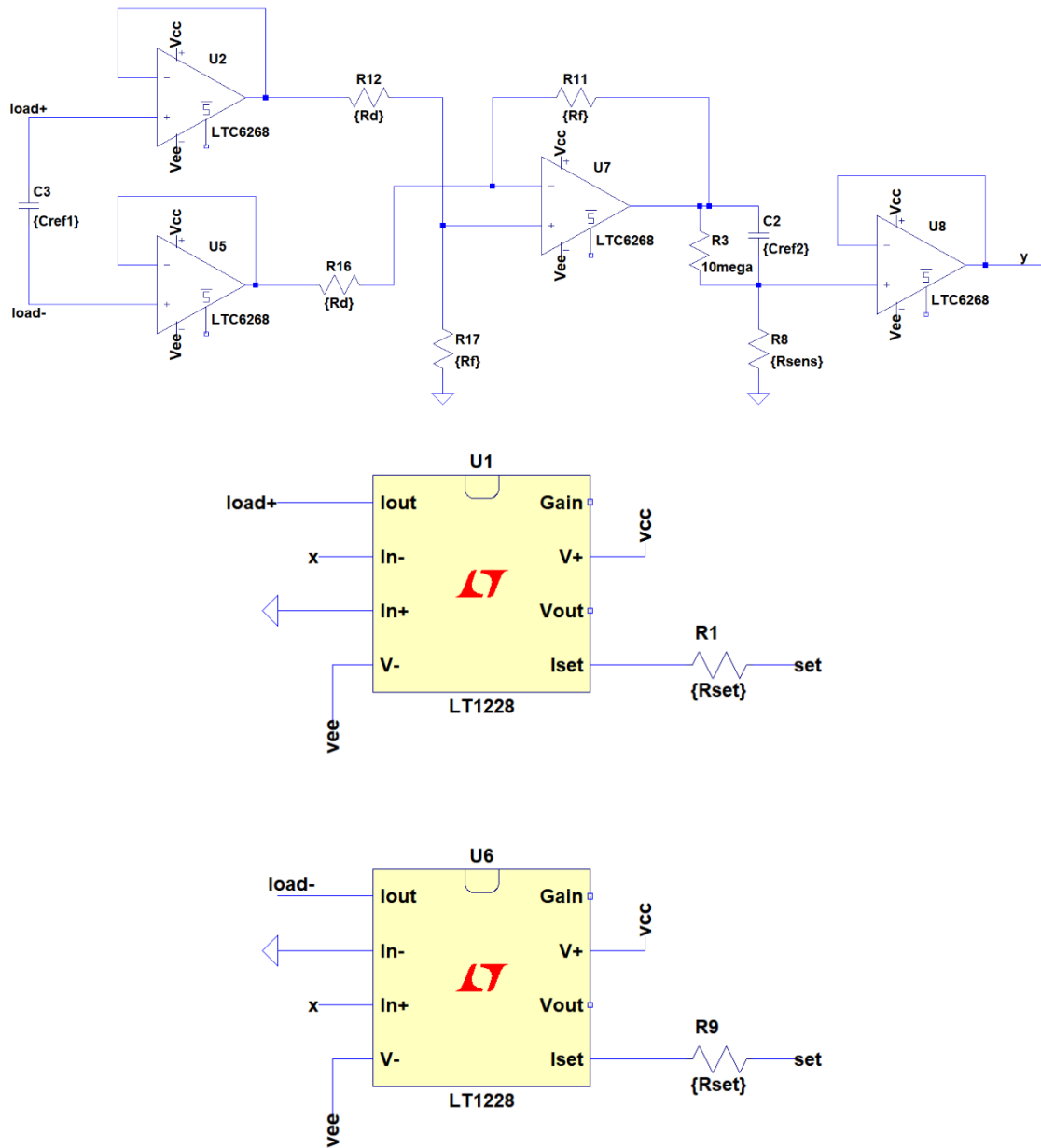


Figure 2.6.7: Variable capacitance circuit used in open loop frequency response simulation

In figure 2.6.8 (of next page), the open loop frequency response is plotted, simulated using a *Tian probe*.

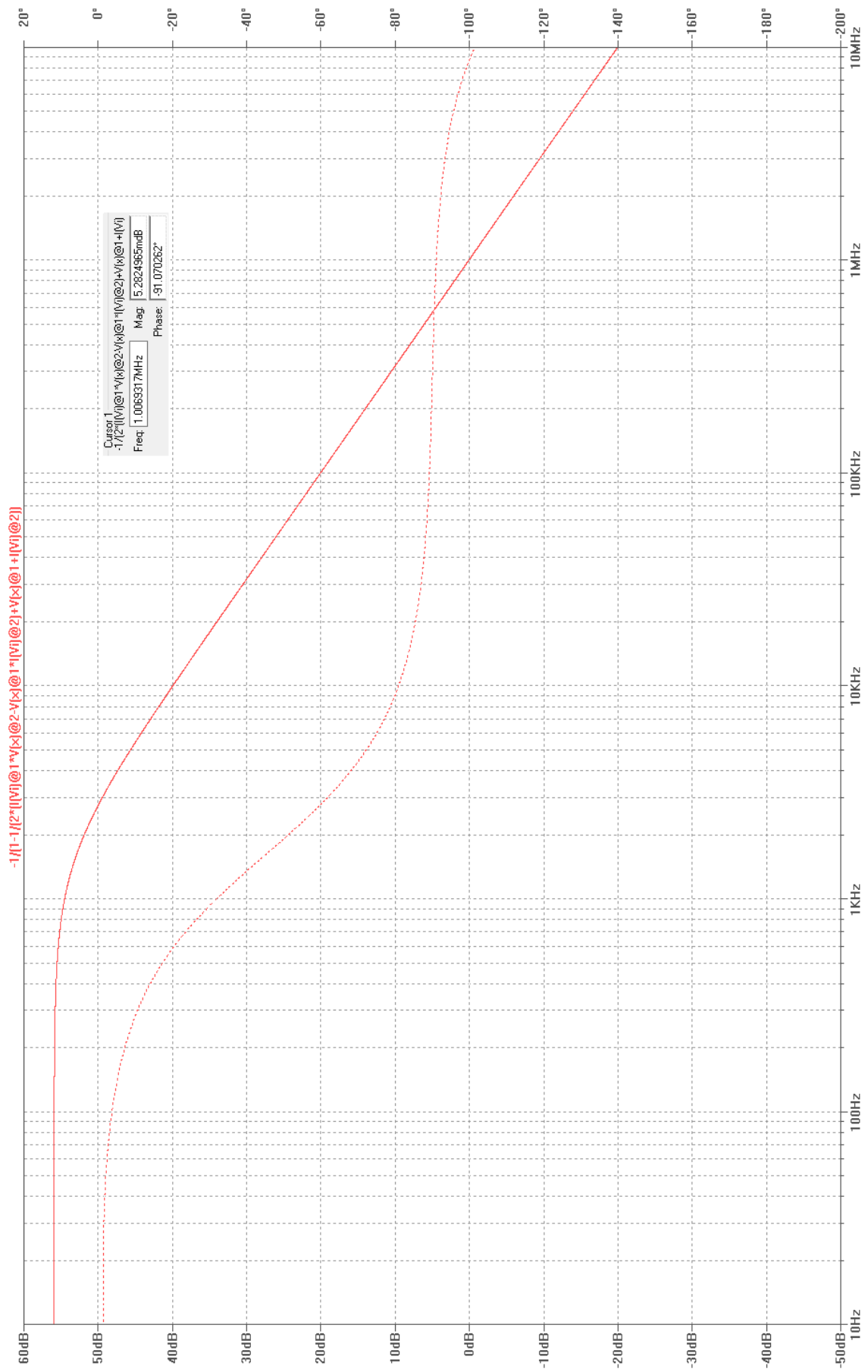


Figure 2.6.8. Open loop frequency response of the variable capacitance circuit

From the data obtained in the simulation, the phase margin can be calculated using the following expression ($|\Delta\phi| \approx 91^\circ$):

$$PM = 180^\circ - |\Delta\phi| = 89^\circ$$

A phase margin of at least 60° is recommended for good stability, 89° is an excellent value for the phase margin, indicating the system is stable. The gain curve does not present bumps or peaks which could indicate local stability issues.

Transient Analysis

In order to assess the circuit's performance, several transient analysis were performed. The circuit used to simulate the transient response includes three comparison models using RC networks, presented in figure 2.6.9. These circuits are needed to estimate the deviation the circuit presents when compared to a "real" capacitor.

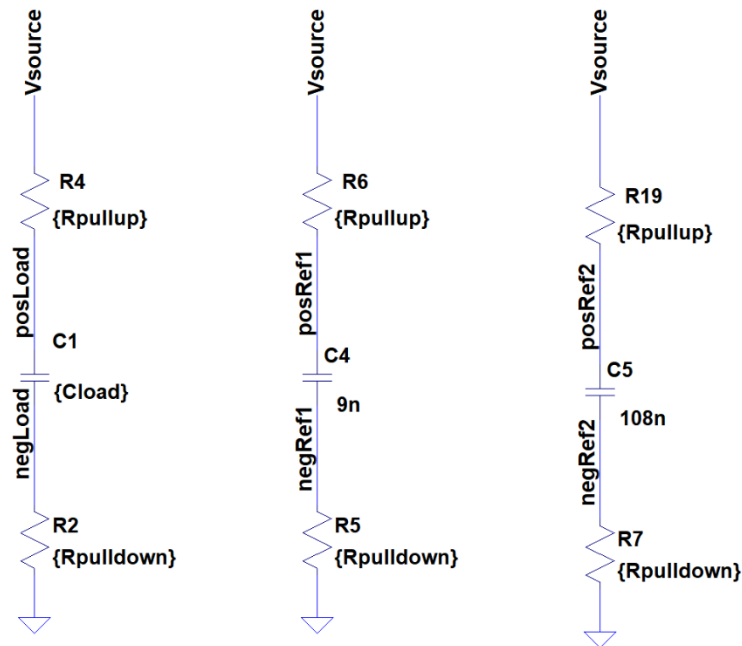


Figure 2.6.9. Comparison models

The RC circuit presented on the left is a comparison model which estimates the capacitance value of the simulated capacitor (in the variable Cload), it is used to evaluate system's performance and to evaluate the accuracy of the model.

The expressions to calculate the capacitance C_{LOAD} are the following:

$$C_{LOAD} \approx \left(1 + g_m R_{sens} \frac{C_{REF2}}{C_{REF1}}\right) C_{REF1} \approx 1 \times 10^{-9} + 99 \times 10^{-6} g_m [F]$$

$$g_m \approx 9.86 \times I_{set} [S]$$

$$I_{set} = \frac{V_{set} - 1.2}{R_{set}} = \frac{V_{set} - 1.2}{5600} [A]$$

A two diode voltage drop occurs in the current control input of the transconductance amplifiers, it was reduced to 1.2 V (instead of the typical 1.25 V), to allow the simulation of the C_{LOAD} capacitance with values of V_{set} as low as 1.2 V, giving positive or null I_{set} value (the current on the control pin must flow inward, because the internal circuit, a Wilson current mirror, acts as a current sink). V_{set} is measured in reference to the negative supply (power supply ground).

The other two (RC) comparison models are used to simulate a low-pass filter circuit, having the approximate maximum and minimum capacitance values the circuit simulates, with the defined V_{set} range (1.2 V to 1.9 V). The pull-up and pull down resistors simulate the step response of the circuit and an RC first order low-pass filter.

The circuit which simulates the transient response is presented in figures 2.6.10 and 2.6.11. The capacitance values are of 1 nF and 66 nF, for capacitors Cref1 and Cref2, respectively. The resistance values are of 1 k Ω , for R_d and R_f, 1.5 k Ω for the R_{sens} resistor, 5.6 k Ω for R_{set}, R_{pullup} and R_{pulldown} have a value of 10 k Ω for the step response and of 80 k Ω for the low-pass filter.

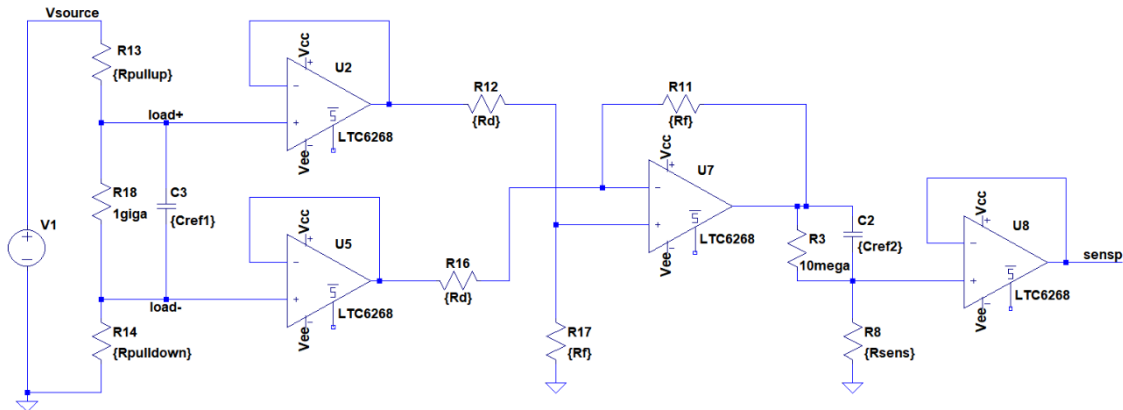


Figure 2.6.10. Variable capacitance circuit for transient response analysis (figure 1)

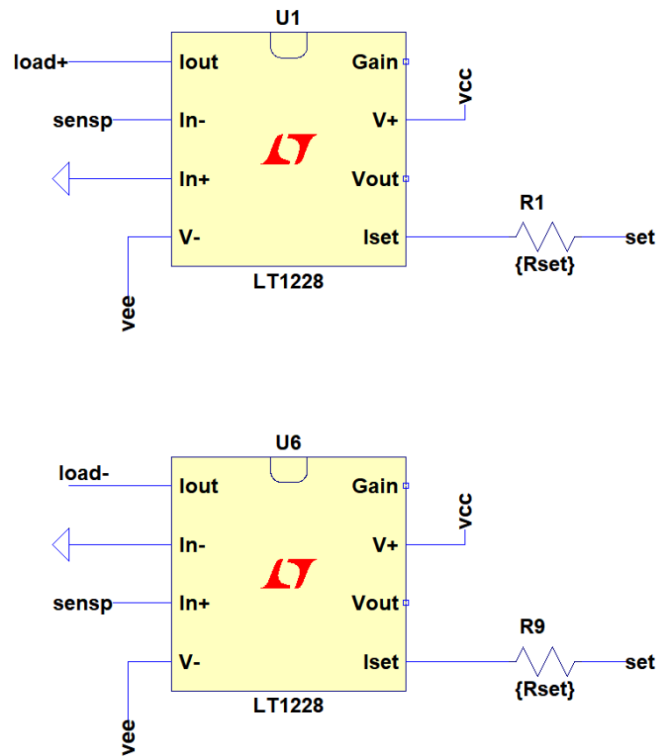


Figure 2.6.11: Variable capacitance circuit for transient response analysis (figure 2)

Step Response

The first performance analysis performed was the step response analysis, for comparison with a “real” capacitor RC network with the same values. Of course the accuracy of the model, is always questionable, because the Iset current input of the transconductance amplifier presents an exponential curve (the voltage drops in two PN semiconductor junctions), meaning that, for lower values the capacitance-voltage (or current) function cannot be accurately modeled by a linear regression. The Vset voltage is stepped from 1.2 V to 2.0 V in 0.1 V increments (measured in reference to Vee), the signal generated by the voltage source (V1) is a square wave with a duty cycle of 50 %, a frequency of 10 Hz, a maximum value of 1 V and a minimum value of 0 V (3.5 V and 2.5 V in relation to Vee, respectively). Figure 2.6.12, shows the step response of the circuit (red), compared to an ideal capacitor model (blue), having a capacitance value estimated by the circuit’s approximate expressions, the simulation runs for 200 ms and 100 ms are wasted (to eliminate initial transients), giving a total representation of 100 ms of signal. The signals are measured differentially at the terminals of the capacitors, of the variable capacitance circuit and comparison models.

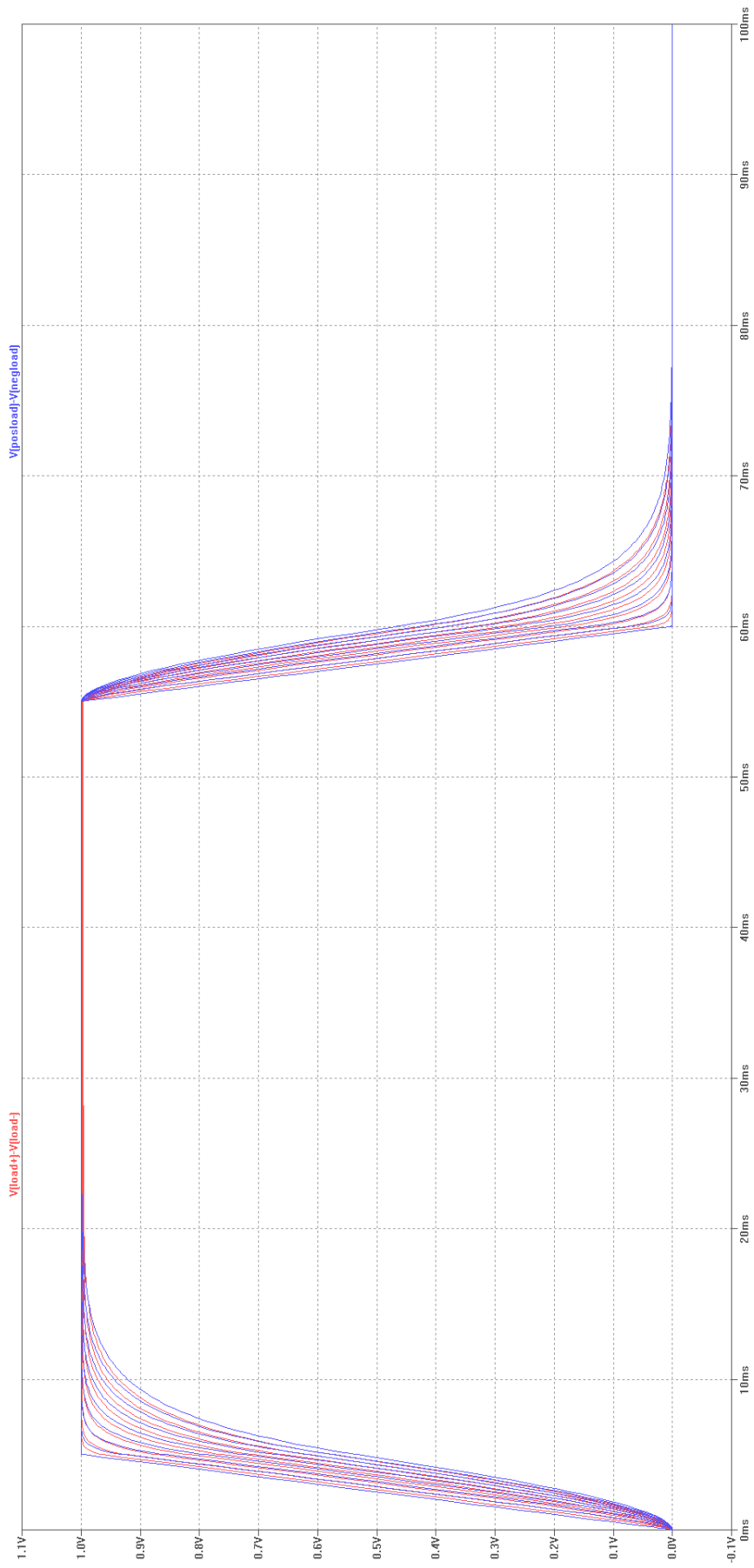


Figure 2.6.12. Variable capacitance circuit step response

The variable capacitance circuit tracks relatively well the step response of a real capacitor, for smaller capacitance values, the error of the model capacitor's capacitance expression is higher. Voltage on the graph is measured in relation to the supply midpoint (virtual ground).

Low-pass Filter

A low-pass filter was tested, this filter is of the first order and is formed by the simulated capacitance, the pull-up and pull-down resistors. The cut-off (-3 dB) frequency was set to 10 Hz at the maximum capacitance (about 100 nF) value of the test range. The expression which gives the pull-up and pull-down resistors value is, assuming both resistors have the same value:

$$R = \frac{1}{4\pi f C} = \frac{1}{4\pi \times 10 \times 100 \times 10^{-9}} \approx 79.5775 \text{ k}\Omega \approx 80 \text{ k}\Omega$$

The value of the pull up and pull down resistors of the simulation circuit is set to 80 k Ω , the 4 π in the expression is related to the fact the signal is measured differentially at the (simulated) capacitor's terminals, and the total series resistance of the circuit is 2R. The voltage is stepped from 1.2 V to 1.9 V (measured from the power supply ground, or Vee) in 0.1 V increments. A sinewave generator, generating a wave with a frequency of 10 Hz, with an amplitude of 1 mV and a DC component corresponding to the supply midpoint (virtual ground) is connected using the pull-up and pull-down resistors with the calculated resistance values), to the input of the variable capacitance circuit and to the model capacitors. These have a capacitance values of 9 nF and 108 nF (values determined for the variable capacitance circuit with 1.2 V and 1.9 V of control voltage, using the constant current method, presented in sub-section Constant Current Source, of this chapter). In figure 2.6.13, the graphical representation of the voltage measured differentially across the variable capacitor terminals is shown, represented by the blue curves. The graphical representation of the 9 nF and 108 nF ideal RC models are also presented, by the orange and red curves, respectively. There is a small error in the maximum capacitance model (red curve), because the actual maximum capacitance of the circuit is not exactly 108 nF (is about 107.6 nF). Apart from this small issue, the response of the system is as expected, with the system behaving (almost) exactly like a "real" capacitor. The simulation runs for 200 ms, 100 ms of samples are wasted, to reject initial transients, one period, 100 ms of the sinewave are represented. Voltage on the graph is measured in relation to the supply midpoint (virtual ground).

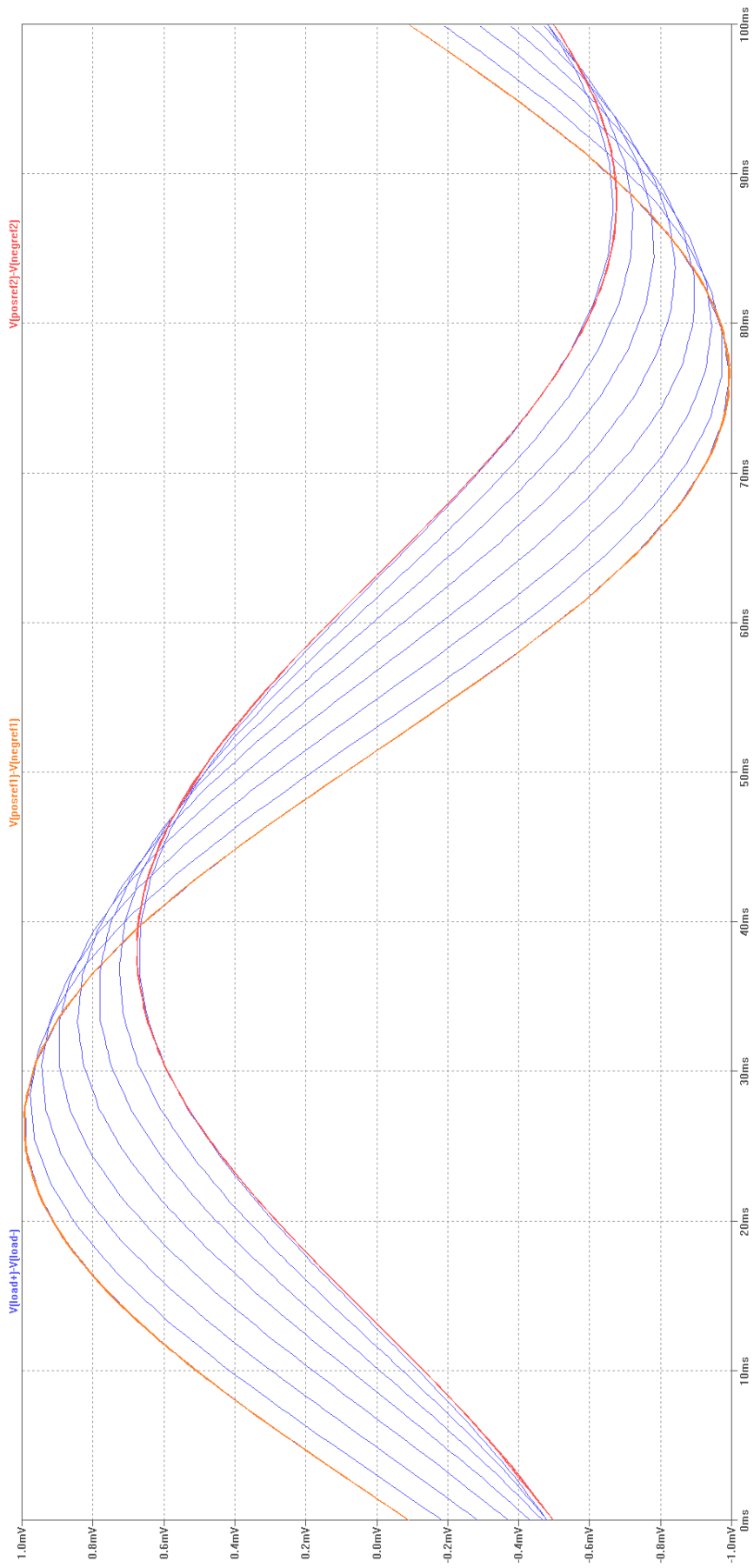


Figure 2.6.13. Low-pass filter transient response to a 1 mV sine wave with a frequency of 10 Hz

Constant Current Source

A commonly employed method to determine capacitance is by flowing a small current at the terminals of a capacitor by means of a constant current source. At first the capacitor is discharged to keep a null potential at its terminals (of 0 V). Then a constant current (usually between 1 μA and 1 mA) is applied until the voltage on its terminal reaches, a predefined voltage of, for example, 0.1 V. The cycle repeats and the average capacitance value is calculated using the following expression:

$$C = \frac{i(t)}{\frac{dv(t)}{dt}} [F]$$

In the simulation performed only one cycle is necessary to determine the capacitance, the capacitor does not need to be discharged, the supply voltages, however, must start at zero. The constant current source (with a value of 1 μA) used in the simulation is presented in figure 2.6.14, it is connected to the terminals of the simulated capacitor.

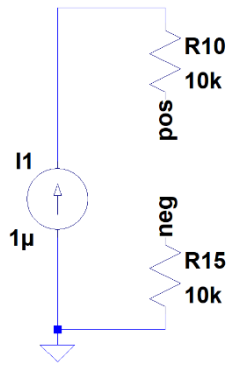


Figure 2.6.14. Constant current source used in the simulation

Resistors were added to simulate floating capacitance. DC blocking capacitors were added at the input of the variable capacitance circuit (simulated capacitor terminals), to determine if the circuit is capable of working with AC current only. The DC blocking capacitors are presented in figure 2.6.15. These capacitors, however, once placed in series with the simulated capacitor, lower the capacitance of the circuit. The capacitance is given by the following expression (C_{sim} corresponds to the total capacitance simulated including DC blocking capacitors, C_{load} is the capacitance of the circuit without the DC blocking capacitors, C_2 and C_6 are the DC blocking capacitors capacitance (2.2 μF):

$$C_{sim} = \left(\frac{1}{C_2} + \frac{1}{C_6} + \frac{1}{C_{load}} \right)^{-1} = \frac{1.1 \times 10^{-6} \times C_{load}}{1.1 \times 10^{-6} + C_{load}} [F]$$

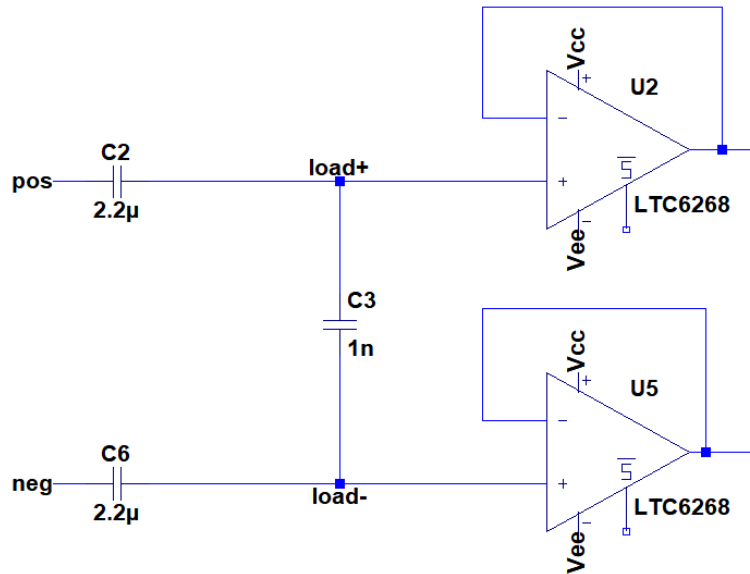


Figure 2.6.15. DC blocking capacitors (C2 and C6) at the terminals of the variable capacitance circuit

The simulation results are presented in table 2.4, the control voltage was stepped in 0.1 V steps, from 1.2 V to 2.0 V. The derivative capacitance expression (see previous page) was used to plot the graph, and the simulation resulted in nine constant capacitance values.

Control Voltage (Vset)	Simulated Capacitance (Csim)
1.2 V	9.06 nF
1.3 V	18.833 nF
1.4 V	30.921 nF
1.5 V	44.023 nF
1.6 V	57.534 nF
1.7 V	71.152 nF
1.8 V	84.718 nF
1.9 V	98.141 nF
2.0 V	111.367 nF

Table 2.4. Capacitance versus control voltage (constant current analysis)

The results are within expected, the capacitance can be varied in the desired range (from 10 nF to 100 nF) using control voltages between 1.2 V and about 1.9 V (referenced to Vee, the power supply ground).

2.6.3 ADC Buffer

The ADC buffer is the amplifier which drives the input of the analog-to-digital converter. It is necessary to know the frequency response of this circuit, because it should feature an anti-aliasing low-pass filter, this circuit element should be able to filter aliasing while allowing the desired signal to pass without being attenuated. The sampling rate span, from 500 SPS to 2000 SPS, generate a minimum aliasing frequency in the range of 250 to 1000 Hz, so the antialiasing filter must have a cut-off frequency lower than 250 Hz. Attention must be paid, because the frequencies of interest, are between 0.01 Hz and 100 Hz, the cut-off frequency must be higher than 100 Hz, in the range of 100 Hz to 250 Hz.

The circuit which simulates the frequency response of the ADC buffer is presented in figure 2.6.16.

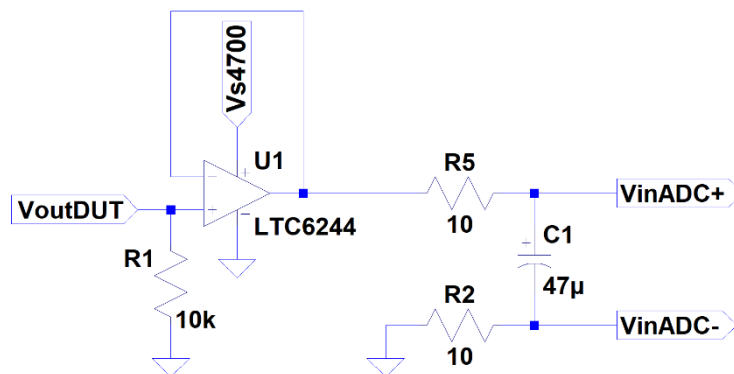


Figure 2.6.16. Schematic of the ADC buffer circuit configuration used in AC analysis

The low-pass filter is formed by the elements R2, R5 and C1, the voltage which drives the ADC comes from the DUT (ECG Front End). The opamp used in the simulation is of a different manufacturer and model, because the model of the opamp incorporated in the circuit is not present in LTSpice libraries, and the LTC6244 is the opamp with more similar characteristics.

The result of the AC analysis (the frequency response of the ADC buffer), is presented in figure 2.6.17. The voltage output is measured differentially because the ADC input is differential. An AC source with unity amplitude and zero phase shift was connected to the buffer's input (labeled VoutDUT) to perform the AC analysis.

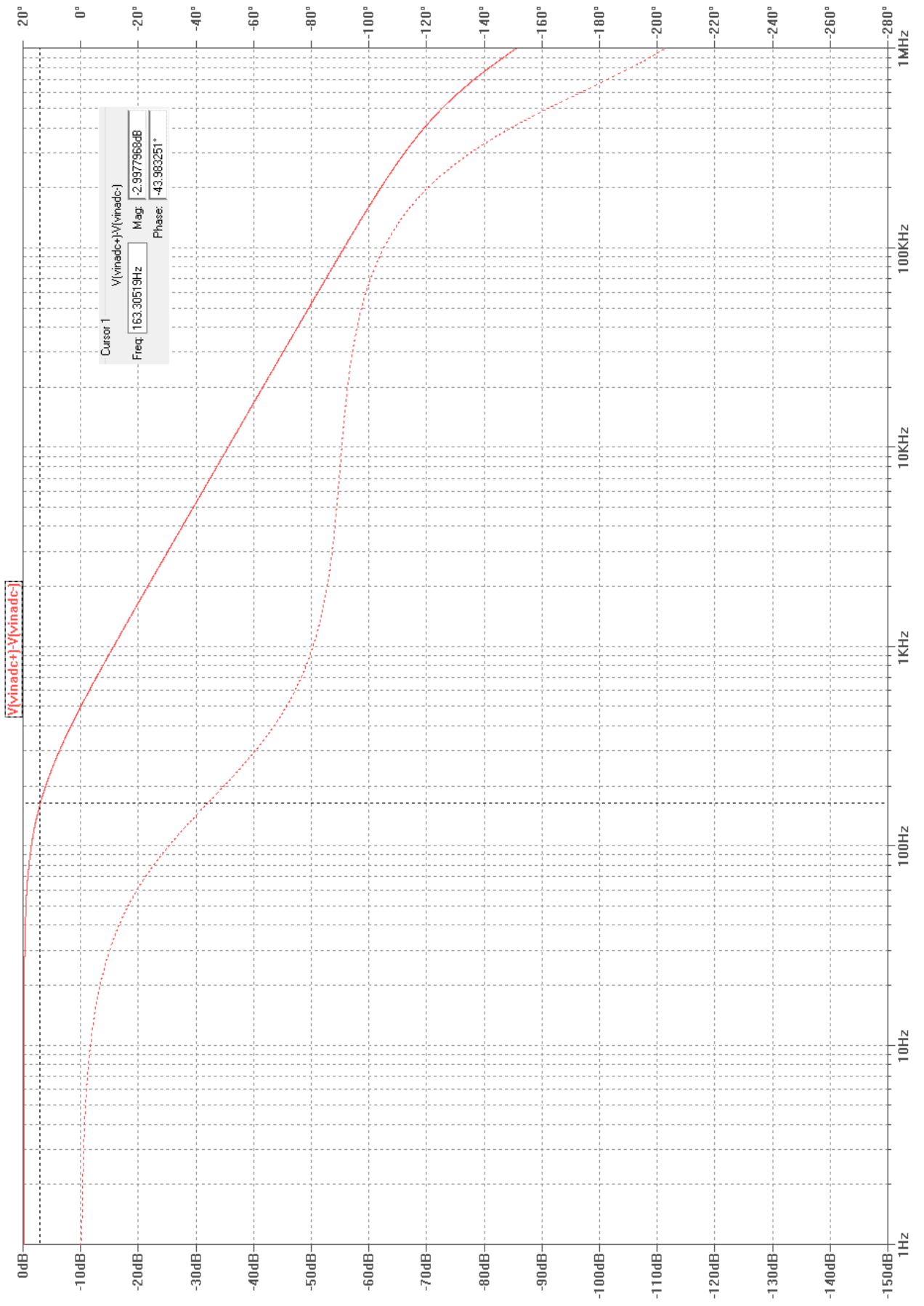


Figure 2.6.17. Frequency response of the ADC buffer

The response of the low-pass anti-aliasing filter is adequate, with a cut-off frequency of about 163 Hz. A higher order filter would present a better frequency response, but with added complexity and cost, for this purpose, a first order filter is adequate, because it has a good cost-performance ratio. In addition, some ECG front ends feature a low pass filter with a cut-off frequency of 100 Hz or less.

3 Test Results and Discussion

In this section, the results of tests performed to the implemented system are presented and discussed. The variable capacitance circuit parameters are determined using different methods and the results are analyzed. A series of tests performed with an analog output ECG front-end, the Analog Devices Incorporated, AD8232, are also presented and explained.

3.1 Variable Capacitance Circuit

The variable capacitance circuit was tested using two methods and three parameters were determined during the tests. The two capacitance measurement methods are the constant current method and the bridge method, the last method allows not only to determine the capacitance but also the series and parallel parasitic resistors of the non-ideal capacitor model. Figure 3.1.1, shows parasitic elements present in a non-ideal capacitor.

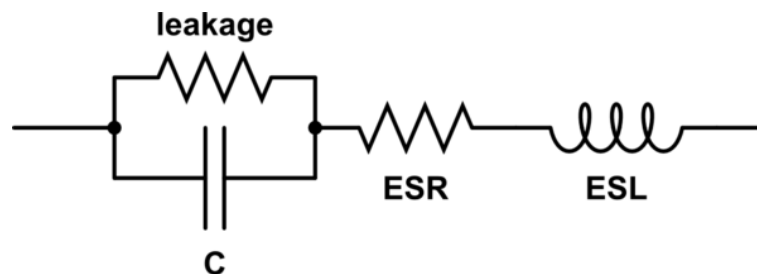


Figure 3.1.1. Simplified model of a non-ideal (real) capacitor [59]

The ESR (equivalent series resistance), C (capacitance) and leakage resistance values were measured for different control voltages, the ESL (equivalent series inductance) was not determined, because this parasitic element usually is caused by the wiring, capacitor manufacturing process or architecture and has a low value, and also because the frequencies of interest of the signal are relatively low (up to 100 Hz).

3.1.1 Constant Current Measurement Method

The capacitance of the circuit was measured using a Keysight Technologies, 34405A digital multimeter. This device measures the capacitance by applying a known current to the capacitor [60]. The simplified equivalent circuit is presented in figure 3.1.2.

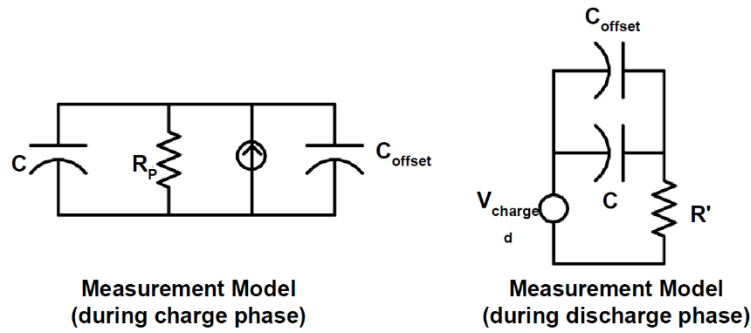


Figure 3.1.2. Keysight 34405A simplified equivalent circuit for capacitance measurement [60]

The capacitance is determined by measuring the voltage change (ΔV), which occurs over a short period of time (Δt). The measurement cycle consists of two parts, a capacitor charge phase and a capacitor discharge phase [60]. The formula used to calculate the capacitance is the following (I corresponds to the constant current provided by the current source during the charge phase):

$$C = \frac{I}{\frac{\Delta V}{\Delta t}} [F]$$

The capacitance values obtained are shown in the table below, the voltage values are referenced to the power supply ground.

Control Voltage	Measured Capacitance
1.0 V	1.4 nF
1.1 V	1.8 nF
1.2 V	8.3 nF
1.3 V	20.1 nF
1.4 V	33.6 nF
1.5 V	47.3 nF
1.6 V	62.4 nF
1.7 V	80.0 nF
1.8 V	101.0 nF

Table 3.1. Measured capacitance versus control voltage

The capacitance measurements were made without DC blocking capacitors with a variable capacitance circuit mounted in a printed circuit board (PCB). The values meet the expectations, the capacitance varies between 10 nF and 100 nF.

A graphical representation of the capacitance values was also made, with Microsoft Corporation's Excel, and a linear regression was also performed in order to obtain an expression of the voltage dependence of capacitance. The graph is represented in figure 3.1.3, the horizontal axis corresponds to the capacitance control voltage, in Volt, measured in relation to the power supply ground, the vertical axis represents the capacitance in nanoFarad.

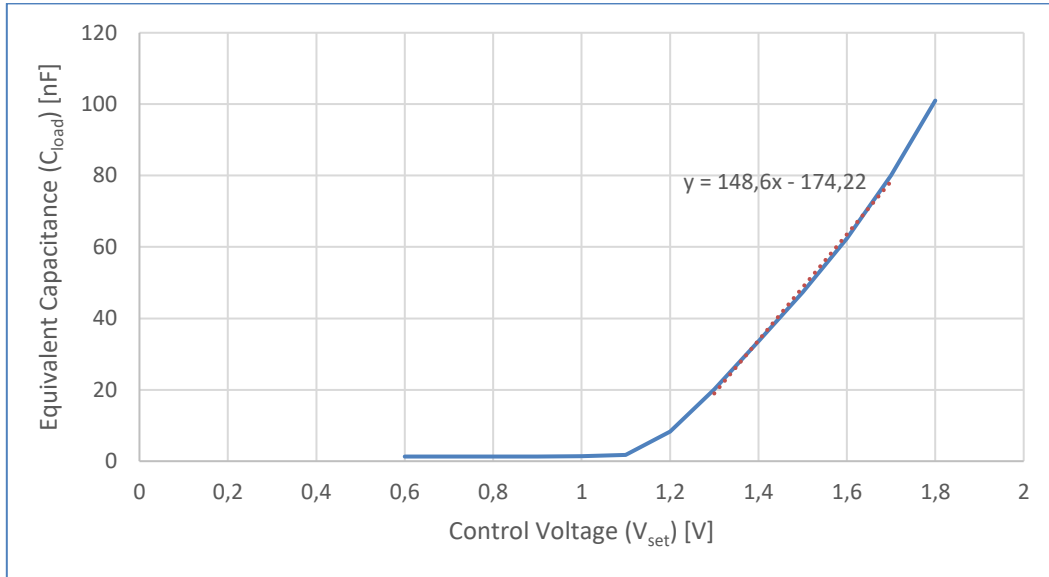


Figure 3.1.3. Graphical representation of capacitance as function of the control voltage

The linear regression is represented in the graph, its expression is also shown, near the blue curve, this function is defined as follows:

$$C_{load} = 148.6V_{ref} - 174.22 \text{ [nF]}$$

Where C_{load} corresponds to the capacitance simulated by the circuit in nanoFarad, V_{ref} corresponds to the control voltage measured in relation to the power supply ground. In the conditions the measurements were performed this expression gives the approximate capacitance value.

3.1.2 Bridge Measurement Method

In order to perform measurements using AC signals another equipment is used, this equipment allows the measurement of resistive parasitic elements. The equipment used was the Model SR715, LCR Bridge, manufactured by Stanford Research Systems Incorporated. This equipment employs the bridge method to measure capacitance and resistance. The equivalent circuit used to determine the LCR values is presented in figure 3.1.4.

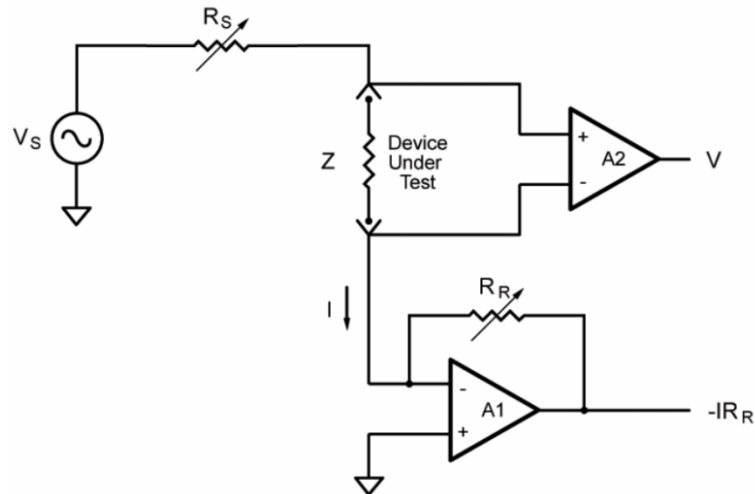


Figure 3.1.4. Schematic of the equivalent measurement circuit of the SR715 LCR Bridge [61]

The equipment measures the impedance of a DUT (device under test) by measuring the voltage across its terminals and the current that flows through it. Both the imaginary and real components of the signal are measured. The ratio of the voltage to current, according to Ohm's law gives the impedance. Voltage and frequency of the test signal generated by the source, labeled V_S , can be adjusted using the equipment's controls. The voltage is applied to the DUT, by resistor R_S , which varies in accordance with the measurement range. The current flows to the virtual ground of A1 (a very small portion), and flows through the resistor R_R , the feedback element of the transimpedance amplifier (current to voltage converter). A1 produces a voltage signal that is proportional to the current ($I \times R_R$). The voltage across the DUT is measured in a different signal path providing a 4-wire Kelvin connection. The real and imaginary parts of the signal are obtained by multiplication of the voltage and current signals with a reference signal in phase and another in quadrature (90 degree phase shift). The resulting signals are measured by an ADC which communicates with a microprocessor. The values are corrected in accordance with calibration factors, converted to impedances, and finally converted to values that can be represented by the display of the device.[61].

The first set of measurements performed using the LCR bridge measure the capacitance and ESR (equivalent series resistance), function called C+R (series equivalent circuit) in the equipment used. The results of the tests performed are presented in table 3.2 The voltages are referenced to the power supply ground.

Control Voltage	Measured Capacitance	Measured ESR
1.0 V	1.491 nF	57.824 kΩ
1.1 V	1.926 nF	38.21 kΩ
1.2 V	7.657 nF	12.468 kΩ
1.3 V	17.77 nF	5.496 kΩ
1.4 V	30.69 nF	3.175 kΩ
1.5 V	46.48 nF	2.202 kΩ
1.6 V	62.20 nF	1.647 kΩ
1.7 V	77.55 nF	1.313 kΩ
1.8 V	93.34 nF	1.077 kΩ
1.9 V	112.1 nF	0.935 kΩ
2.0 V	129.9 nF	0.802 kΩ

Table 3.2. Measured capacitance and ESR versus control voltage

A graphical representation was made in Excel with the measurement results, and the linear regression of the capacitance estimated (figure 3.1.5).

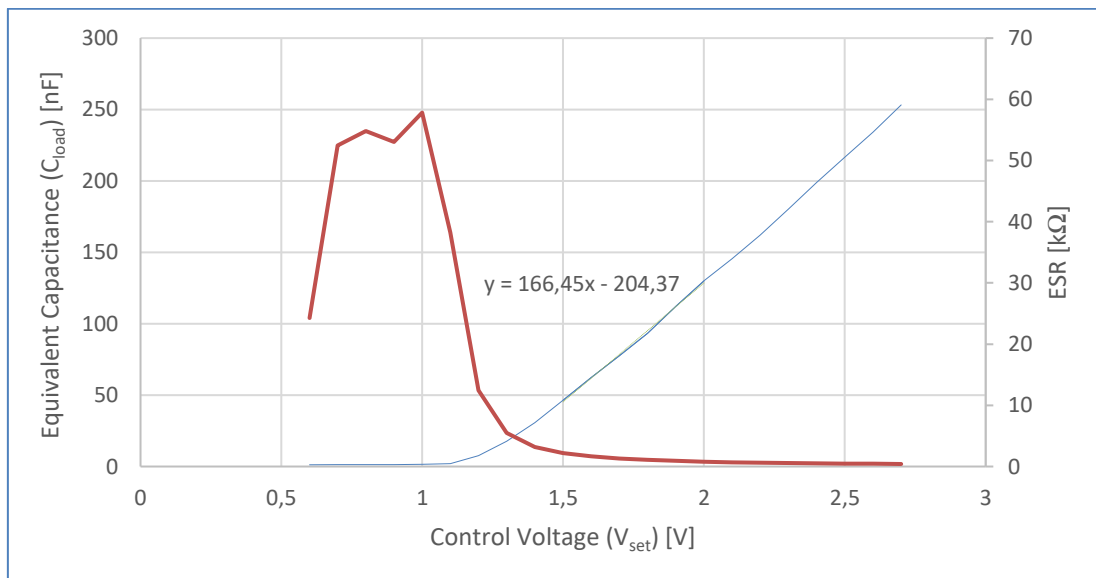


Figure 3.1.5. Graphical representation of ESR and capacitance as functions of control voltage

The blue curve corresponds to the capacitance, the red curve corresponds to the ESR. The linear regression is represented on the graph, close to the capacitance curve.

The horizontal axis represents the control voltage in Volt, the vertical axis on the left corresponds to the capacitance in nanoFarad, the vertical axis on the right corresponds to the series resistance, ESR, in kiloOhm. The function that resulted from the linear regression calculated in Excel has the following expression:

$$C_{load} = 166.45V_{ref} - 204.37 [nF]$$

C_{load} corresponds to the capacitance simulated by the circuit in nanoFarad and V_{ref} corresponds to the control voltage measured in relation to the power supply ground. In the conditions the test was performed this expression gives the approximate capacitance value. The variable capacitance circuit was measured without DC decoupling capacitors, mounted on a printed-circuit board, using a signal with 0.1 V_{RMS} and a frequency of 1 kHz.

The parallel (leakage) resistance of the circuit was also measured using the LCR Bridge, in a test called C+R (parallel equivalent circuit) in the equipment. The results of the tests performed are presented in table 3.3. The tests were performed in the same conditions as the ESR tests, except for the test signal used, that has a frequency of 100 Hz and 1 V_{RMS}. The voltages are referenced to the power supply ground.

Control Voltage	Measured Capacitance	Measured Leakage Resistance
1.0 V	1.428 nF	1028 kΩ
1.1 V	2.857 nF	996 kΩ
1.2 V	8.051 nF	869 kΩ
1.3 V	18.046 nF	614 kΩ
1.4 V	31.342 nF	407 kΩ
1.5 V	46.089 nF	305 kΩ
1.6 V	61.807 nF	241 kΩ
1.7 V	74.869 nF	278 kΩ
1.8 V	91.083 nF	221 kΩ
1.9 V	107.77 nF	184 kΩ
2.0 V	124.83 nF	154 kΩ

Table 3.3. Measured capacitance and parallel resistance versus control voltage

A graphical representation was made in Excel from the measurement results and a linear regression performed (figure 3.1.6).

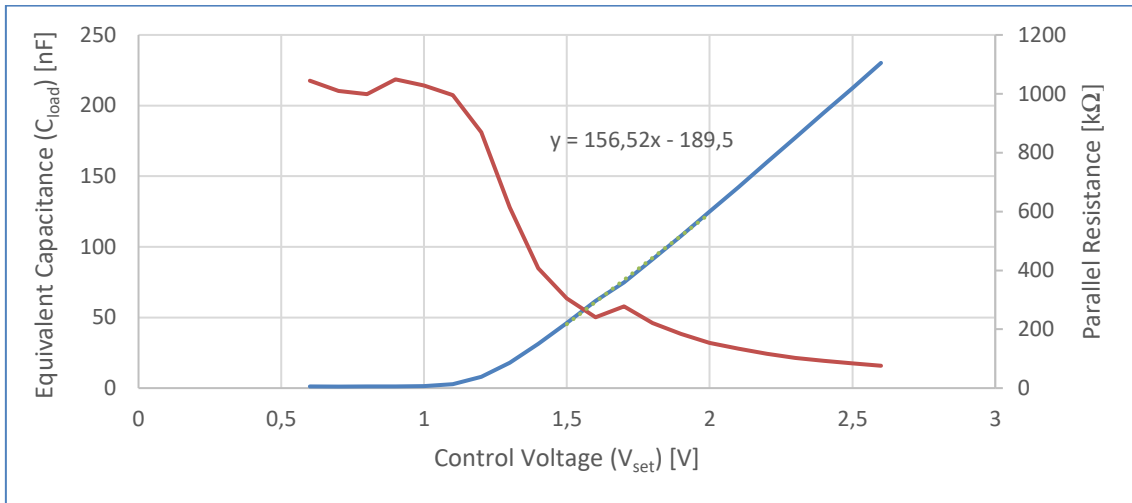


Figure 3.1.6. Graphical representation of the capacitance and leakage resistance as functions of the control voltage

In the graph, the blue curve corresponds to the function of the capacitance simulated by the circuit and the red curve corresponds to the parallel (leakage) resistance of the capacitor. The horizontal axis corresponds to the control voltage referenced to the power supply ground in Volt, the vertical axis on the left corresponds to the capacitance in nanoFarad, the vertical axis on the right corresponds to the parallel (leakage) resistance in kiloOhm. A linear regression of the capacitance curve was also performed and is presented in the graph between the two curves, its expression is the following:

$$C_{load} = 156.52V_{ref} - 189.5 \text{ [nF]}$$

C_{load} corresponds to the capacitance simulated by the circuit in nanoFarad, V_{ref} corresponds to the control voltage, in Volt, measured in relation to the power supply ground. In the conditions the test was performed this expression gives the approximate capacitance value.

Results Discussion

The capacitance measurements are relatively consistent, for the two measurement methods, meaning the circuit is behaving as a capacitor as expected. There are, however, some issues, because, the ESR decreases as the capacitance increases and shows relatively high values on the order of the kiloOhm or dozens of kiloOhm. Another issue is the leakage resistance, which appears to decrease as the capacitance increases, reaching relatively low values, on the order of the hundreds of kiloOhm.

3.2 ECG Front End

Several ECG front end performance tests were executed, to assess the system capabilities. The ECG front end was tested for:

- Large common-mode offset variation (fast restore performance)
- Different values of skin-electrode resistance and capacitance
- Lead-off performance
- Time varying skin-electrode resistance and capacitance (misplaced electrode)
- Common-mode and differential noise rejection
- Baseline wander

The tests were performed to the Analog Devices incorporated, AD8232, ECG front end, with fast restore activated and in a two electrode configuration.

In the tests performed the horizontal axis represents the time in seconds. The left vertical axis represents the output voltage of the DUT in Volt, referenced to the power supply ground, otherwise specified. The AD8232 is supplied by the 3.3 V rail of the power supply, so voltage values between -2.5 V (0 V) and 0.8 V (3.3 V) are expected (referenced to the 5 V supply midpoint and to the power supply ground, between parenthesis), assuming the output amplifier of the ECG front end is rail-to-rail.

3.2.1 Common-mode Offset Variation

A common-mode offset variation test was performed, the skin-electrode impedance values are of 100 k Ω in parallel with 10 nF. The common-mode and differential noise is set to minimum. The ECG amplitude is about 1.4 mVpp (at the input of the skin-electrode simulation circuit). The test duration is 30 seconds.

The test is performed with an initial common-mode voltage of about 0 V (referenced to the midsupply voltage). After 10 seconds of test time, the offset suffers a sudden change to 0.5 V (simulating poor contact of the electrode with the skin), and after 20 seconds returns to its initial value of 0 V.

The result of the test is presented in figure 3.2.1. The right vertical axis represents the common-mode input offset voltage, in Volt, referenced to the 5 V supply midpoint. The blue trace represents the DUT output voltage, the red trace represents the common-mode input offset voltage.

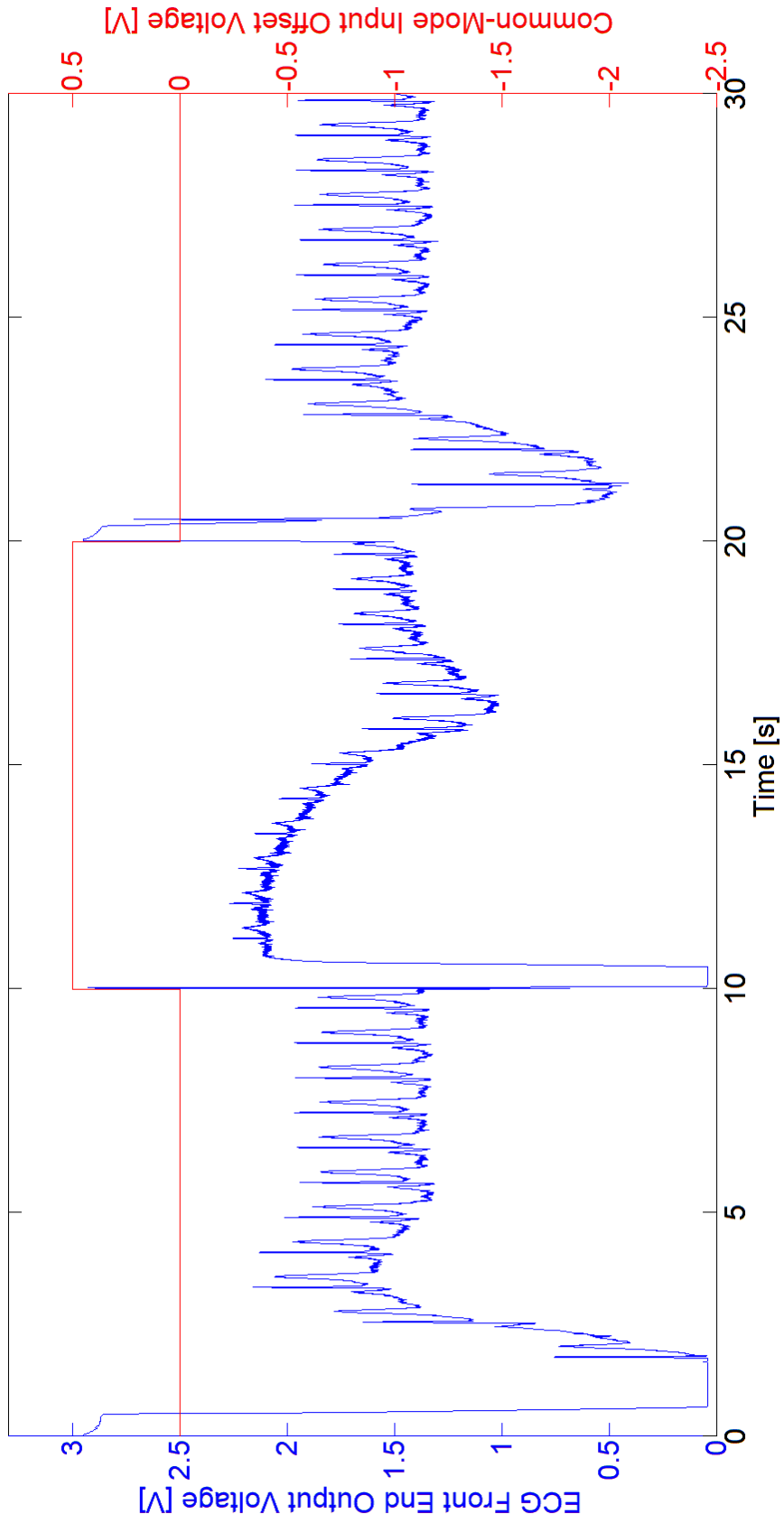


Figure 3.2.1. Common-mode offset variation test

The change in the common-mode DC component is noticeable at 10 s, the DUT saturates, fast restore circuit is enabled. The baseline level is restored at about 18 s, 8 seconds after the event. At 20 s, the common-mode voltage changes again and the baseline drops, the baseline level is restored at about 25 s.

3.2.2 High Skin-Electrode Resistance

This test includes a high resistance in the skin-electrode interface of both electrodes. The resistance was set to 900 k Ω in parallel with 10 nF. The common-mode and differential noise is set to minimum. The DC component (referenced to the power supply midpoint, 2.5 V) is 0 V for the common-mode and differential components of the signal. The ECG amplitude is about 1.4 mVpp (at the input of the skin-electrode simulation circuit). The parameters are initially defined and remain constant throughout the test. The test runs for 10 seconds.

The result of the test is presented in figure 3.2.2. It can be noticed that, when compared to the other tests, the amplitude of the ECG signal is much inferior and the signal also presents more noise. A larger resistance, generate more thermal noise (Johnson-Nyquist noise). Another reason is the noise, which is set to minimum, but it is still be present, and as the amplitude is lower, the signal to noise ratio is also lower and the signal appears to have more noise.

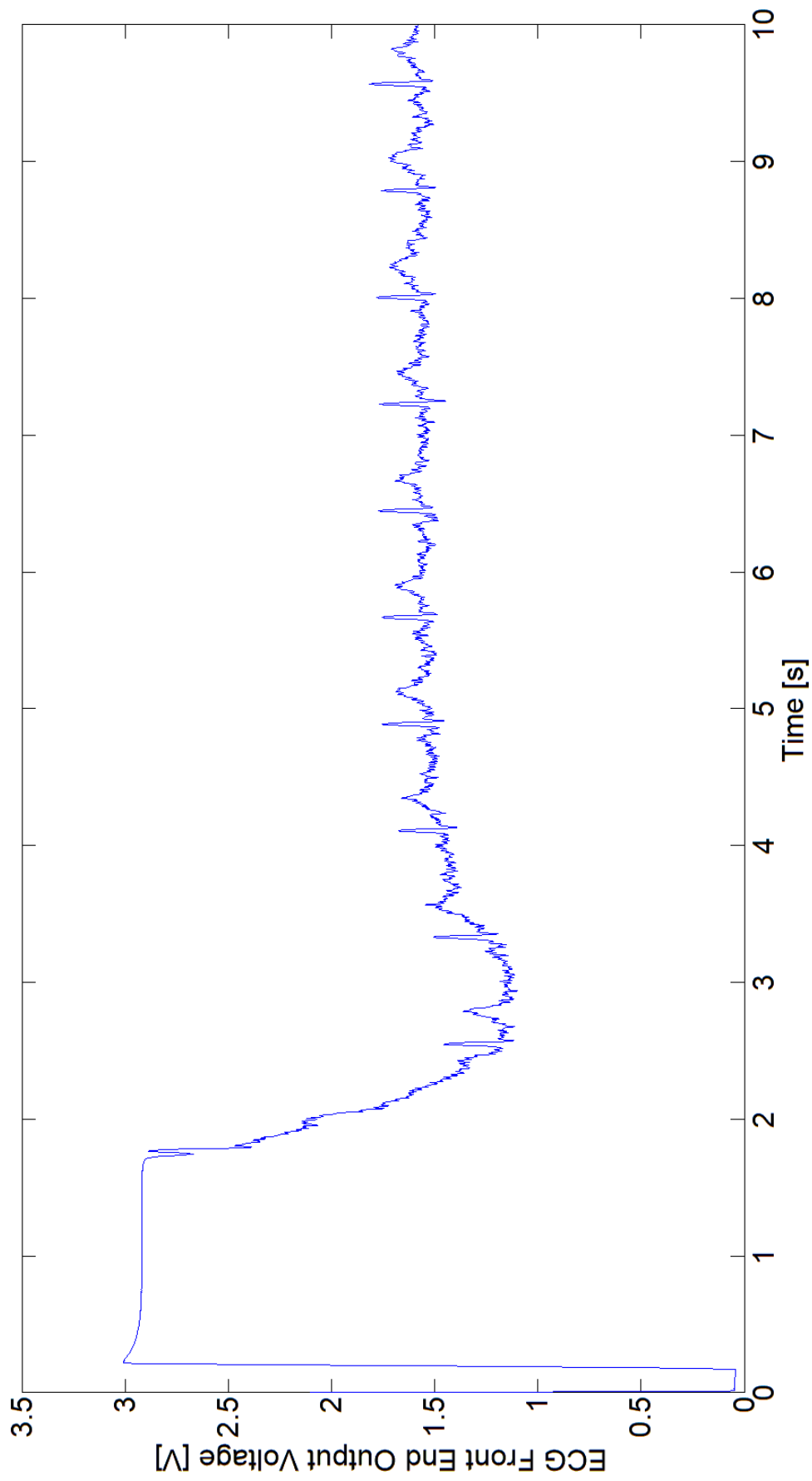


Figure 3.2.2. High skin-electrode resistance test

3.2.3 High Skin-Electrode Capacitance

In this test the capacitive component of the skin-electrode model is set to 50 nF in both simulated electrodes. The resistance is set to 100 k Ω for both electrodes. The remaining parameters have the same value as in the previous test. The test runs for 10 seconds.

The result of the test is presented in figure 3.2.3. In this test the amplitude of the signal increases and the noise increases. A higher capacitance has a lower impedance for time varying signals, allowing more noise to ingress to the input of the DUT.

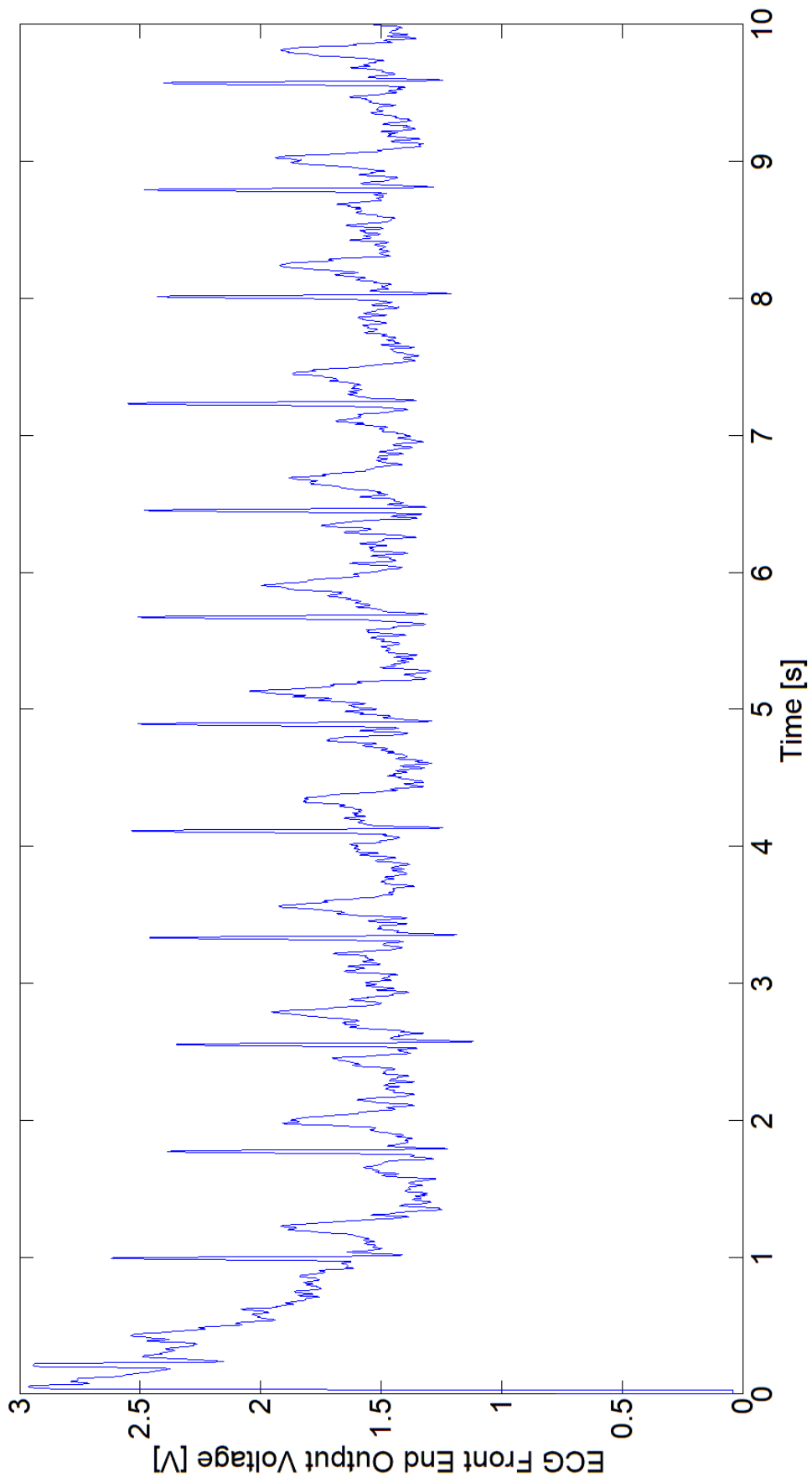


Figure 3.2.3. High skin-electrode capacitance test

3.2.4 Lead-Off Performance

The lead-off performance test is performed by disconnecting one of the (simulated) electrodes from the input of the DUT. In this test the positive electrode is disconnected after 30 seconds and reconnected after 40 seconds. The negative electrode is disconnected after 70 seconds and reconnected after 80 seconds. The skin-electrode impedance is 100 k Ω in parallel with 10 nF. The remaining parameters have the same values as in the previous test. The test duration is 120 seconds.

The result of the lead-off test is presented in figure 3.2.4. The right vertical axis represents the output voltage of the ECG front end, in Volt, referenced to the power supply ground. The left vertical axis represents the lead-off switch logic state, “1” means the switch is closed (simulating the electrode connected to the patient’s body), and “0” corresponds to the switch in the open position (simulates the opposite situation, in which the electrode is disconnected from the patient’s body). The black trace represents the output voltage of the DUT, the red trace represents the positive electrode (left arm electrode) lead-off switch logic state and the blue trace represents the negative electrode (right arm electrode) lead-off switch logic state.

At 30 s, the positive electrode is disconnected and the sudden impedance change makes the DUT saturate to negative supply rail. At 40 s, the electrode is reconnected and the DUT saturates to the positive supply rail, because of the sudden impedance change. The ECG front-end recovers the signal at about 63 seconds, taking about 23 seconds to recover the signal after lead-off. At 70 s, the front-end is disconnected from the negative electrode and saturates to the positive supply rail. The electrode is reconnected at 80 s, and the DUT saturates to the negative supply rail. The front-end recovers the ECG signal after about 17 seconds, at about 97 seconds of test time elapsed.

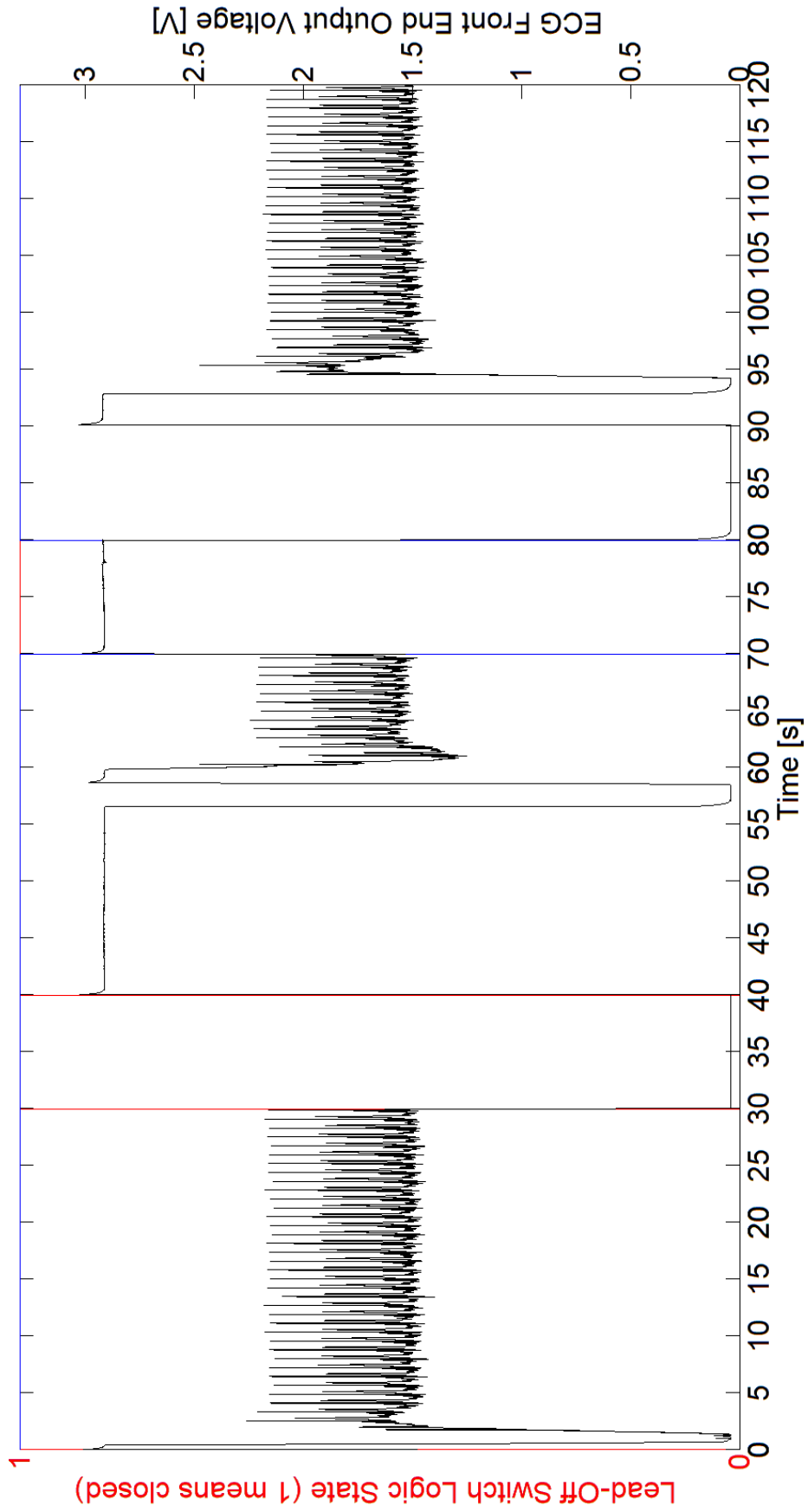


Figure 3.2.4. Lead-off performance test

3.2.5 Time Varying Skin-Electrode Resistance

In this test the skin-electrode resistance is varied over time, controlled in a square wave fashion with a frequency of 0.1 Hz. The minimum resistance value is 100 k Ω and the maximum resistance is 900 k Ω . This test simulates poor contact of the electrode with the skin. Which could be caused by variations of the pressure applied in the electrode against the skin. The remaining parameters are the same as in the previous test. The test duration is 10 seconds.

The result of the test is presented in figure 3.2.5. The right vertical axis represents the skin-electrode model capacitance in k Ω . The blue trace represents the output voltage of the DUT, the red trace represents the skin-electrode model resistance variation.

The test starts with a skin-electrode resistance of 900 k Ω , after about 4 s the ECG front-end locks the ECG signal, but with low amplitude and noise. At 5 s the impedance drops to 100 k Ω , causing the DUT to saturate. The front-end restores the signal at 9 s, now, since the impedance is much lower, the signal has much higher quality.

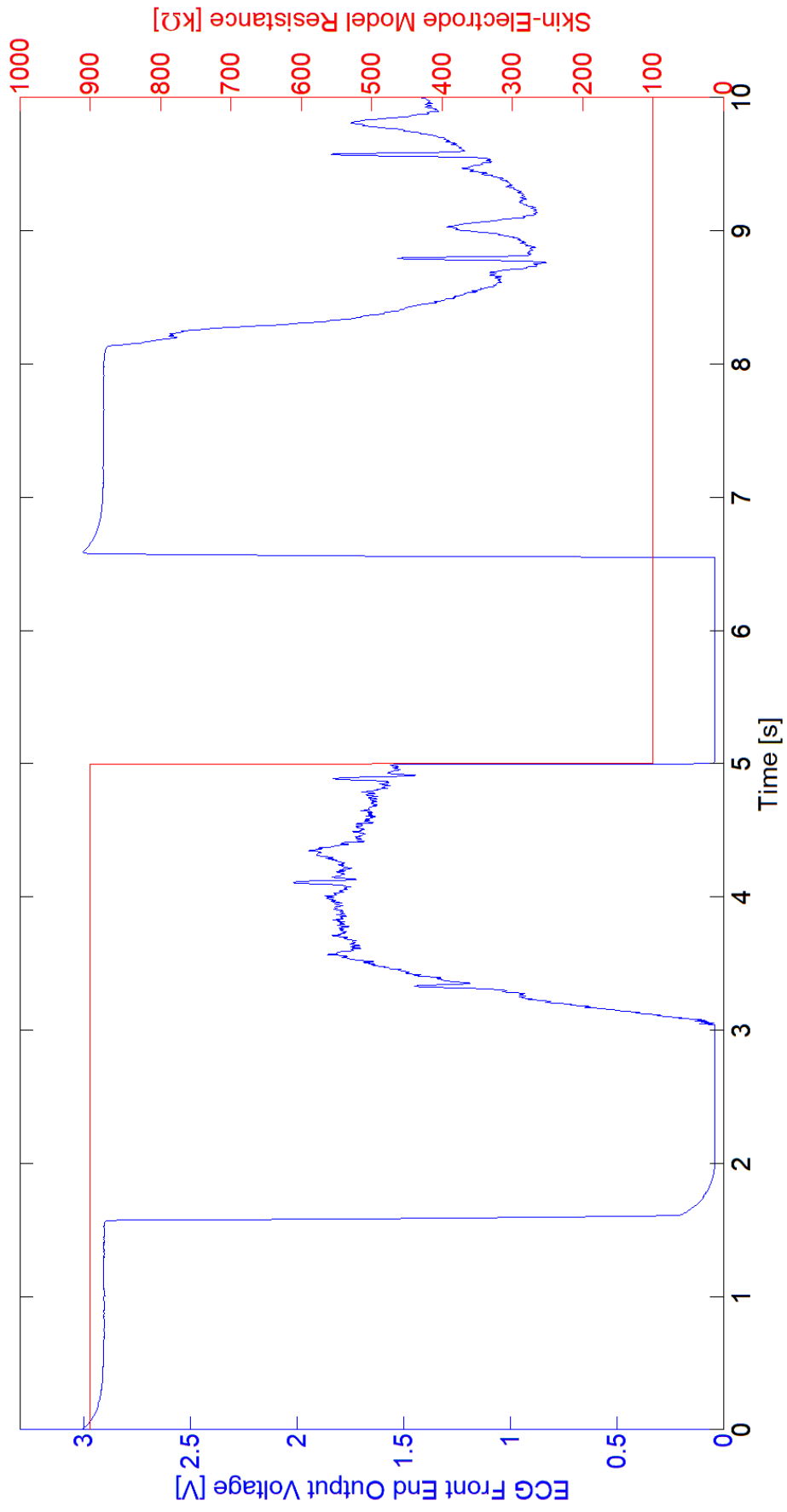


Figure 3.2.5. Time varying skin-electrode resistance test

3.2.6 Time Varying Skin-Electrode Capacitance

The capacitive component of the skin-electrode interface is varied over time, controlled by a square wave with a frequency of 0.1 Hz. The maximum capacitance is 50 nF and the minimum capacitance is 10 nF. The resistance of both electrode-skin interfaces is 100 k Ω . The remaining parameters are the same as in the previous test. This test simulates variations in the skin-electrode interface surface (area) of contact. The test duration is 10 seconds

The result of the test is shown in figure 3.2.6. The right vertical axis represents the skin-electrode model capacitance in nF. The blue trace represents the output voltage of the DUT, the red trace represents the skin-electrode model capacitance variation.

The test starts with a skin-electrode capacitance of 50 nF, this capacitance is abruptly changed to 10 nF at 5 s of test, the front-end saturates and restores the signal at about 7 s. The signal shows more noise with the higher capacitance value (50 nF).

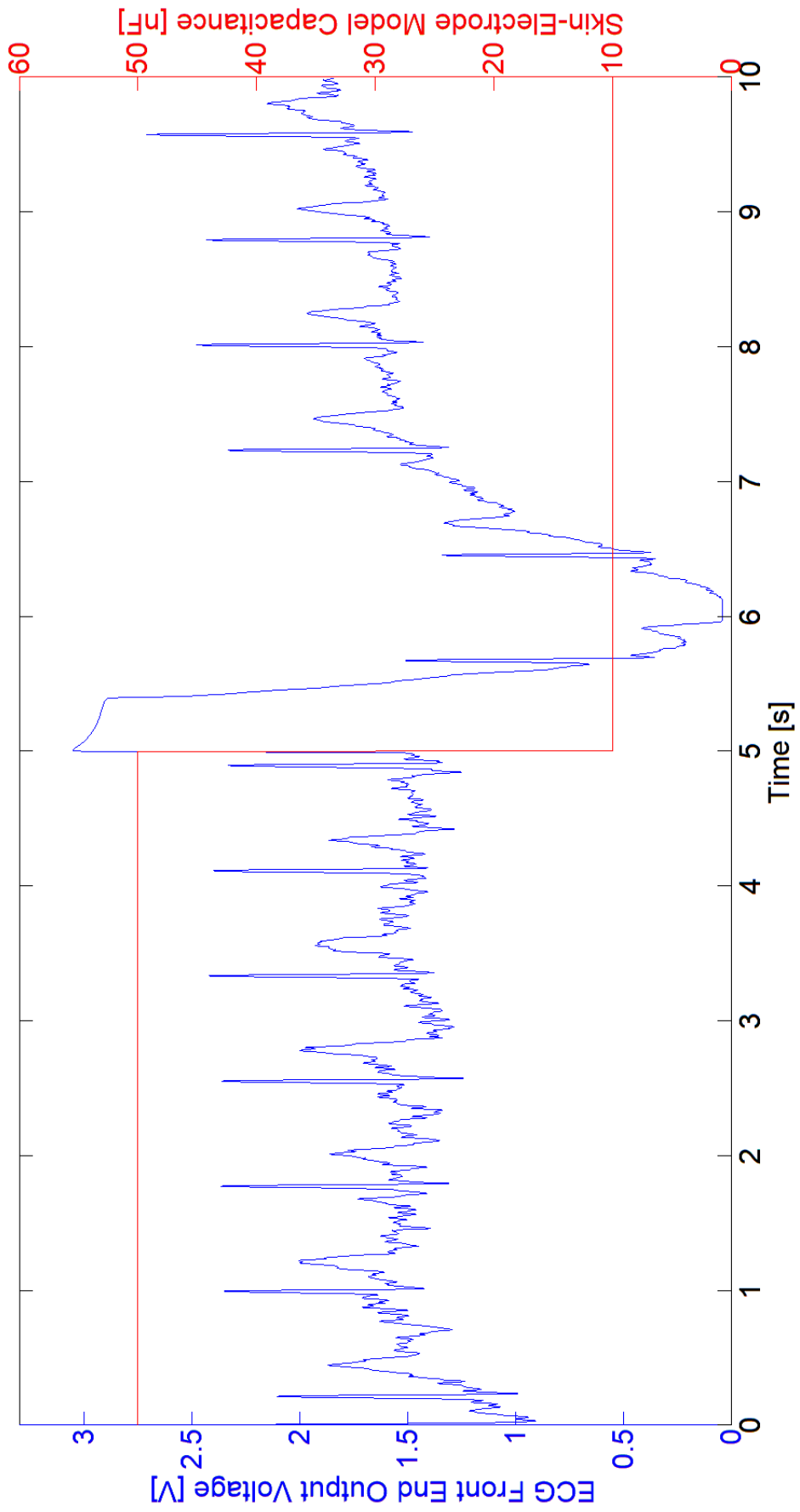


Figure 3.2.6. Time varying skin-electrode capacitance test

3.2.7 Common-mode Noise

In this test common-mode noise is added to the ECG signal, to analyze the noise performance of the front-end, with a frequency of 50 Hz and an amplitude of 100 mV. The capacitance and resistance values of the skin-electrode interface are of 47 nF and 51 k Ω , respectively. The common-mode DC component is 0 V (referenced to the supply midpoint). The amplitude of the ECG signal is 1.4 mVpp. The test duration is 10 seconds.

The result of the test is presented in figure 3.2.7. The presence of 50 Hz noise is evident, because the signal displays a thick baseline. The noise rejection performance is remarkable, the front-end is rejecting a common-mode noise signal with an amplitude of 0.1 V (0.2 Vpp), which is more than one hundred times higher than the amplitude of the ECG signal.

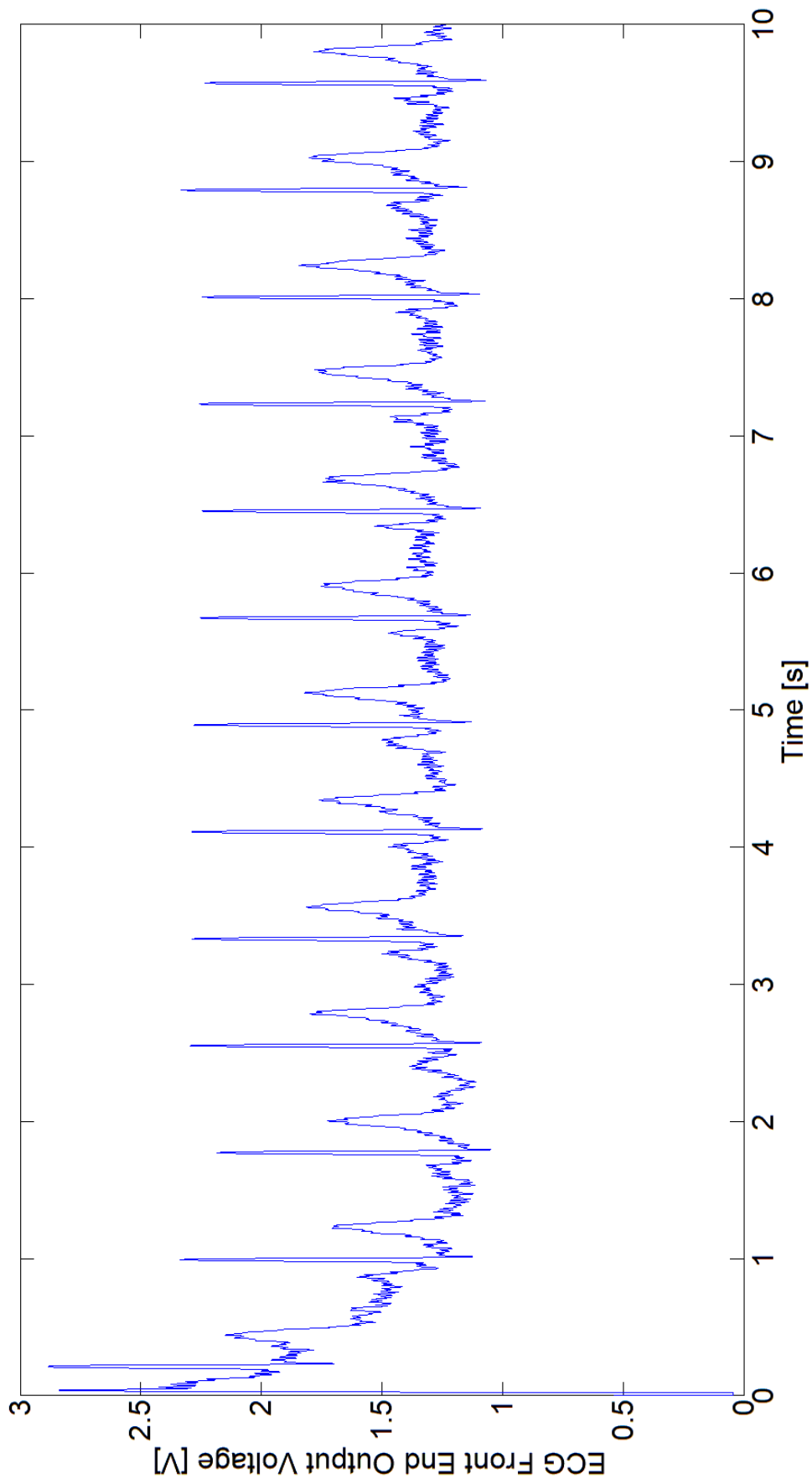


Figure 3.2.7. Common-mode noise rejection test

3.2.8 Differential Noise

In this test the noise is added to the differential component of the ECG signal, to analyze the performance of the front-end, the added noise has a frequency of 50 Hz and an amplitude of 0.1 mV. The skin-electrode interface has a capacitance of 10 nF and a resistance of 100 k Ω . The remaining parameters are the same as in the previous test. The test duration is 10 seconds.

The test result is presented in figure 3.2.8. The presence of 50 Hz noise is evident, because the signal displays a thick baseline. The differential component noise rejection performance of the ECG front end is very far from being as good as the common-mode rejection, despite having a 40 Hz low-pass filter. The interference signal in this case has an amplitude of 0.1 mV (0.2 mVpp) and the baseline is as thick as a signal with common-mode addition of an interference signal with an amplitude of 100 mV (200 mVpp).

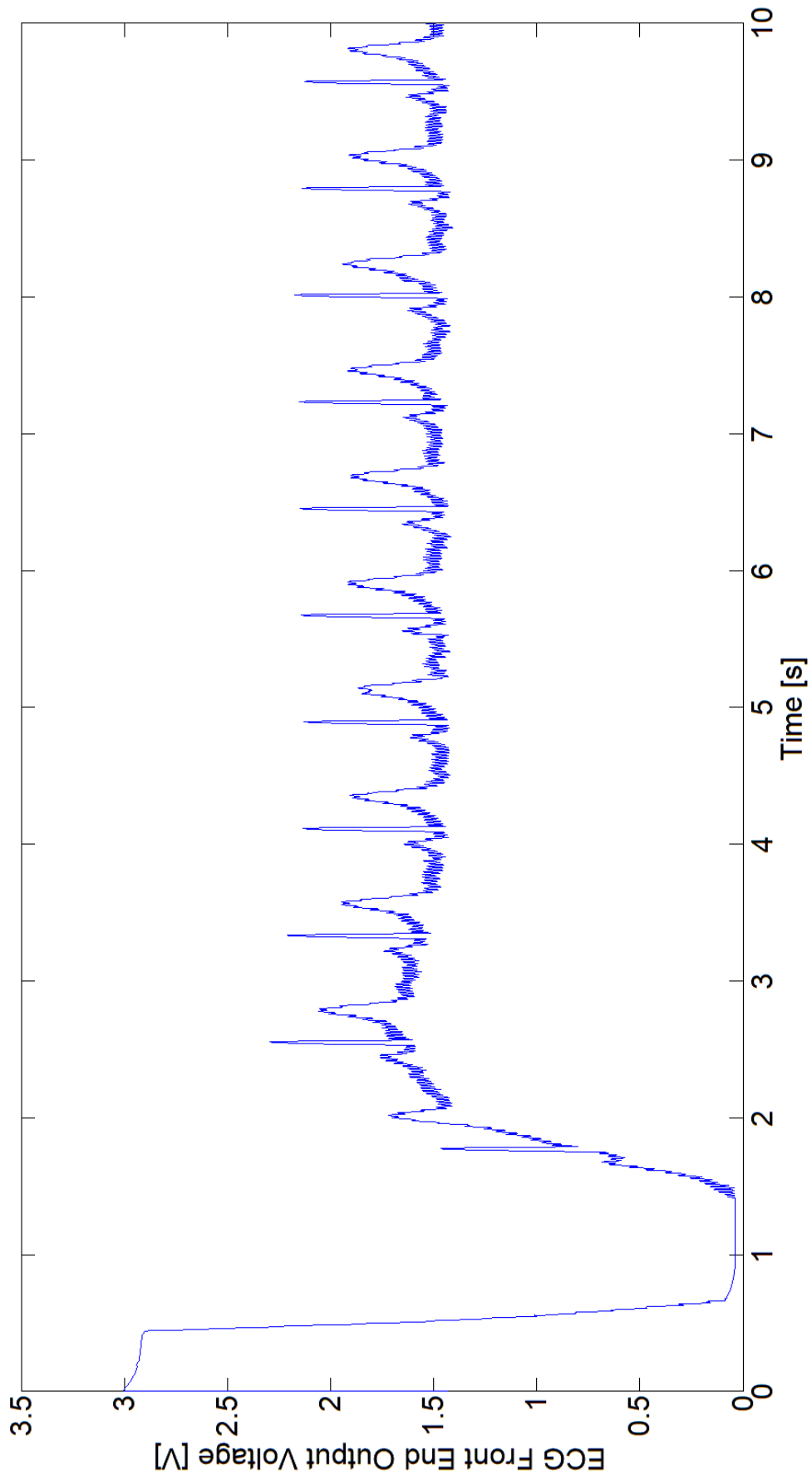


Figure 3.2.8. Differential noise rejection test

3.2.9 Baseline Wander

Baseline wander occurs due to motion of the subject and/or because of the muscular activity involved in respiration. To simulate baseline wander a differential signal with a frequency of 0.2 Hz and an amplitude of 0.5 mV is added to the ECG signal. The remaining test parameters have the same values as the previous test. The test duration is 10 seconds.

The test result is presented in figure 3.2.9. The ECG front-end features a 0.5 Hz high-pass filter, however the baseline is still being observed, if the amplitude is greater than about 0.1 mV.

3.2.10 Discussion

Overall, the tested front-end has a good performance, having a relatively low restore time, inferior to 5 seconds in most of the tests performed. It has however a relatively high restore time after lead-off, of more than 10 seconds. The common-mode noise rejection performance is much superior when compared to the differential noise rejection. The front-end also has poorer performance in the presence of high skin-electrode capacitance and resistance values.

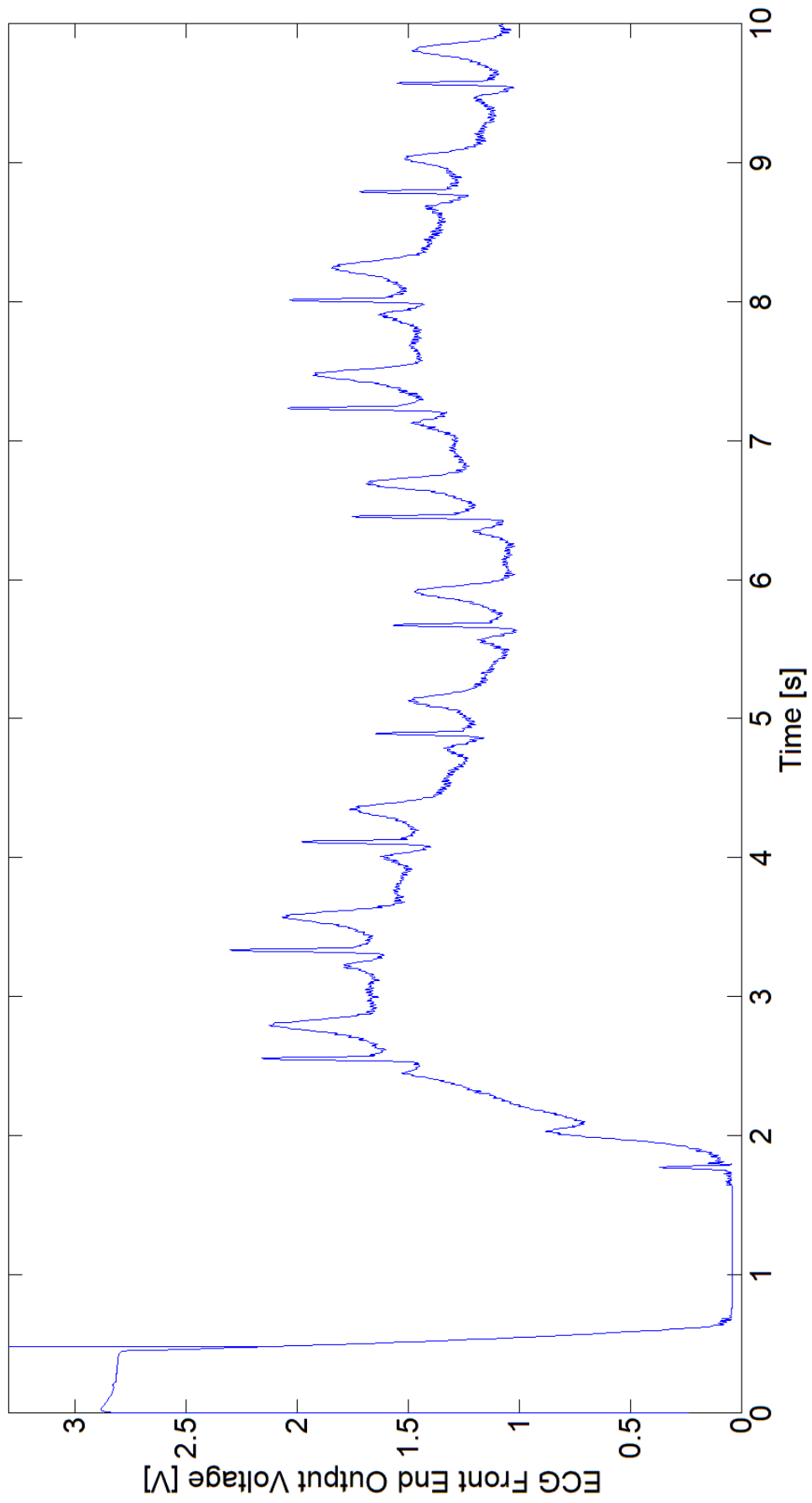


Figure 3.2.9. Baseline wander test

4 Conclusions and Future Work

In sum the objectives were achieved, the system worked as expected, being capable of providing a set of features usually not found in state of the art ECG test equipment, and allowing the realization of a set of customized tests important to evaluate the performance of electrocardiogram (ECG) front-ends. The most important tests that can be performed with this innovative system are:

- Variable impedance of skin-electrode independently adjustable in each electrode (allows the simulation of several types of electrodes, of skin and poor contact situations).
- Fully adjustable common-mode and differential ECG signal components (addition of mains interference in both components of the signal, differential and common-mode, common-mode DC variations to simulate motion of the electrodes or subject).
- Lead-off performance test (allows the realization of lead-off tests to evaluate the front-end recovery time, each electrode is individually controlled).

An innovative variable capacitance circuit was implemented and operated as supposed, allowing the simulation of capacitances between 10 nF and 100 nF. This circuit made possible the simulation of the capacitive components of the skin-electrode interface. It can be used with a high resolution and accuracy DAC to provide a very smooth and precise variation.

The maximum current consumption of the circuit is of about 250 mA, using two 1000 mAh powerbanks, the system can be operated for about 2 hours (until the battery reaches about half charge) in order to guarantee reliable operation. Of course, much larger powerbanks are available on the market, with 10000 mAh or more, with two powerbanks of this capacity the system can run for about 20 hours (until the batteries reach half charge).

A very important aspect to mention is the importance of having a stiff power supply, with large reservoir capacitors and a star ground point. These design considerations reduce significantly the noise and interference coming from the supply rails, which could severely affect the performance of a system that works with small amplitude signals and has sources of digital noise, like for example a microcontroller.

The system must always operate with batteries (powerbanks) with at least half charge, otherwise the voltage will drop and the impedance at the battery terminals increase. The ground point impedance should present the lowest possible resistance, and with low charge batteries the noise and interference rejection of the power supply can drop to unacceptable levels.

There are, however, a few negative aspects, the variable capacitance circuit, for instance, has a relatively low leakage resistance for higher capacitance values, in the order of the hundreds of kiloOhm. This can negatively impact the measurements taken, because this resistance appears in parallel with the resistance of the skin-electrode interface at higher frequencies. This aspect might be improved using a different model of operational transconductance amplifier (OTA).

The resistance simulation circuit used, an 8 bit digital potentiometer, does not allow a very smooth resistance variation for lower resistance values, the signal is varied in steps, this could affect the accuracy of the tests performed. A possible solution is a higher resolution potentiometer or a circuit based on transconductance amplifiers.

4.1 Future Work

The implemented system works as expected, however it is far from being perfect and there is plenty of room for improvement. The signal generation, lead-off, power supply, variable resistance and capacitance control sections are mounted in breadboard. A PCB would give much better results because it has less parasitic resistance, capacitance and inductance, and a lower impedance ground would definitely improve the interference and noise from the supplies. A shielded signal path with surrounding ground tracks, will increase the signal-to-interference ratio of the system, providing cleaner signals. Additionally, a Faraday cage placed in the signal generation path, connected to the circuit's ground, is also very helpful to block EMI and RFI, avoiding the interference of external signals, like for example, the mains interference, the dominant interference in ECG systems. The entire circuit, must also be isolated from external sources of interference, a metal chassis connected to the system ground is advisable, to act as an external shield, and provide further interference rejection, the enclosure must have a slot with wire connections to place the ECG front end.

The system must also be able to perform tests to digital output ECG front-ends (DUTs), and currently can only be used to test analog output DUTs, that do not feature an internal analog-to-digital converter. Additional parameters in the test file may be required to configure digital front ends.

Post processing can also be performed in the microcontroller, allowing the user to perform a series of tests and obtain the results without having to analyze the output wave in a computer, some possible tests are:

- Lead-off recovery time calculation
- Fast restore time calculation
- Signal-to-noise ratio calculation
- ECG signal distortion measurement
- Frequency domain analyzes

The results of the tests may be stored on the SD card in an additional text file created by the system.

The system could have a feature in which the user loads impedance variation WAVE files from the SD card, to perform customized impedance variation patterns. More ECG waveform files should also be added, giving freedom to the user for choosing the most adequate waveform for each test.

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Appendices

Appendix A - The Origin of Biopotentials

A biopotential by definition is an electric potential that is measured between two points in living cells, tissues or organisms, and which accompanies the biochemical processes. It corresponds to the transfer of “information” between or within cells [62].

The cell membrane is composed by a very thin (usually between 7 and 15 nm thick) lipid-protein complex, the transmembrane ion channels (that act like pores) allow the flow of ions across the membrane, this cell structure also behaves as a “leaky capacitor”, it possesses a thin dielectric material that acts as a charge separator [63].

The cell membrane is impermeable to intracellular proteins and organic anions, it is selectively permeable to sodium cations (Na^+), potassium cations (K^+) and chlorine anions (Cl^-). The concentration of potassium cations is 30-50 times greater in the intracellular medium, and the concentration of sodium cations is about 10 times greater in the extracellular medium. In resting state the cell membrane is only permeable to potassium cations, these flow outwards leaving an equal number of a anions in the intracellular medium, the electrostatic field formed (pointing in the direction of the cell nuclei), attracts the chlorine and potassium ions close to the membrane. In the excited cell state, the ion concentration across the membrane differs, creating a diffusion gradient, ions flow, creating an electric field that opposes flow, until the equilibrium is reached (similar to a PN semiconductor junction, ions flow by diffusion and create a potential difference which inhibits further flow of charged ions) [62, 63].

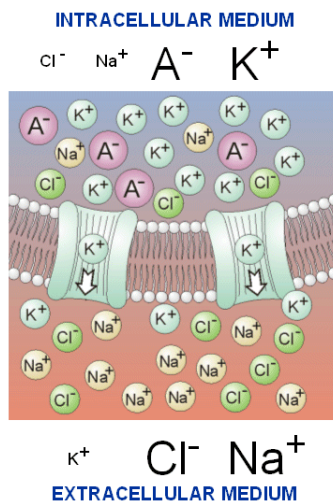


Figure 5: Ion flow in the cell membrane [64]

Equilibrium Potential

When the net current through the membrane is zero, the cell is in the resting state. The equilibrium transmembrane (resting) potential could be determined with the concentration of ions inside (in the intracellular medium) and outside the cell (in the extracellular medium), using the Nernst equation, assuming that K^+ is the main ionic species involved in the resting state ($P_k \gg P_{Na}$) [63]:

$$E_K = \frac{RT}{nF} \ln \frac{[K]_o}{[K]_i} = 0.0615 \log_{10} \frac{[K]_o}{[K]_i} [V] \quad (1)$$

Equation (1) parameters:

E_K corresponds to the cell membrane equilibrium potential for potassium, in Volt (V)

R corresponds to the universal gas constant ($\cong 8.314472(15) J \cdot mol^{-1} \cdot K^{-1}$)

T corresponds to the absolute temperature in Kelvin (K)

n corresponds to the number of (valence) electrons transferred during the reaction

F corresponds to the Faraday constant ($\cong 9.64853399(24) \times 10^4 C/mol$)

$[K]_o$ corresponds to the concentration of potassium cations (K^+) in the extracellular medium, the unit is mol/l or mol/dm^3

$[K]_i$ corresponds to the concentration of potassium cations (K^+) in the intracellular medium, the unit is mol/l or mol/dm^3

The Nernst equation is incomplete because it only has in account the concentration of potassium cations, and though these ions play the main role, they are not the only species involved in the formation of biopotentials. The Goldman-Hodgkin-Katz (GHK) formulation accounts for other ionic species in the intracellular/extracellular medium [63]:

$$E_{m, K_xNa_{1-x}Cl} = \frac{RT}{F} \ln \left\{ \frac{P_K[K]_o + P_{Na}[Na]_o + P_{Cl}[Cl]_i}{P_K[K]_i + P_{Na}[Na]_i + P_{Cl}[Cl]_o} \right\} [V] \quad (2)$$

Equation (2) parameters:

$E_{m, K_xNa_{1-x}Cl}$ corresponds to the cell membrane potential in Volt (V)

R corresponds to the universal gas constant ($\cong 8.314472(15) J \cdot mol^{-1} \cdot K^{-1}$)

T corresponds to the absolute temperature in Kelvin (K)

F corresponds to the Faraday constant ($\cong 9.64853399(24) \times 10^4 C/mol$)

P_{ion} corresponds to the permeability coefficient of the membrane for a specific ionic species (K, Na or Cl) in m/s

$[ion]_o$ corresponds to the ion concentration of a specific species (K, Na or Cl) in the extracellular medium, the unit is mol/m^3

$[ion]_i$ corresponds to the ion concentration of a specific species (K, Na or Cl) in the intracellular medium, the unit is mol/m^3

The Resting State

The excitable cells maintain a steady potential difference between the extracellular and intracellular medium (usually between 50 mV and 100 mV). In excitable cells the membrane is slightly permeable to sodium cations (Na^+) and freely permeable to potassium cations and chloride anions (K^+ and Cl^-). The table shows an example of the concentration of major species of ions from a frog skeletal muscle, it shows the buildup of potassium cations in the intracellular medium, sodium cations and chloride anions in the extracellular medium [63].

Assuming a temperature room temperature of 20 °C (293 K) and the typical values of ion permeability coefficient for the frog skeletal muscles ($P_K = 2 \times 10^{-6} \text{ cm/s}$, $P_{Cl} = 4 \times 10^{-6} \text{ cm/s}$, $P_{Na} = 2 \times 10^{-8} \text{ cm/s}$), the following concentration of ions was observed [63].

Ion Species	Intracellular Medium Ion Concentration [mmol/l]	Extracellular Medium Ion Concentration [mmol/l]
Na^+	12	145
K^+	155	4
Cl^-	4	120

The equilibrium potential could now be calculated using the Goldman-Hodgkin-Katz (GHK) formulation [63].

$$\begin{aligned}
 E &= 0.0581 \log_{10} \left[\frac{P_K(4) + P_{Na}(145) + P_{Cl}(4)}{P_K(155) + P_{Na}(12) + P_{Cl}(120)} \right] = \\
 &= 0.0581 \log_{10} \left[\frac{26.9 \times 10^{-6}}{790.24 \times 10^{-6}} \right] = -85.3 \text{ mV}
 \end{aligned}$$

Sodium-Potassium Pump

A continuous transport of ions against electrochemical gradients is required to maintain a steady state ionic imbalance. The sodium-potassium pump actively transports sodium cations to the extracellular medium and potassium cations to the intracellular medium in the 3:2 (1.5) ratio, 3 Na⁺ ions per 2 K⁺ ions. The associated pump current (i_{NaK}) is an outward current that tends to increase the negativity of the intracellular potential. Energy for the pump is provided by Adenosine Triphosphate (ATP) produced by mitochondria in the cell [63]. The factors that influence the flow of ions in the cell membrane are:

- Diffusion gradients
- Inward directed electric field
- Availability of pores
- Active ion transport against an established electrochemical gradient

Action Potential

Action potential is a brief transient disturbance of membrane potential, due to a stimulus adequate to bring about depolarization sufficient to exceed the threshold potential. The action potential occurs when membrane stimulation exceeds a threshold value of about 20 mV. The action potential develops in 4 steps [62, 63]:

1. The permeability of the cell membrane to sodium and potassium cations changes
2. Permeability of the cell membrane to sodium cations increase rapidly, allowing the ions to flow from the extracellular medium to the intracellular medium, making the inner side of the membrane more positive
3. Permeability of the cell membrane to potassium cations increase slowly, allowing these ions to flow from the intracellular medium to the extracellular medium, making the cell return to the resting potential
4. The cell reaches the rest state and the sodium-potassium pump restore the ion concentrations to the initial values

In the excited state the flux of ions per open channel is greater than one million per second and since the body behaves as an inhomogeneous volume conductor, the ion fluxes develop measurable voltage potentials on the body surface [62].

The Polarization States of The Cell Membrane

There are three polarization states, the polarized state in which the cell remains at the steady resting potential, the depolarized state, when the magnitude of the membrane potential decreases, and the hyperpolarized state, that corresponds to an increase in the magnitude of the membrane potential [63].

As previously stated, the action potential is a brief transient disturbance of the membrane potential, a change in the membrane potential due to a stimulus, which brings about depolarization enough to exceed the threshold potential level. The repolarization is the state that occurs when the membrane returns to equilibrium after the action potential [63].

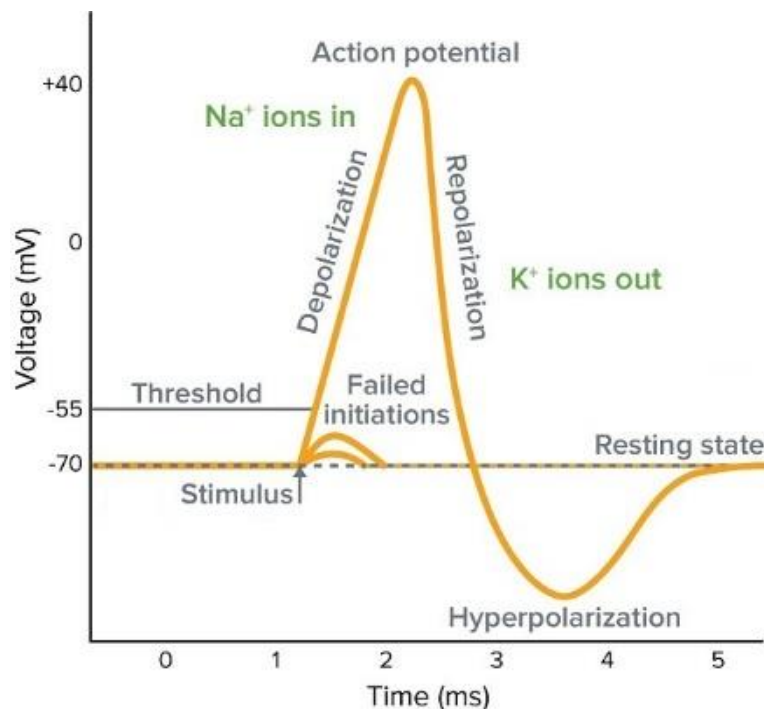


Figure 6: Variation of membrane potential over time, showing the action potential [65]

The Circuit Model of the Axon

Ludvig Hermann, suggested that under subthreshold conditions, the cell membrane can be described by a uniformly distributed leakage resistance and parallel capacitance. A theoretical circuit could be elaborated to evaluate the response to an arbitrary current stimulus. The resistive component, shown in figure 3 takes in account the ionic membrane current (i_{mi}). The capacitance shows that the membrane behaves as a poor conductor, but is a good dielectric, as a consequence, the current (i_{mc}) must be included as a component of the cell membrane electric current. The axial paths (intracellular and extracellular) are entirely resistive [65].

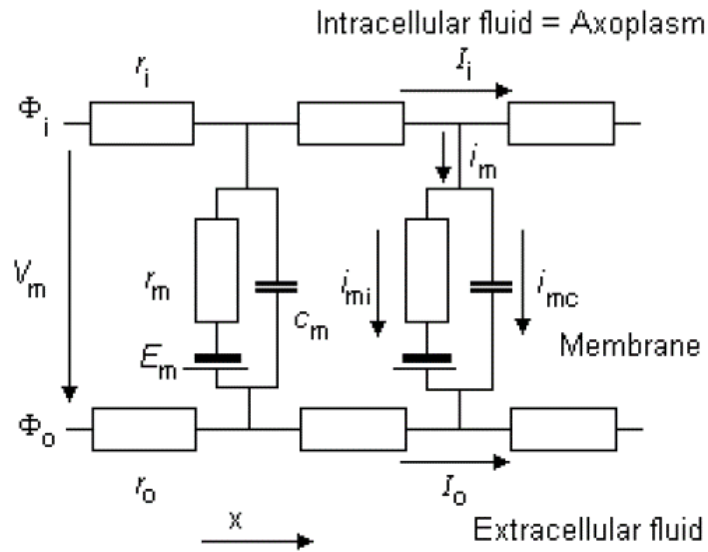


Figure 7: Equivalent Circuit Model of the Axon [65]

Description of the symbols of figure 3:

r_i corresponds to the intracellular axial resistance of the axoplasm per unit length of the axon [$k\Omega/cm$]

r_o corresponds to the extracellular axial resistance of the bounding extracellular medium per unit length of the axon [$k\Omega/cm$]

r_m corresponds to the product between the membrane resistance and the unit length of the axon (in the radial direction) [$k\Omega \cdot cm$]

c_m corresponds to the membrane capacitance per unit of length of the axon [$\mu F/cm$]

I_i corresponds to the total longitudinal intracellular current [μA]

I_o corresponds to the total longitudinal extracellular current [μA]

i_m corresponds to the total transmembrane current per unit length of the axon [$\mu A/cm$] (measured in the radial direction)

i_{mc} corresponds to the capacitive component of the transmembrane current per unit length of the axon [$\mu A/cm$] (measured in the radial direction)

i_{mi} corresponds to the ionic component of the transmembrane current per unit length of the axon [$\mu A/cm$] (measured in the radial direction)

Φ_i corresponds to the voltage potential inside the membrane [mV]

Φ_o corresponds to the voltage potential outside the membrane [mV]

$V_m = \Phi_i - \Phi_o$ corresponds to the membrane voltage [mV]

Appendix B - Electrocardiography Fundamentals

The electrocardiogram (ECG) is a linear graphic recording of the electrical impulses generated by the heart during the cardiac cycle. The electrical impulses are measured by an instrument and the electrical current is picked up by electrodes placed in contact with the patient's skin. The ECG equipment displays the voltage measured differentially between a pair of electrodes. The horizontal axis represents the time and the vertical axis the voltage. This medical examination is used for monitoring purposes, to check the heart rate and identify abnormalities in the heart's electrical activity [66].

Nerve Supply to the Heart

The heart is supplied by the two branches of nerves of the autonomic nervous system, the sympathetic (adrenergic) and the parasympathetic (cholinergic). The sympathetic nervous system is the responsible for increases in the heart rate. Norepinephrine and Epinephrine are the chemicals responsible to increase the heart rate, automaticity, AV conduction and contractility. The parasympathetic (cholinergic) nervous system is responsible for decreasing the heart rate. The vagus nerve, carries the impulses responsible to slow the heart rate and conducts the impulses through the AV node and ventricles. The stimulation of the parasympathetic system release a chemical called acetylcholine, which is responsible for slowing the heart rate. The vagus nerve is stimulated by the baroreceptors (which act like pressure sensors), specialized nerves cells, located in the aorta and in the internal carotid arteries. When the baroreceptors are stimulated (when the pressure increases) the vagus nerve is also stimulated. For example, during hypertension periods, the baroreceptors stretch and become activated [67].

Transmission of Electrical Impulses in the Heart

The heart pumps the blood through the body due to an electrical stimulus. The generation and transmission of the electrical impulses depends on four characteristics of the cardiac cells [67]:

- **Automaticity** corresponds to the ability of a cell to spontaneously initiate an impulse. The pacemaker cells exhibit this behavior.
- **Excitability** is the result of ion shifts across the cell membrane which indicates the ability of a cell to respond to a stimulus.
- **Conductivity** is the ability that a cell have to transmit an electrical impulse
- **Contractility** refers to the ability a cell have to contract after receiving a stimulus

During the time the impulses are being transmitted, the cardiac cells undergo cycles of depolarization and repolarization. At rest, the cardiac cells remain in the polarized state, during this state there is no electrical activity [67].

The cell membrane separates the intracellular medium from the extracellular medium, the ion concentration (of sodium and potassium) on these two mediums differs and creates a negative charge inside the cell. This is called the resting potential. After a stimulus, the flow of ions across the cell membrane causes an action potential, also called cell depolarization. When the cell reaches full depolarization, it attempts to return to the rest state, this process is called repolarization. The flow of ions reverses and the electrical charges return to the normal values. A depolarization-repolarization cycle consists of five phases (numbered 0 to 4). The action potential is represented by a curve which represents the voltage changes during the five phases [67].

During phase 0, the cell receives an impulse from a neighbor cell and becomes depolarized. Phase 1 is characterized by early, rapid repolarization. Phase 2, called the *plateau phase*, is a period of slow repolarization. During the phases 1, 2, and also in the beginning of phase 3, the cardiac cell is said to be in the absolute refractory period. In this period, the cell cannot be excited, independently of the presence of a stimulus or its strength. Phase 3 is the rapid repolarization phase, which occurs as the cell returns to the original state. In the last half of this phase, while the cell is in its refractory period, a very strong stimulus could cause depolarization. Phase 4 corresponds to the resting phase of the action potential. At the end of this phase, the cell is ready to respond to another stimulus. The resulting electrical activity (of the four phases) is represented in the electrocardiogram (ECG) [67].

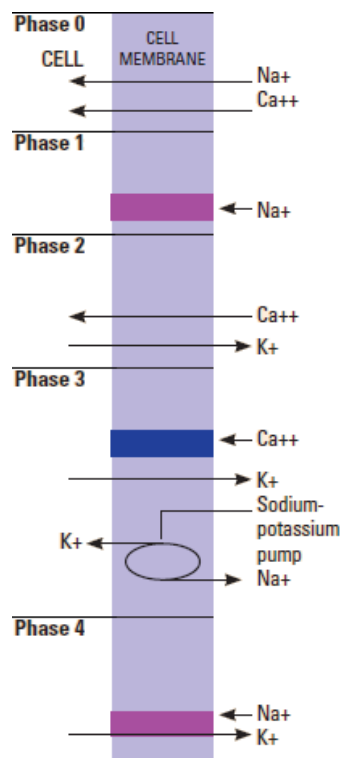


Figure 8: The five phases of the depolarization-repolarization cycle [67]

The flow of ions throughout the phases of the cardiac cells depolarization-repolarization cycle is represented in figure 1. During the depolarization-repolarization cycle, the ions flow as follows [67]:

- **Phase 0** is the phase of **rapid depolarization**, the sodium cations (Na^+) flow rapidly and the calcium cations (Ca^{2+}) flow slowly, from the extracellular medium to the intracellular medium.
- **Phase 1** is the **Early repolarization**, in this phase the sodium channels close and the cell membrane becomes impermeable to sodium cations (Na^+).
- **Phase 2** is the **Plateau phase**, during this phase the calcium cations (Ca^{2+}) continue to flow from the extracellular medium to the intracellular medium and the potassium cations (K^+) flow in the opposite direction.
- **Phase 3** is the phase of **rapid repolarization**, in this phase the calcium channels close, making the cell membrane impermeable to calcium ions (Ca^{2+}), the potassium cations flow rapidly from the intracellular medium to the extracellular medium. The sodium-potassium pump performs the active transport of ions, the potassium cations (K^+) are transferred from the extracellular medium to the intracellular medium and the sodium cations (Na^+) are transferred to the extracellular medium from the intracellular medium.
- **Phase 4** is called the **resting phase**, the cell membrane is impermeable to sodium cations (Na^+), potassium cations (K^+) flow from the intracellular medium to the extracellular medium.

The action potential curve shows the voltage variations in a myocardial cell during the depolarization-repolarization cycle. The graph represented in figure 2, shows the voltage variations in a non-pacemaker cell [67].

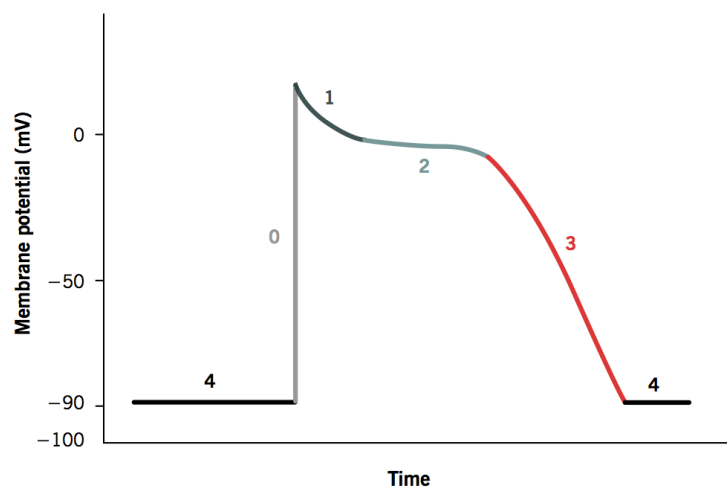


Figure 9: Action potential curve of a non-pacemaker myocardial cell, the phases of the depolarization-repolarization cycle are represent by numbers from 0 to 4 [68]

The Cardiac Conduction System

After depolarization and repolarization occurs, the resulting electrical impulse flow through the heart following a path called the **conduction system**. The impulses flow from the SA (sinoatrial) node and through the inter-nodal tracts and Bachmann's bundle to the AV (atrioventricular) node. Then the impulses flow through the bundle of His, the bundle branches, and finally it reaches the Purkinje fibers [67].

The SA (sinoatrial) node is located in the upper right corner of the right atrium, where the superior vena cava joins the atrial tissue mass. This node acts as the heart's main pacemaker, generating impulses at 60 to 100 times per minute. The impulses generated in the SA node, follow a specific path through the heart. Since the cells are unable to respond to a stimulus immediately after depolarization (during the refractory period), the impulses usually will not flow in the opposite direction [67].

The electrical impulses are propagated throughout the heart by specialized fibers, causing the heart to contract (figure 3) [67].

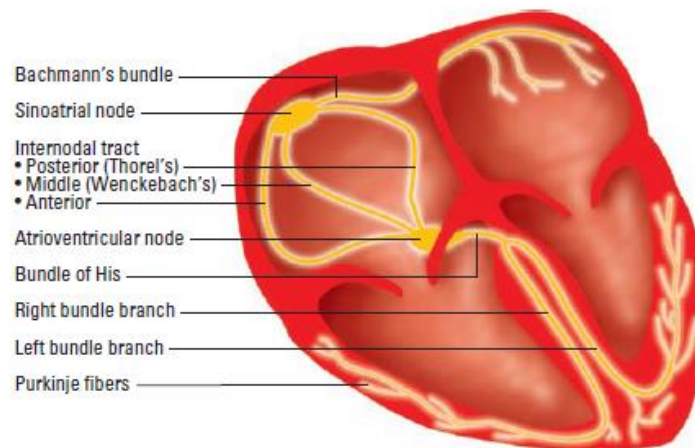


Figure 10: Elements of the cardiac conduction system [67]

Impulses from the SA (sinoatrial) node flow through the Bachmann bundle, tracts of tissue, extending from the SA node to the left atrium. The electrical impulses are thought to be transmitted throughout the right atrium through the anterior, middle, and posterior intermodal tracts. It is, however, unclear, if those tracts actually exist, since impulse transmission through the right and left atria occurs so rapidly that the contraction of the atria occurs almost simultaneously [67].

The AV (atrioventricular) node is located in the inferior right atrium near the ostium of the coronary sinus, it is responsible for delaying the impulses that reach it [67].

The nodal tissue itself does not contain pacemaker cells, the tissue surrounding it (junctional tissue) contains pacemaker cells, which generate impulses at a rate of 40 to 60 times per minute. The delay imposed by the AV node is of about 0.04 seconds, to prevent the ventricles from contracting too rapidly. This delay allows the filling phase of the ventricles to be completed as the atria contracts. The delay also allows the cardiac muscle to fully stretch to achieve peak cardiac output [67].

The tract of tissue extending into the ventricles next to the interventricular septum is called bundle of His, and it resumes the rapid conduction of the impulse through the ventricles. The bundle of His, divides into the left and right bundle branches. The right bundle branch extends down the right side of the interventricular septum and through the right ventricle. The left bundle branch extends down the left side of the interventricular septum and through the left ventricle. The left bundle branch splits into two branches, the left anterior fasciculus, extending through the anterior portion of the left ventricle, and the left posterior fasciculus, which runs through the lateral and posterior portions of the left ventricle. The impulses travel much faster in the left bundle branch (which feeds the larger and thicker walled left ventricle) in comparison with the right bundle branch (which feeds the smaller, thinner-walled right ventricle). The difference in conduction speed allow both ventricles to contract simultaneously. The network of nervous tissue that extends through the ventricles is called His-Purkinje system [67].

The Purkinje fibers extend from the bundle branches to the endocardium, deep into the myocardial tissue. These fibers are responsible for the rapid conduction of impulses through the cardiac muscle, to assist in its depolarization and contraction. The Purkinje fibers also actuate as pacemaker, able to supply impulses at a rate of 20 to 40 times per minute and sometimes at an even slower rate. It is not normal for the Purkinje fibers to act as a pacemaker, it only occurs when there is a blockage of the bundle of His (conduction defect), or if a higher pacemaker node, like the SA or AV node is not generating impulses [67].

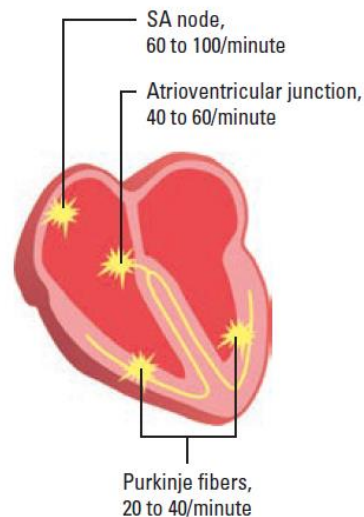


Figure 11: Impulse generation rate of the pacemaker cells located in the three critical areas of the heart [67]

ECG recordings

The electrical activity of the heart produces currents that radiate through the surrounding tissues to the skin. Electrodes attached to the skin, sense the currents generated by the heart and transmit them to the ECG equipment. The currents are transformed into a waveform and the heart's depolarization-repolarization cycle is graphically represented. The ECG trace shows the precise sequence of electrical events occurring in the heart cells throughout the depolarization-repolarization cycle. The ECG trace is then used by medicine practitioners to assess cardiac function, by the identification of rhythm and conduction disturbances [67].

ECG Leads

The electrodes placed in the skin measure the direction of the electrical current generated by the heart. A lead provides information about the heart's electrical activity between a negative pole and a positive pole. Between the two poles an imaginary line represents the lead axis, a term that refers to the direction of the current flowing in the heart. The direction of the current influences the direction in which the waveform points in the ECG (figure 5) [67].

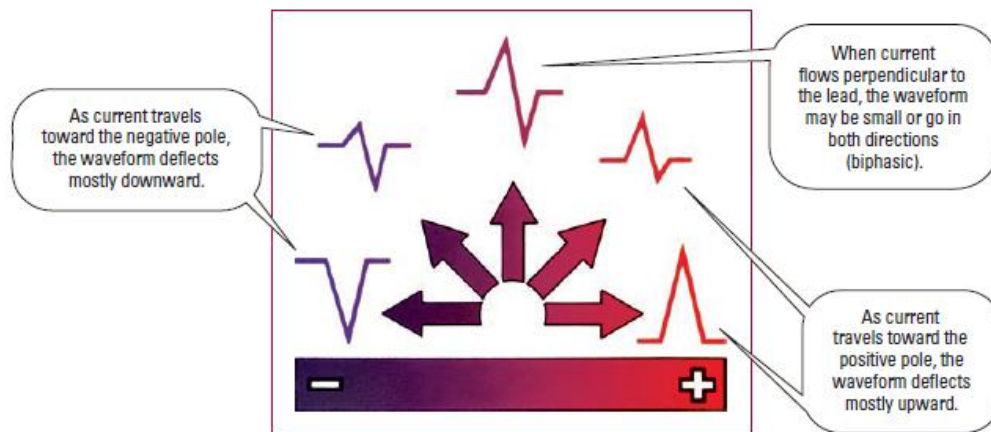


Figure 12: Possible directions of electrical current (depolarization) on a lead. The direction of the current determines the upward or downward deflection of the electrocardiographic waveform [67]

The Einthoven's triangle (figure 6), defines the positioning of the standard limb leads. The electrode leads numbered I to III are about equidistant to the heart and form an equilateral triangle. The lead I axis extends from shoulder to shoulder, the right arm electrode is the negative and the left arm electrode is the positive. The lead II axis extends from the right arm to the left leg, the negative electrode is positioned on the right arm and the positive electrode is positioned in the left leg. The lead III axis extends from the left arm to the left leg, the negative electrode is placed on the left arm and the positive electrode is positioned on the left leg. A third electrode (generally placed on the right leg or sometimes in the chest) may be present, the reference electrode, the addition of this electrode improves interference and noise rejection. The leads labeled aVR, aVL and aVF are called **augmented leads**, because the weak signals coming from these unipolar (single-ended) leads are enhanced by the ECG. The "a" stands for augmented, and R, L and F is related to the position of the positive electrode **R**ight arm, **L**eft arm, **F**ront (left leg). These three leads provide information about electrical activity of the heart in the frontal plane [67].

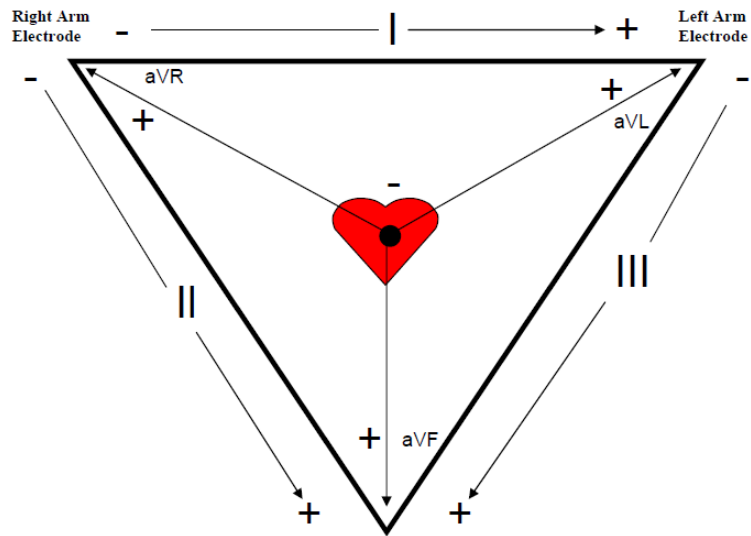


Figure 13: The Einthoven's triangle defines the positioning of the standard limb leads (used in the first electrocardiograms recorded) [66]

Appendix C - Electrocardiography History

Knowledge of bioelectricity started with the observation of Luigi Galvani [69] that a frog muscle contracted when exposed to electrical discharging process. Galvani postulated the idea of animal electricity, which was for a long time opposed by Alessandro Volta. After the development of sensitive galvanometers, it was possible to prove that there are charges and currents within the frog itself. Matteucci demonstrated in 1843 that also from the resting heart muscle electrical current could be measured [70]. DuBois-Reymond investigated these phenomena in more detail and introduced the term “action potential” for the electrical current changes associated to muscle contraction [adapted from 71]. The action current accompanying a spontaneous beating heart, associated with the systolic shorting of the myocardial fibers, has first been observed by Koelliker and Müller [72, 73].

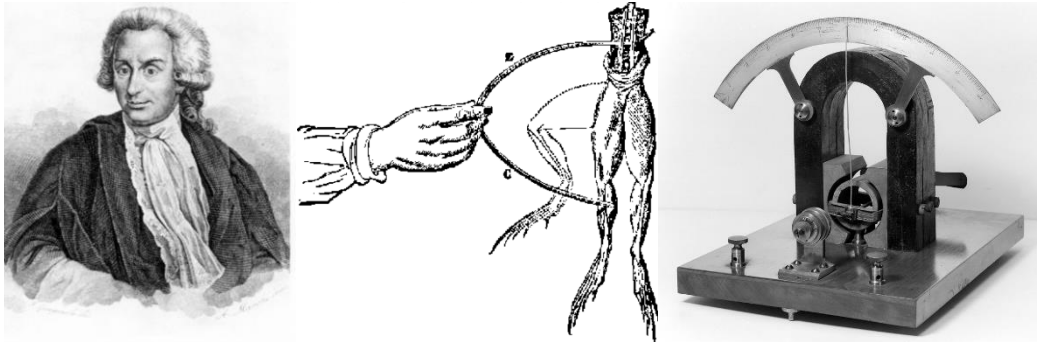


Figure 14: Luigi Galvani (1737-1798), physician famous for pioneering bioelectricity [74] (left), the frog experiment conducted by Luigi Galvani, suggesting the existence of bioelectricity [75] (center), an early galvanometer used to measure electrical currents, designed by D'Arsonval [76] (right)

The Electrocardiograph and its Precursors

The first galvanometer (equipment used to measure current variations) was the “rheoscopic frog”, an experiment conducted by Matteucci, showing that a muscle could be made to contract, when its nerve was brought in contact with a second muscle, which was in an excited state [adapted from 77]. Du-Bois Reymond demonstrated in 1843 the action potential of a skeletal muscle. He found that the repeated stimulation of the nerve of a partly injured muscle, resulted in diminution of the potential difference, between injured and uninjured muscle. This diminution of the injury potential, was a result of the action potential, which DuBois-Reymond referred to as “negative variation” [77].

Kölliker and Müller, in 1856, showed that the negative variation could be observed on a beating heart. They applied the nerve of a rheoscopic limb, to the pulsating ventricle, and showed that the muscles of the preparation contracted, a “scarcely perceptible time before systole”. Donders, in 1872, and Engelmann, in 1873, confirmed and extended the observation of Kölliker and Müller [77].

By the 1870's the electromotive phenomena of cardiac muscle were well established. Subsequent knowledge of the nature of these phenomena, depended on the development of suitable instruments, with which to record electric potentials generated by the heart [77].

The "reoscopic frog limb", only allowed the electrical current to be sensed, rather than measured. The galvanometers with the precision required to measure the action currents of living tissues, only came into existence in 1825 (Nobili, 1825; Schweigger, 1826) [adapted from 77]. Early galvanometers, where of the moving-coil type, and, although astatic, they were relatively insensitive [77].

In 1849, DuBois-Reymond attempted to construct an instrument which could measure bioelectric currents, with greater sensitivity than was possible with the galvanometers available at the time [77]. The instrument developed was a galvanometer with a two position switch, in one position the device generates a stimulus and disconnects to the tissue, in the other position the tissue was connected to the galvanometer and the stimulus was interrupted. This instrument was used to sample the magnitude of the electric current for brief times, it was called the "rheotome" [adapted from 77]. The rheotome was modified by many physiologists and physicists, notably by Lenz, who in 1854, developed a method for constructing a time-course curve of the variations in the electric current during a single induction cycle. The construction of such curves, was impossible before the development of the rheotome, because the available galvanometers moved too slowly [77]. Lenz, was the first to course the variation in intensity of an alternating current [adapted from 77].

Juilius Bernstein (1839-1917), a pupil of DuBois-Reymond, was interested in plotting the time course of the negative variation (action current). To accomplish this, he modified the rheotome so that the interval between stimulation and sampling could be varied. This instrument, introduced in 1868, was called "the differencial rheotome" (showed in figure 2). The first electrocardiograms ever recorded were obtained with Bernstein's differencial rheotome [77].

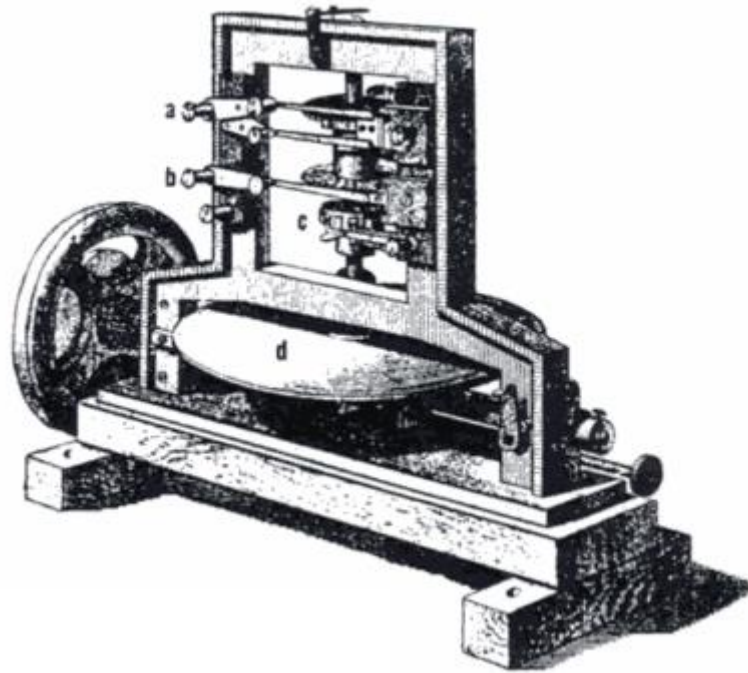


Figure 15: The Bernstein's Differential Rheotome, the first device used to obtain an electrocardiogram, the first “electrocardiograph” [77]

Although the differential rheotome could record the time course of the variations of cardiac action potentials, the instrument lacked sensitivity. A more satisfactory instrument for measuring bioelectric currents was devised by Gabriel Lippmann (1845-1921) in 1872. This instrument, the “capillary electrometer” (figure 3), had great sensitivity, which made it immediately popular amongst electrophysiologists [77].

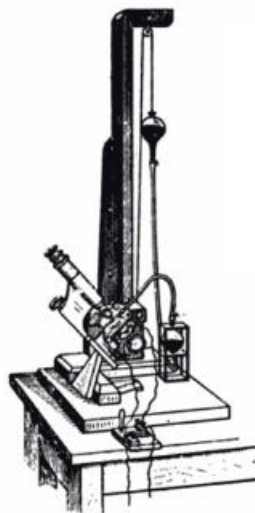


Figure 16: The capillary electrometer as constructed by Lippmann in 1872 [77]

Einthoven started using existent galvanometers for his purposes, most of the devices available at the time were of the moving-coil type, like, for example, the D'Arsonval galvanometer (described by Jacques Arsène d'Arsonval in 1889). These instruments, consisted of a coiled wire suspended with magnetic field of a permanent magnet. Variations in the intensity of current passing through the coil caused it to move, this movement was recorded by mirrors or other devices. In 1900, Willem Einthoven started to design and construct his own galvanometer [adapted from 77]. The fruit of Einthoven's efforts, was the development of a sensitive, rugged, and ideal instrument for recording potential variations from the heart, the "string galvanometer" [77].

Einthoven first described the string galvanometer in a preliminary report published in 1901, although the date usually ascribed to the Einthoven electrocardiograph is 1903, the date of the publication of a detailed description of the string galvanometer, and a comparison between the records obtained with this device and the capillary electrometer. This device was the first to make electrocardiography possible and literally created a new branch in medicine [adapted from 77].

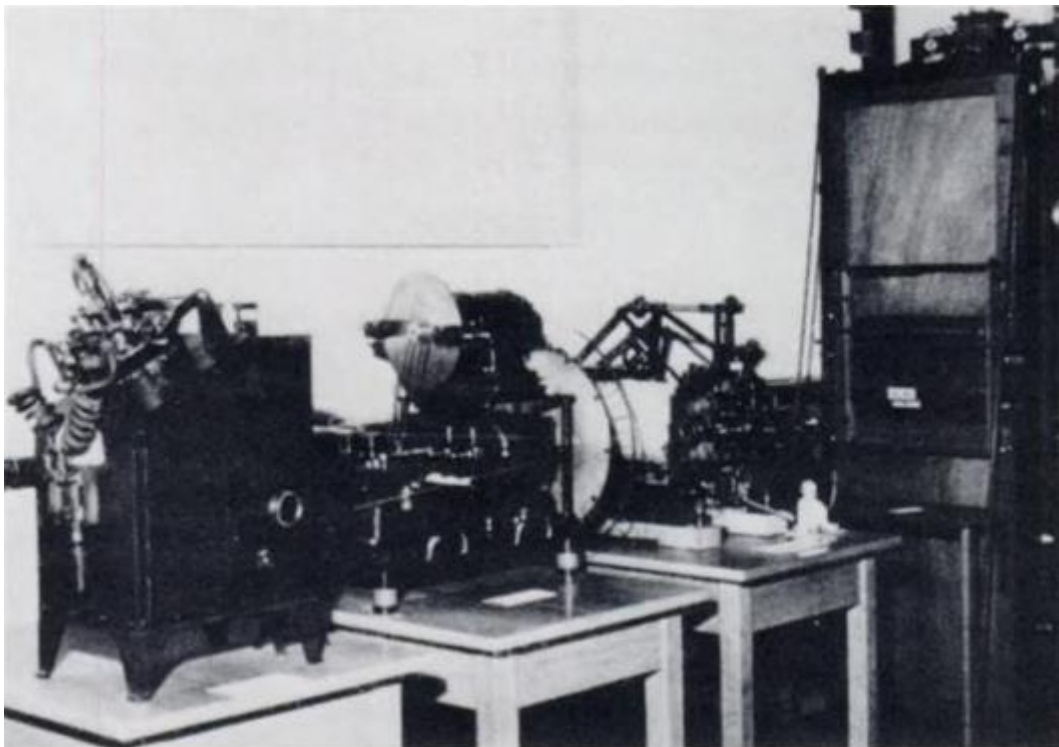


Figure 17: Einthoven's original string galvanometer on display in the museum of the University of Leiden, during the centennial celebration of the birth of Einthoven, in June, 1960. The unit on the left is an arc lamp. The unit on the center is a water-cooled electromagnet, capable of producing a 22 kGauss field. The unit on the right is the projection lens system. The independent timer with its spokes, is situated between the electromagnet and the lens system. The large panel on the right is the falling-glass-plate camera. The entire instrument was constructed in Einthoven's laboratory. (Photograph courtesy of Professor H. A. Snellen of the University of Leiden, School of Medicine.) [77]

As the string galvanometer electrocardiograph became available for clinical use, improvements were made to make it more practical. Earlier electrocardiograms recorded by Waller used five electrodes, one on each of the four extremities of the mouth, with 10 leads derived from the different combinations [78]. Einthoven was able to reduce the number of electrodes to three, by excluding those which he thought provided the lowest yield, the right leg and mouth electrodes. The resulting three leads were used to construct Einthoven's triangle (figure 5), an important concept to this day [79]. In 1924, Einthoven was awarded the Nobel Prize in physiology and medicine, for the invention of the electrocardiograph [80].

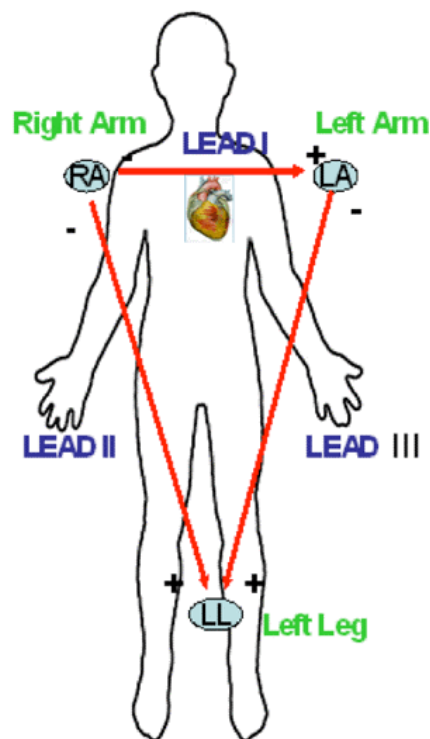


Figure 18: The Einthoven's triangle, showing the position of the electrodes [81]

The first electrodes were cylinders of electrolyte solution in which extremities were rinsed (as can be seen on figure 6) [77]. The positive leads were placed on the left arm and leg, to produce deflections on electrocardiogram tracing as the normal electrical activation of the heart, was noted to be from the right-upper quadrant to the left-lower quadrant [77, 80].

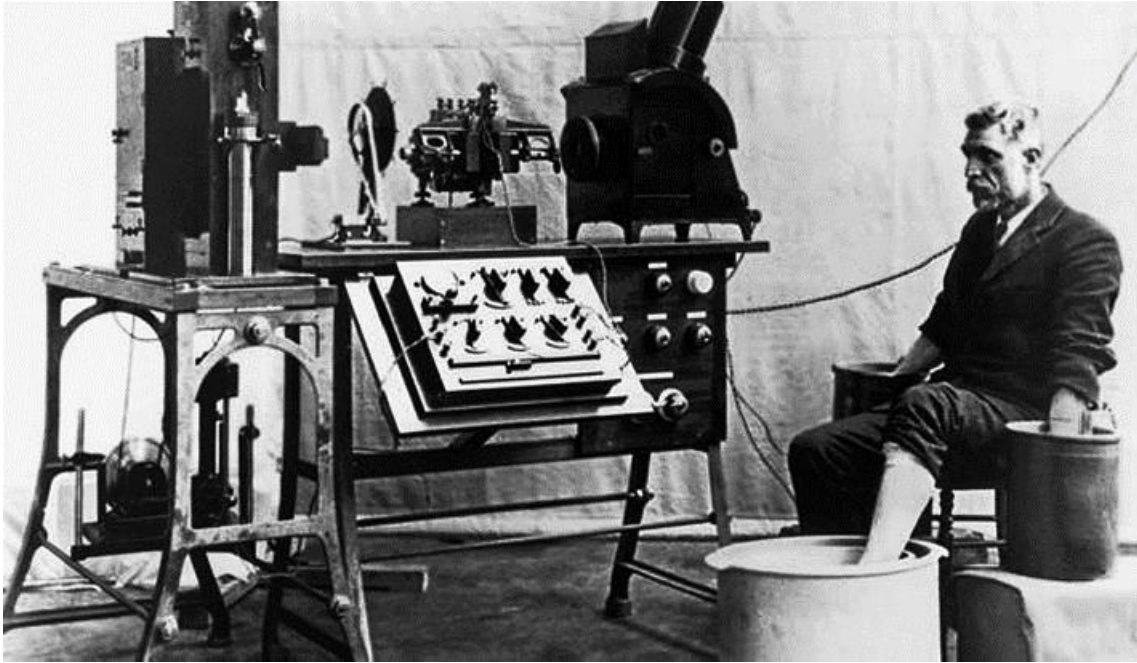


Figure 19: First Einthoven string galvanometer, manufactured by the Cambridge Scientific Instrument Company of London. Supplied by E. A. Schäfer at Edinburgh in 1908 (image courtesy of Cambridge Scientific Company of London) [77, 80]

The First Electrocardiograms

After Julius Bernstein introduced the Differential Rheotome, which was the first device used to record an electrocardiogram, many scientists used this device to better understand the electrical activity of the heart. Marchand, in 1877, recorded the time course of the potential variations from the frog's heart, by means of the differential rheotome. He presented his data in tables, which indicated the intensity of the electric current, at various intervals during the cardiac cycle. Engelmann, in 1878, was the first to graphically represent the time course of the potential variations from the heart (electrocardiogram). The curves published by Engelmann clearly shown the diphasic nature of the action potentials recorded from the heart. Soon thereafter, Burdon-Sanderson, used the differential rheotome, to record the potential variations from the tortoise's heart (figure 7) [77].

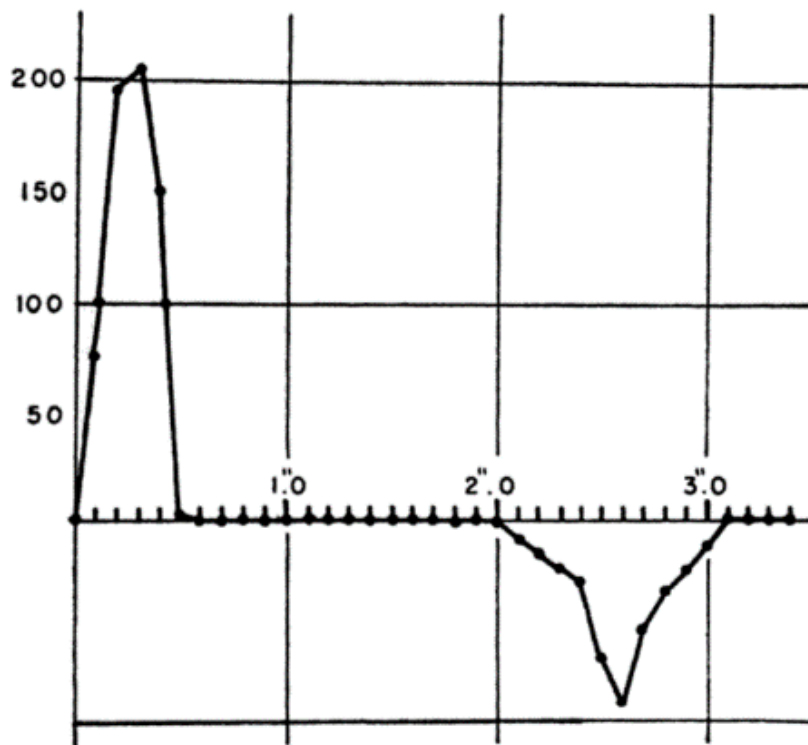


Figure 20: Potential variations over time, recorded by Burdon-Sanderson, from the Tortoise's heart, in 1878. This graphical representation shows similarities with electrocardiograms recorded with modern instruments [77]

The curves published by Burdon-Sanderson show remarkable similarity to electrocardiograms obtained with modern galvanometers. It was from these curves that Burdon-Sanderson first described the details of the repolarization wave of the ventricle (T wave) [77].

The T wave was first detected by Kölliker and Müller, in 1856, when they observed that the negative variation from the heart in contact with the “rheoscopic frog”, was occasionally followed by a minute twitch, which they called the “positive variation” [77].

In 1876 Marey devised a method by which the potential variations recorded by the capillary electrometer could be photographed. Thus, by 1876 a sensitive instrument was available by means of which permanent and direct records of bioelectrical phenomena could be obtained [77]. However, despite its great sensitivity, the capillary electrometer lacked in speed, its movements were very slow indeed, due to this fact, Willem Einthoven of Leiden, started searching for a faster galvanometer. Despite this problem this device was very useful for studying the electrical activity of the heart [adapted from 77].

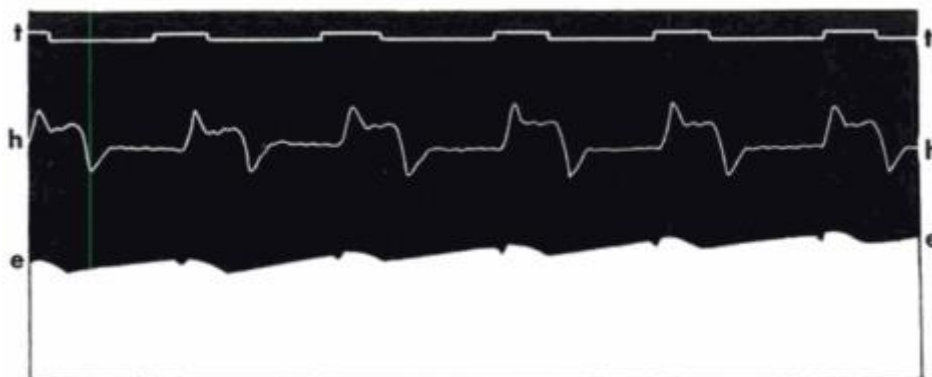


Figure 21: The first electrocardiogram recorded from a human being was obtained with the capillary electrometer in 1887. The electrocardiogram is the lower part of the illustration. The curve labeled t is the time basis in 0.05 second intervals, h is the cardiophone tracing, and e is the electrometer recording (from Waller, A. D.: *J. Physiol.* 8:229, 1887, *An Introduction to Human Physiology* [3rd.; London: Longmans, Green & Co., 1896].) [77]

Augustus Désiré Waller, physiologist of London, discovered that the electrical activity of the human heart could be recorded by means of the capillary electrometer without opening the chest and exposing the heart. Before him, Marey, Burdon-Sanderson and Page, Gotch, Burch, Engelmann, and others had been recording the electrical activity associated with the beat of the exposed heart of many animals, but none of them had realized that this activity could also be recording for the intact heart from the chest wall over precordium. Waller was the first to record the electrical activity of the human heart (1887). In his initial paper, he called the record an “electrogram” [77]. The following year, in the opening lecture of the 1888-1889 session of St. Mary’s Hospital Medical School in London, he referred to the records obtained with the capillary electrometer, “cardiograms”. It was Einthoven who introduced the term “electrocardiogram” [77].

“The last decade of the 19th century witnessed the rise of a new era in which physicians used technology along with clinical history and physical examination for the diagnosis of heart disease” [80]. Was also in this last decade, that Einthoven began his experiments, in the search of a more satisfactory equipment to study and better understand the electrical activity of the human heart [77].

Willem Einthoven and George J. Burch in the 1890s, developed calibration methods for correcting the records obtained with capillary electrometer, and were able to obtain a waveform that was close to the “real” ECG shape [adapted from 72 and 82] (see figure 9). The denomination which Einthoven attributed to electrocardiographic waveforms, is still in use today [adapted from 72].

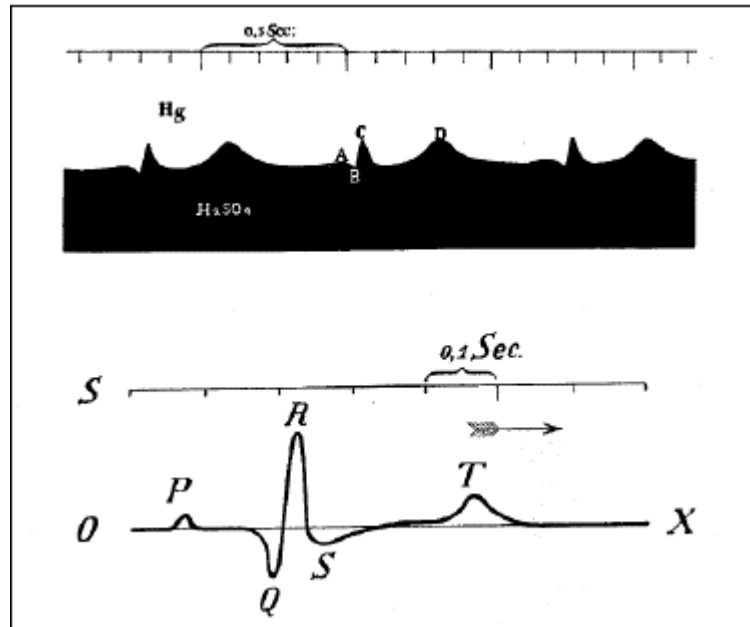


Figure 22: Einthoven's suggested electrocardiographic notation, which resulted from the experiments with the capillary electrometer, it is the same notation used nowadays, the P and T waves, and the QRS complex. The graphic on the lower side was obtained by empiric methods [72]

After working for a number of years with the capillary electrometer and being dissatisfied with the records obtained with this instrument. Willem Einthoven of Leiden University in Holland, began to look for a more satisfactory method for recording the electrical activity of the heart [adapted from 72 and 77].

The very first electrocardiograms recorded, in which the trace resembles the ones that are obtained using modern equipment, were obtained in the XX century. With commercial electrocardiographic equipment, constructed using the same principles as the string galvanometer developed by Willem Einthoven. Two devices were made at first, one by Edelmann and Sons in Munich, Germany, in consultation with Einthoven and the other one was built by the Cambridge Instrument Company of London, and was supplied to the University of Edinburgh, in Holland, in 1908. The electrocardiograms recorded with this latter equipment were superior to the ones recorded with the Edelmann's device (see figure 10) [adapted from 77].

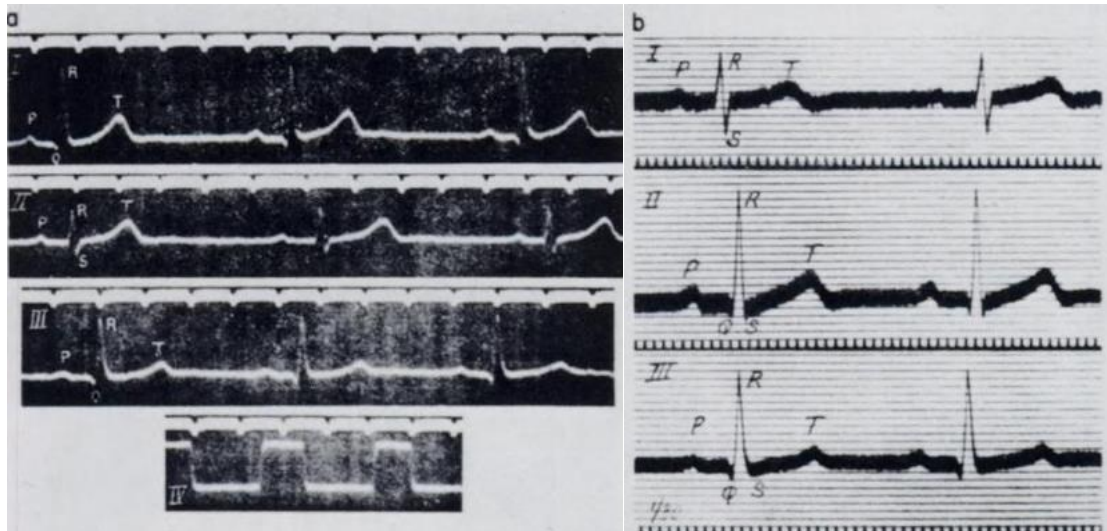


Figure 23: Electrocardiograms obtained by Lewis: in the left, with the letter "a", with the Edlmann's string electrocardiograph. In the right, made with the letter "b", obtained with the Cambridge string electrocardiograph [77]

The Electronic Electrocardiograph

With the vacuum tube invention, the era of electronics started, and opened new horizons, since it could be used, for example, to amplify electrical signals from the heart. Ernestine and Levine, in 1928 wrote a report in the American Health Journal about the use of the vacuum tube, to amplify the electrocardiogram signals, instead of the complex, mechanical amplification devices, like the string galvanometer. In the same year, Frank Sanborn's succeeds in converting a table ECG equipment into the first portable ECG. Soon thereafter, many companies followed, and made their own portable electrocardiographs. At this time, the "portable" equipment, was still being used in conjunction with a mirror galvanometer, like one of the first electronic ECG devices in Europe, that was produced by Siemens, in 1934 (figure 11) [adapted from 72].

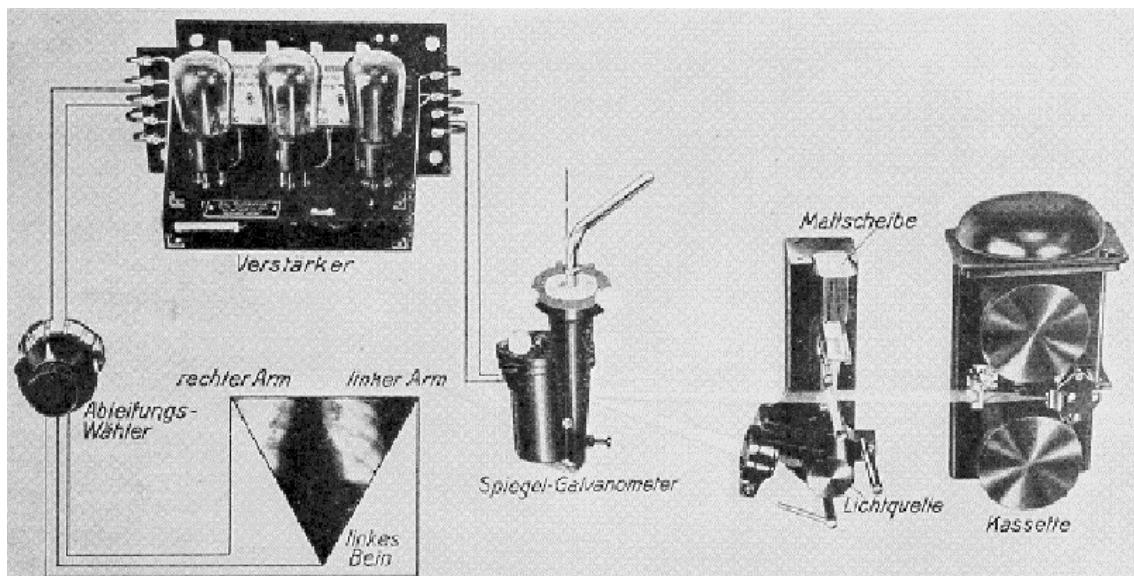


Figure 24: Scheme of electrocardiograph featuring a vacuum-tube amplifier, manufactured by Siemens, in 1934. Right arm, left arm and left leg are connected to a lead selector switch. The signal of the selected channel, was amplified and fed into a mirror galvanometer. The light beam of the mirror galvanometer is projected onto a glass plate and recorded on a film cassette [72, 77]

The next significant step was made with the invention of the cathode ray tube (CRT). The cathode ray oscilloscope opened the doors for the development of equipment, which allowed the ECG waveform to be analyzed in real time, and with much smaller and lighter equipment. Several methods have been developed to record ECG signals on paper, between the 1930s and 1940s, including pen-writing ("direct writing"), and ink-jet. The Cardirex portable ECG equipment, with an ink-jet writing system, was capable of representing signals with frequencies up to 800 Hz, being very successful and helpful in its era [adapted from 72].

With the introduction of computers, laser printers and modern ink-jet systems, the recording of time dependent signals without distortion in paper, ceased to be a problem, replacing all or almost all of the older devices [adapted from 72].

Evolution of the Electrodes

The electrodes play a really important role in the pick-up of bioelectricity, and are a vital component in the electrocardiograph, its design is determinant in the performance of the ECG equipment. The first electrodes were the pan electrodes, that consisted of containers filled with an electrolyte solution, with immerse electrodes, in which the patient introduced both hands, and the left foot (accordingly to the Einthoven's triangle), to perform a medical examination, the electrocardiogram. Figure 12, depicts the technique used by Waller to pick-up the electromotive forces generated by the human heart [adapted from 72].

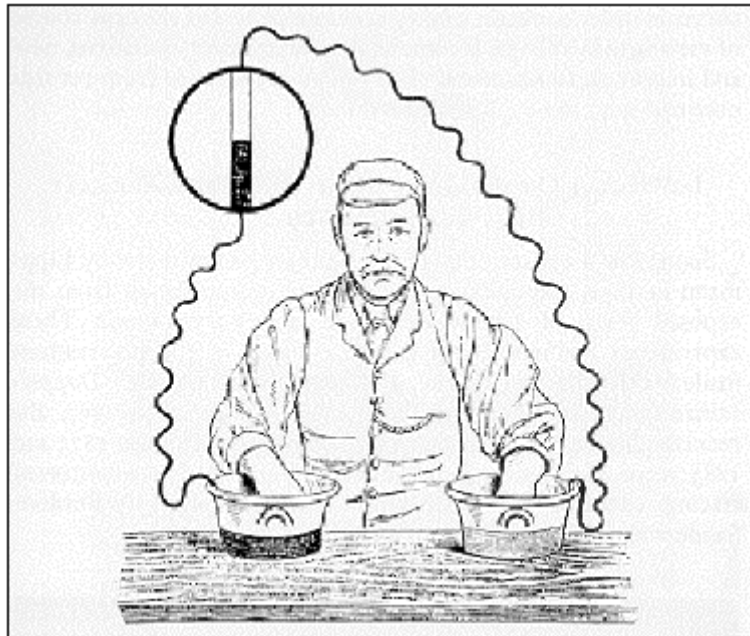


Figure 25: Subject connected to the capillary electrometer by means of pan electrodes [72]

There is a basic difference in generation and representation of electrical signals in biological tissue and metallic conductors. In biological tissue, electrical fields are generated by biochemical processes, in which ions are separated, concentrated, and moved on account of thermodynamic forces, concentration gradients, or impressed electrical potential gradients [72].

The problem in making electrical measurements from biological tissue, is therefore that potential differences to be measured reside in an electrolyte medium, while the measurement instruments are connected by metallic wires featuring electron conduction [72, 83]. The electrode-electrolyte interface is depicted in figure 13.

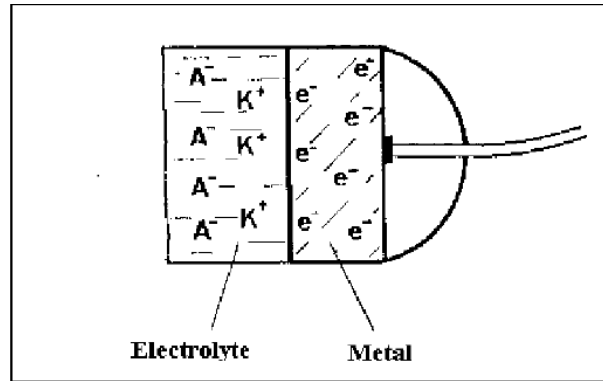


Figure 26: At skin electrode interface, a transformation of electric conductivity, has to take place. In electrolytes, anions A^- and K^+ , represent the current, in electrical equipment, the electrons, are the charge carriers, which represent the electric current. Metal electrode and electrolyte, form an electric half-cell, with conductivity transformation and galvanic potentials [72]

The transformation of electron conductivity into ion conductivity, takes places by chemical reduction and oxidation reactions. Electrical measurements are taken as potential differences between two electrodes. Each measurement process includes two metal-electrolyte-skin interfaces, developing electromotive forces of their own, which interfere with the quantity to be measured [72].

To better understand the behavior of the electrolytes and the skin-electrode interface, extensive research was necessary. After this research, it was possible to design and optimize electrodes for low-noise, high fidelity acquisition of bioelectric signals [adapted from 72]. A complete model of the skin-electrode interface and related problems, has been published [72, 84]. The skin-electrode interface acts as a (non-linear) high-pass filter, due to the ohmic resistance, capacitances and voltage dependent voltage sources [adapted from 72].

Advancements in electrode design, and the introduction of high input impedance amplifiers, like, for example, the instrumentation amplifier (figure 14), contributed significantly to the acquisition of low distortion, and low-noise electrocardiograms.

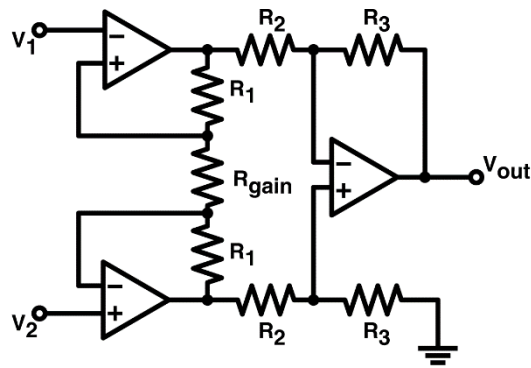


Figure 27: The Instrumentation Amplifier, which contributed for higher quality, low noise electrocardiograms, it features high input impedance and high common-mode rejection. This amplifier is used in most of the modern ECG amplifiers [4].

Two main types of electrodes are used nowadays, for monitoring and diagnosing purposes, these are shown in figures 15 and 16 [adapted from 72].

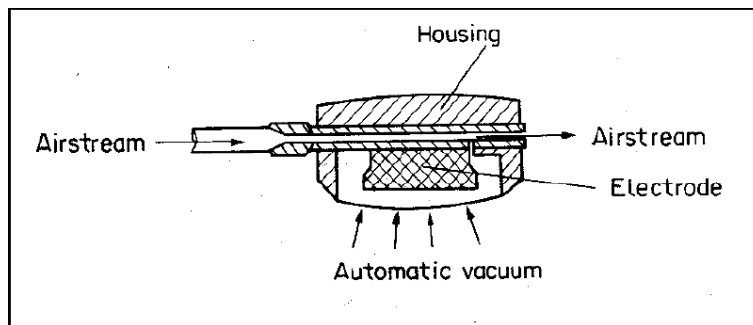


Figure 28: An electrode, primarily used in short-term recordings. The electrode is held in place by vacuum, generated by a small compressor and supplied through the lead cables. The little hole in the air stream tube produces the vacuum (like in Ventury pumps), as long as the stream of air is maintained. There are systems which produce the vacuum by means of a pump [72]

Figure 16 depicts a fluid column (also called the “floating” or the “liquid junction” electrodes) [adapted from 72].

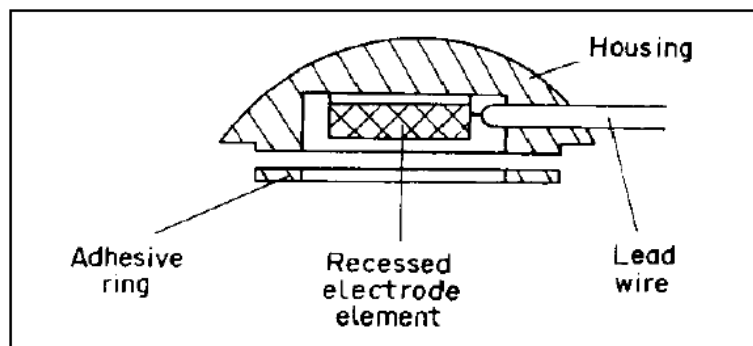


Figure 29: The electrode element (generally made of silver), is recessed, so that it does not come into contact with the skin itself. The cavity is filled with electrode paste or gel, which provides an electrolytic bridge between electrode and skin. In some designs, the distance between the skin and the electrode is maintained, by an open foam disc, placed over the contact area and saturated with electrolyte paste [72]

The Electrocardiogram Nowadays

The first electrocardiographs were large, complex, expensive and heavy equipment, which only a few research institutions had, in the present days there are miniature electrocardiographs, which can be carried in a bag and maybe in the future in the pocket. The new health check-up devices are able to measure the blood percentage of oxygen (oximetry/photoplethysmography), the glucose levels per unit of volume in the blood, and the arterial (blood) pressure, some might also perform other specific examinations.

The introduction of **DSPs (Digital Signal Processors)**, allowed complex filters (which can also be implemented using analog circuits), like notch filters (used to filter the mains frequency) and bandpass filters, to be implemented in a single integrated circuit, the digital filters also have the advantage of reaching a much higher Q factor, allowing the implementation of more “perfect” filters. There is also the possibility to remove or attenuate undesired artifacts, like those caused by tremor or motion.

State of the art electrodes are much smaller and more “comfortable”, they can be incorporated in the chassis of electronic equipment (like, for example, smartphones, tablets and laptops), in steering wheels [1], in handlebars or in clothes.

In the present, circuits are designed to occupy the smallest area possible, as this will allow the development of smaller devices, and with a larger scale of integration, which also contributes to lower production costs. Some integrated circuit manufacturers, developed ASICs (Application Specific Integrated Circuits), featuring a complete 2 lead (with or without reference electrode) ECG front-end, this devices can be used in portable devices, being part of a more complex circuits, like tablet PCs, smartphones, smart watches, PCs, and other similar devices.

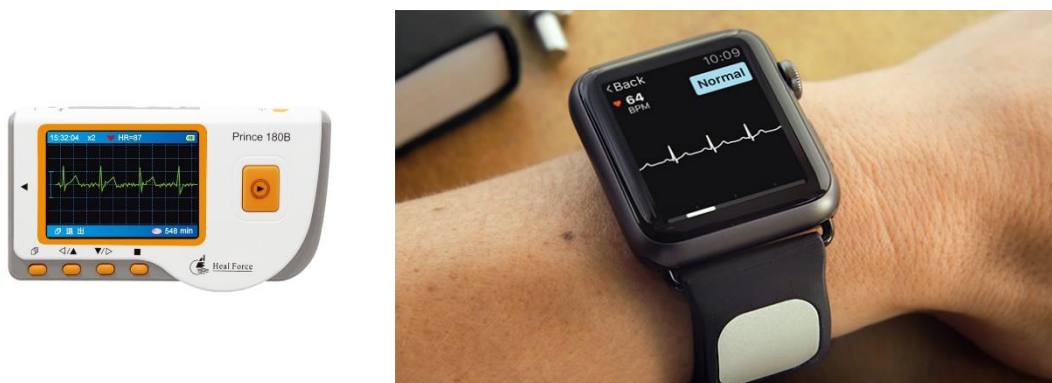


Figure 30: Portable ECG equipment (on the left) [85], ECG being performed on a smart watch (on the right) [86]

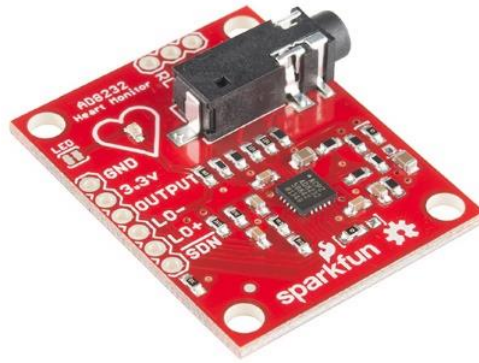


Figure 31: Sparkfun's Heart Rate Monitor, featuring the AD8232 front-end (IC). This board is used for ECG acquisition in conjunction with microcontrollers and/or DSPs, it features an analog output [37]

The new advancements are bringing the before large electrocardiographs that were present only in hospital, or examination centers, to the homes. Maybe someday, these devices will become more common, helping people promptly diagnosing dangerous heart diseases, without visiting the doctor or performing examinations on a center.

Appendix D - State of the Art ECG Test Equipment

ProSim™ 8 Vital Signal and ECG Patient Simulator

There are many manufacturers of test equipment for biomedical instruments, one of the most known is the manufacturer of electronic test equipment, Fluke Corporation. The ProSim™ 8 Vital Signal and ECG Patient Simulator is presented (figures 1 and 2), as an example of electrocardiograph (ECG) test equipment.



Figure 32: The ProSim™ 8 Vital Signal and ECG Patient Simulator from Fluke Corporation (front panel view) [19]



Figure 33: Different views of the ProSim™ 8, from left to right, top view of the equipment and SpO₂ probe, side view of the equipment with SpO₂ probe, the ProSim™ 8 and accessories [19]

Functions of the Equipment

The ProSim™ 8 offers a relatively vast set of functions, the focus of this project is the electrocardiography (ECG), so only the related set of functions are listed, of those some might be summarized, and/or only superficially explained. The functions of the ProSim™ 8 related to ECG equipment testing are as follows [87]:

- ECG waveform generation:
 - 12 lead ECG with independent outputs referenced to the right leg electrode
 - Amplitude level adjustable from 0.05 mV a 5.0 mV (from baseline to R wave peak at the reference lead (II))
 - Adjustable ECG rate from 10 BPM to 360 BPM (adjustable in 1 BPM steps)
 - Adult and pediatric QRS complex duration adjustment (80 or 40 ms)
 - ST segment elevation level adjustment from -.0.8 mV to 0.8 mV
 - Pacemaker waveform generation
 - Arrhythmia simulation
 - Fetal and maternal ECG generation
- ECG performance tests:
 - Adjustable amplitude of the test signals, from 0.05 mV to 5.0 mV
 - Pulse wave generation with a rate of 30 BPM, 60 BPM, with 60 ms pulse width
 - Square wave generation with a frequency of 0.125 Hz, 2.0 Hz or 2.5 Hz
 - Triangle wave generation with a frequency of 0.125 Hz, 2.0 Hz or 2.5 Hz
 - Sine wave generation with a frequency of 0.05 Hz, 0.5 Hz, 1 Hz, 2 Hz, 5 Hz, 10 Hz, 25 Hz, 30 Hz, 40 Hz, 50 Hz, 60 Hz, 100 Hz and 150 Hz
 - R-wave detection test
 - QRS detection test
 - Tall T-wave rejection test
 - ECG artifacts and interference:
 - 50/60 Hz interference
 - EMG
 - Baseline wander
 - Respiration

RIGEL Medical PatSim200

Another important company, manufacturer of medical test equipment, is the Seaward Group. And one of the most remarkable testing instruments for medical applications (more specifically, featuring ECG equipment testing functions), is produced by this company, the RIGEL Medical PatSim200. This device is presented in figures 3, 4 and 5.



Figure 34: Front view of the RIGEL medical PatSim200 [88]



Figure 35: Side view of the RIGEL PatSim200, showing the ECG output jacks[88]



Figure 36: Front view of the RIGEL medical PatSim200, in this picture the device appears to be testing an ECG monitor, generating a normal ECG waveform [89]

Functions of the Equipment

As is typical in medical testing equipment, the RIGEL PatSim200 possesses a relatively vast set of testing options and functions, some are not related to ECG testing, and since the focus of this project is ECG testing equipment, those unrelated functions are not mentioned in the list. Since this equipment has a vast set of ECG testing functions, some might be summarized, and/or superficially explained. The ECG testing functions of the RIGEL PatSim200 are presented in the following list [90]:

- ECG waveform generation:
 - 12 lead ECG with independent outputs for each signal lead
 - 18 heart rate selectable values between 30 and 300 BPM
 - Adjustable ECG amplitude (relative to reference lead II) between 0.05 mV and 5.5 mV
 - ST segment elevation and depression with 18 selectable values (8 elevated and 8 depressed)
 - Neonatal ECG Mode (QRS complex width is reduced to 40 ms)
 - Arrhythmia simulation
 - Pacer waveform generation
- ECG performance tests:
 - Square wave generation with frequencies of 2 Hz or 0.125 Hz
 - Triangle wave generation with a frequency of 2 Hz
 - Generation of pulses at a rate of 60 to 240 BPM
 - Sine wave generation with frequencies of 0.05, 0.5, 1, 10, 25, 30, 40, 50, 60 and 100 Hz
 - R-wave detection test (QRS detection), havers-triangle wave at rates from 30 to 250 BPM (6 selectable values), with selectable amplitude (from 0.05 mV to 0.5 mV, adjustable in 0.05 mV steps) and width (12 selectable values between 8 and 200 ms)
 - Amplitude adjustment of the performance testing signals from 0.5 to 50 mV in 0.5 mV steps

MedTec-Science GmbH MS410 ECG Simulator

MedTec manufactures the MS410 ECG Simulator, a “low-cost”, high quality, certified, ECG test equipment. This equipment has many features found on more expensive devices. It is an ECG performance oriented device, lacking the features to test other types of medical instrumentation. The device is shown on pictures 6 and 7.



Figure 37: Front view of the MedTec MS410 ECG Simulator [91]



Figure 38: Back view of the MedTec MS410, showing the signal output jacks [91]

Functions of the Equipment

The MS410 ECG Simulator possess only ECG equipment testing functions, however, some functions might be less relevant in the scope of this project, and may be summarized and/or only superficially exposed. The following list contains the main features of the MS410 [91]:

- ECG waveform generation:
 - 8 heart rate configurations (30, 45, 60, 75, 90, 120, 150 or 180 BPM)
 - Arrhythmia simulation
 - Pacemaker waveform generation
 - ST elevation and depression
- ECG performance tests:
 - 1 mV Calibration signal generation
 - 50/60 Hz interference generation
 - Baseline variation
 - Electrode malfunction
 - Spikes
 - High frequency interference

Netech MiniSim 1000 Advanced Patient Simulator

The Netech MiniSim 1000 is a high quality patient simulator, with functions to test ECG, blood-pressure, respiration and temperature monitoring equipment. It is manufactured by Netech Corporation, a company specialized in the development and manufacturing of biomedical and industrial test equipment. The equipment is shown in figure 8.



Figure 39: The Netech MiniSim 1000 Patient Simulator [92]

Functions of the Equipment

Like other patient simulators, the Netech MiniSim 1000 has an extensive list of medical equipment performance tests. Some functions, though very important, are not very relevant to this project, which focuses on ECG testing equipment. Given the fact that there are ECG testing functions in this equipment that might be less relevant in the project scope, some functions might be superficially covered, omitted or summarized. The equipment has the following ECG test features [93]:

- ECG waveform generation:
 - 12 lead ECG with independent outputs referenced to the right leg electrode
 - 14 selectable heart rates (30, 60, 70, 80, 90, 100, 120, 150, 180, 210, 240, 270, 300 and 350 BPM)
 - Adjustable ECG amplitude* from 0.15 to 5 mV
 - Pacemaker waveform generation
 - Arrhythmia simulation
 - ST segment elevation and depression
- ECG performance tests:
 - Sine, triangle and square wave generation with frequencies between 0.1 and 100 Hz
 - Adjustable test wave amplitude* (0.1, 0.2, 0.5, 1.0, 2.0, 3.0, 4.0, 5.0 mV)
 - Pulse generation (20 ms pulse width, 1 mV amplitude*, repeated in 4 second intervals)
 - R-wave detection (adjustable width from 10 to 120 ms, amplitude* adjustment from 0.15 to 5.0 mV)
 - Tall T-wave test

* all amplitudes referenced to lead II

WhaleTeq Single Channel ECG Test System (SECG 4.0)

A different variety of ECG test equipment is the SECG 4.0, produced by WhaleTeq, a computer controlled and powered ECG test system, with arbitrary waveform generation capabilities. The equipment is presented in figure 9.



Figure 40: Top view of the SECG 4.0 Single Channel ECG Test System [94]

Functions of the Equipment

Contrary to other ECG test equipment, the SECG 4.0 does not generate ECG signals using samples present in an internal read-only memory, instead this device generates waves from samples generated by a computer. A summary of the set of tests that may be performed by this device (using the software provide by WhaleTeq) is presented in the following list [95]:

- ECG performance tests:
 - Sine wave generation (with adjustable amplitude and frequency)
 - Triangle wave generation (with adjustable amplitude and frequency)
 - Square wave generation (with adjustable amplitude and frequency)
 - Rectangular pulse generation (with adjustable amplitude, pulse width and frequency)
 - Triangular pulse generation (with adjustable amplitude, pulse width and frequency)
 - Exponential waveform generation (with adjustable amplitude, pulse width and frequency)
 - ECG waveform generation (adjustable amplitude, heart rate, QRS complex duration and T wave amplitude)
 - ECG performance waveforms generation (defined by ANSI/AAMI, from IEC 60601, fixed amplitude)
 - DC offset adjustment
 - Input impedance test (places a 620k Ω resistor in parallel with a 4.7 nF capacitor in series with the main function)
 - Output lead electrode selection (more than one lead electrode may be selected, unselected outputs are connected to ground)
 - Pacemaker waveform generation
 - Baseline reset test
 - Mains noise generation (50 or 60 Hz, adjustable amplitude from 0.05 to 0.2 mVpp)
 - AAMI EC 13 Drift Test (to perform baseline drift tests)
 - Dynamic range test
 - Frequency scan
 - Slow heart rate ECG (generates heart rates between 3 and 30 BPM)

Appendix E - Microcontroller Code

The microcontroller code is very extensive to be presented in an appendix of this report, so it is stored in a folder named “Code”, the code filename plus extension is “Code.ino”. The file opens with Arduino IDE open source software, which can be found in the following link:

<https://www.arduino.cc/en/Main/Software>

References

- [1] <https://www.cardio-id.com/cardiowheel>
- [2] Thakor, Nitish V., “Biopotentials and Electrophysiology Measurement”, CRC Press LLC, 1999
- [3] metrology.tkk.fi/courses/S-108.4010/2006/Biopotentials.ppt
- [4] <https://www.allaboutcircuits.com/technical-articles/practical-uses-of-instrumentation-amplifiers/>
- [5] Instrumentation Amplifier With Precision Voltage Reference, SBOS060 (INA125), Burr-Brown (Texas Instruments), 2009
- [6] Single and Dual Supply, Rail-to-Rail, Low Cost Instrumentation Amplifier; AD623 Data Sheet; Analog Devices, Inc; 2018
- [7] <http://www.kevinboone.net/electricity.html>
- [8] https://e2e.ti.com/cfs-file/__key/communityserver-discussions-components-files/73/5482.Capture.PNG
- [9] J. G. Webster, “Reducing Motion Artifacts and Interference in Biopotential Recording”, IEEE Trans. Biomed. Eng., 31, 823-826, 1984
- [10] J.C. Huhta and J. G. Webster, “60 Hz interference in electrocardiography”, IEEE Trans. Biomed. Eng., 20, 91-101, 1973
- [11] James Karki; “Analysis of the Sallen-Key Architecture”, SLOA024B Application Report, 1999, Rev. 2002
- [12] Jim Karki; “Active Low-Pass Filter Design”, SLOA049B Application Report, 2002
- [13] LB-5 High Q Notch Filter, SNOA680 (LB-5), National Semiconductor (Texas Instruments), 1969, Rev. 2011
- [14] N. V. Thakor, “Electrocardiographic monitors”, Encyclopedia of Medical Devices and Instrumentation, Webster J. G., Ed., New York: Wiley, pp. 1002-1017, 1988
- [15] J. H. Nagle, “Biopotential amplifiers”, in The Biomedical Engineering Handbook, Bronzino J. D., Ed., Boca Raton, FL: CRC Press, pp. 1185-1195, 1995
- [16] J. G. Webster, Ed., “Medical Instrumentation: Application and Design”, 3rd ed., New York: Wiley, 1998
- [17] M. R. Neuman, “Biopotential amplifiers”, in Medical Instrumentation: Application and Design, Webster J. G., Ed., 3rd ed., New York: Wiley, 1998
- [18] P. Horowitz and W. Hill, “The Art of Electronics”, 2nd ed., Cambridge, England: Cambridge University Press, 1989
- [19] <https://www.flukebiomedical.com/products/biomedical-test-equipment/patient-monitor-simulators/prosim-8-vital-signs-patient-simulator>
- [20] OPAx350 High-Speed, Single-Supply, Rail-to-Rail Operational Amplifiers MicroAmplifier Series, SBOS099D (OPA350, OPA2350, OPA4350), Texas Instruments Incorporated, 2018
- [21] <https://store.arduino.cc/arduino-due>
- [22] <https://www.indiamart.com/proddetail/arduino-due-r3-19489840373.html>

- [23] <https://www.arduino.cc/en/Guide/ArduinoDue>
- [24] <https://www.instructables.com/id/Micro-SD-Card-Tutorial/>
- [25] <https://www.geeker.co.nz/accessories/catalex-micro-sd-tf-card-module.html>
- [26] <https://forum.arduino.cc/index.php?topic=360325.0>
- [27] 1.2 V to 37 V adjustable voltage regulators, LM217, LM317 datasheet, STMicroelectronics, 2018
- [28] ADS8339 16-Bit, 250-kSPS, Serial Interface, Micro-Power, Miniature, SAR Analog-to-Digital Converter; SBAS677A (ADS8339), Texas Instruments Incorporated, 2018
- [29] 16-Bit, Dual Channel, Ultra-Low Glitch, Voltage Output, Digital-to-Analog Converter; SLAS430A (DAC8552), Texas Instruments Incorporated, 2018
- [30] THS452x Very Low Power, Negative Rail Input, Rail-To-Rail Output, Fully Differential Amplifier, SBOS458H (THS4521, THS4522, THS4524), Texas Instruments Incorporated, 2018
- [31] James Karki, Fully-Differential Amplifiers Application Report, SLOA054E, Texas Instruments Incorporated, 2002, Rev. 2016
- [32] Operational Amplifier stability compensation methods for capacitive loading applied to TS507, AN2653 Application Note, STMicroelectronics, 2007
- [33] Quad Bilateral Switch for Transmission or Multiplexing of Analog or Digital Signals, HCF4066B, STMicroelectronics, 2001
- [34] ADS8339 16-Bit, 250-kSPS, Serial Interface, Micro-Power, Miniature, SAR Analog-to-Digital Converter; SBAS677A (ADS8339), Texas Instruments Incorporated, 2018
- [35] Karthik Soundarapandian, Mark Berarducci; “Analog Front-End Design for ECG Systems Using Delta-Sigma ADCs”, SBAA160A Application Report, 2009, Rev. 2010
- [36] Single-Lead, Heart Rate Monitor Front End; AD8232 Data Sheet; Analog Devices, Inc; 2018
- [37] <https://learn.sparkfun.com/tutorials/ad8232-heart-rate-monitor-hookup-guide>
- [38] Low-Power, 2-channel, 24-Bit Analog Front-End for Biopotential Measurements, SBAS502B (ADS1291, ADS1292, ADS1292R), Texas Instruments Incorporated, 2018
- [39] Ultra-Low Power, Single-Channel Integrated Biopotential (ECG, R-to-R Detection AFE, MAX30003, Maxim Integrated Products, Inc.; Rev.1, 2016
- [40] Swanson D. K., Webster J. G.; A model for skin-electrode impedance, Biomedical Electrode Technology - Theory and Practice, pp. 117-128, Academic Press, 1974
- [41] B. Taji, S. Shirmohammadi, V. Groza and I. Batkin, “Impact of Skin-Electrode Interface on Electrocardiogram Measurements Using Conductive Textile Electrodes”, IEEE Transactions on Instrumentation and Measurement, 2013
- [42] C. Assambo, A. Baba, R. Dozio, and M. J. Burke, “Determination of the Parameters of the Skin-Electrode Impedance Model for ECG Measurement”, Department of Electronic and Electrical Engineering Trinity College Dublin, Proceedings of the 6th WSEAS Int. Conf. on Electronics, Hardware, Wireless and Optical Communications, Corfu Island, Greece, 2007
- [43] A. Baba and M. J. Burke, “Measurement of the electrical properties of ungelled ECG electrodes”, International Journal of Biology and Biomedical Engineering, Issue 3, Volume 2, 2008

- [44] Yu Mike Chi, Tzyy-Ping Jung and Gert Cauwenberghs, "Dry-Contact and Noncontact Biopotential Electrodes: Methodological Review, IEEE Reviews in Biomedical Engineering, Vol. 3, pp. 106-119, 2010
- [45] J. Costa, D. Almeida, "Circuit to Reproduce an Electronically Tunable Capacitor", paper in preparation
- [46] 100 MHz Current Feedback Amplifier with DC Gain Control, LT1228, Linear Technology Corporation, 2012
- [47] DAC121C081 and DAC121C085 12-Bit Micro Power Digital-to-Analog Converter With an I²C-Compatible Interface, SNAS395F (DAC121C081, DAC121C085), Texas Instruments Incorporated, 2018
- [48] I²C-Compatible, 256-Position Digital Potentiometers; AD5241/AD5242 Data Sheet; Analog Devices, Inc; 2015
- [49] <https://www.sparkfun.com/products/12650>
- [50] <https://www.arduino.cc/en/Reference/SPI>
- [51] <https://www.corelis.com/education/tutorials/spi-tutorial/>
- [52] <http://forum.arduino.cc/index.php?topic=230359.0>
- [53] Karthik Hemmanur, "Inter-Integrated Circuit (I2C)", ECE 480- Design Team 3, 2009
- [54] <https://nettigo.eu/products/micro-sd-card-reader-module>
- [55] <http://soundfile.sapp.org/doc/WaveFormat/>
- [56] SMART ARM-based MCU, SAM3X / SAM3A Series Datasheet, Atmel Corporation, 2015
- [57] <http://www.robgray.com/temp/Due-pinout-A4.png>
- [58] Michael Tian, V. Visvanathan, Jeffrey Hantgan, and Kenneth Kundert, "Striving for Small-Signal Stability", IEEE Circuits and Devices Magazine, vol. 17, no. 1, pp. 31-41, January 2001
- [59] <https://electronics.stackexchange.com/questions/132145/supercapacitors-vs-high-voltage-capacitors-with-inductive-loads-used-in-coilgun>
- [60] Keysight 34405A 5 ½ Digit Multimeter, User's and Service Guide, Keysight Technologies, ed. 13, 2014
- [61] Model SR715 Model 720 LCR Meters, User's Manual, Stanford Research Systems Incorporated, rev. 1.6, 2006
- [62] metrology.tkk.fi/courses/S-108.4010/2006/Biopotentials.ppt
- [63] <https://www.egr.msu.edu/classes/ece445/mason/Files/6-Biopotentials.pdf>
- [64] Malmivuo, Jaakko & Plonsey, Robert. (1995). "Bioelectromagnetism. "3. Subthreshold Membrane Phenomena". 44-65
- [65] <https://www.moleculardevices.com/applications/patch-clamp-electrophysiology/what-action-potential>
- [66] "Basic ECG Interpretation Learning Package", Bendigo Health, 2009
- [67] Lippincott Williams & Wilkins, "ECG Interpretation Made Incredibly Easy!", 5th ed., Wolters Kluwer Health, 2011
- [68] <http://www.pathophys.org/physiology-of-cardiac-conduction-and-contractility/>

- [69] Galvani, A.L., “De viribus electricitatis in motu musculari commentarius”, De Boloniensi Scient. et. art. instituto atque academia commentarii 7, 363, 1791
- [70] Matteucci, C., “Suru n phénomène physiologique produit par les muscles en contraction”, Ann. chim.et phys. 6:339, 1842
- [71] Du-Bois Reymond, “E. Untersuchugen über tierische Elektizität”, Bd. I u. II Berlin, Reimer 1848-60
- [72] Chr. Zywiertz, “A Brief History of Electrocardiography - Progress through Technology”, Biosigna Institute for Biosignal Processing and Systems Research, Hannover, Germany
- [73] Kölliker, A., Müller, H., “Nachweis der negative Schuankung des Muskelstromes am natürlich sich contrahierenden Muskel”, Verh. phys. Med. Ges., 6:528, 1856
- [74] https://www.researchgate.net/figure/Luigi-Galvani-1737-1798_fig5_236197969
- [75] https://www.researchgate.net/figure/Stimulation-experiment-of-Luigi-Galvani-The-electrochemical-behavior-of-two-dissimilar_fig7_321001434
- [76] <https://wellcomecollection.org/works/r5xws5y8?query=galvanometer>
- [77] George Edward Burch, Nicholas P. DePasquale, “A History of Electrocardiography”, Norman Publishing, San Francisco, 1990
- [78] Waller, A. D., “On the electromotive changes connected with the beat of mammalian heart, and of the human heart in particular. Phil Trans R Soc Lond B 1889; 180:169-94
- [79] Einthoven W, Fahr G., De Waart A.: “On the direction and manifest size of the variation of potential in the human heart and on the influence of the position of the heart on the form of an electrocardiogram”. Am Heart J 1950, 40(2):163-211
- [80] Majd AlGhatrif & Joseph Lindsay, “A brief review: history to understand fundamentals of electrocardiography”, Journal of Community Hospital Internal Medicine Perspectives, 2012, 2:1, 14383
- [81] <https://ekg.academy/learn-ekg?courseid=324&seq=6>
- [82] Einthoven, W.: “Über den Einfluß des Leitungswiderstandes auf die Geschwindigkeit der Quecksilberbewegung im Lippmann ‘schen Capillarelectrometer” and “Über die Form des menschlichen Ecg. Pflügers Arch. ges. Physiol. 8:229-34, 1887
- [83] J. H. Nagle, “Biopotential amplifiers”, in The Biomedical Engineering Handbook, Bronzino J. D., Ed., Boca Raton, FL: CRC Press, pp. 1185-1195, 1995
- [84] Gatzke, R. D.: “The electrode: A measurement systems viewpoint”. Miller A. H., Harrison DC, eds. “Biomedical Electrode Technology”. New York: Academic Press, 1974: 99-116
- [85] <http://www.healforce.com/en/index.php?ac=article&at=read&did=457>
- [86] <https://www.medgadget.com/2016/03/kardia-ecg-band-for-apple-watch-unveiled.html>
- [87] Fluke® Biomedical ProSim™ 8 Vital Signs Simulator, Getting Started Manual, PN 3984515, Rev. 3, Fluke Corporation, 2011-2016
- [88] <http://www.rigelmedical.com/userfiles/patsim200-patient-simulator.php?ref=shortlink>
- [89] <https://www.medicalplasticsnews.com/news/new-medical-device-designed-by-teesside-university-lecturer/>
- [90] RIGEL PatSim200 Patient Simulator, Instruction Manual, 404A920 Revision 1.1, RIGEL Medical, Seaward Group, 2016

- [91] MS410 ECG Simulator, Instruction Manual, Version 1.6, MedTec-Science GmbH, 2016
- [92] https://www.netechcorp.us/Products/details/MiniSim-1000-Patient-Simulator_70
- [93] Netech MiniSim 1000 Patient Simulator, Instruction Manual, Netech Corporation, 2003
- [94] <https://www.whaleteq.com/en/Products/Detail/18/SECG%204.0#tag=proOverview>
- [95] Single Channel ECG Test System, User Manual, WhaleTeq Co, LTD, 2017