Transformerless Ultra-High Gain Buck-Boost DC-DC Converter with Single-Switch of Reduced Voltage Stress

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***Abstract*— This paper introduces a new DC-DC power converter topology capable of both step-up and step-down voltage conversion, with an exceptionally high voltage gain ratio.. Besides the high extension of the voltage gain range, the converter is also characterized by the use of a single switch. Moreover, the stress imposed on the switch's voltage is minimized, enabling the utilization of low-voltage, low RDS-ON MOSFETs. Consequently, this modification leads to reduced costs and losses associated with switch conduction and turn ON. Another aspect concerning the proposed converter is that the input current exhibits a continuous behavior, which can be significant for various applications. The paper provides insights into the operational performance, steady-state behavior, and mathematical underpinnings of the proposed dc-dc converter. Comparative evaluation of the static voltage gain of the proposed converter and other topologies with comparable characteristics will also be shown. Verification of the presented converter's key features are conducted through both simulation and experimental assessments using a 440-W laboratory prototype. Through these analyses, the efficacy and viability of the modified coupled-inductor SEPIC converter with enhanced voltage gain capability are confirmed.**

Keywords—DC-DC converter, transformerless, ultra-high gain, Buck-Boost

I. Introduction

There has been a growing requirement for high conversion gain dc-dc power converters across diverse power electronics applications in recent times. This surge in interest can be ascribed to numerous factors. First, the rapid expansion of renewable energy (RE) sources has underscored the necessity for converters designed to achieve high voltage gain ratios. This is particularly relevant due to the typically low-voltage outputs of numerous renewable energy sources, such as fuel cells and photovoltaic modules. In such cases, stepping up the low input voltage to higher levels is essential to ensure the effective operation of grid-forming or grid-feeding converters [1]. On the other hand, a significant aspect is the potential for more efficient distribution of electrical energy at elevated DC voltage levels (for instance, 380–400 V or beyond). This is particularly notable in sectors like electrified aviation, telecommunications and DC power systems, where the transmission of electrical energy can be conducted with improved efficiency, enhanced reliability, and superior power quality [2-9].

Traditionally, Boost and Buck-Boost configurations are utilized to elevate output voltage levelsStill, exceeding conversion rates of four or five becomes impractical due to the existence of parasitic elements [10]. Furthermore, operating at high duty cycles compromises Boost converter efficiency, leading to shorter turn-off times that may increase electrical disturbances and current variations (ripple), necessitating larger magnetic components [11,12]. Another alternative for for high-voltage applications is the utilization of a flyback converter [13]. While this topology is suitable for such applications with a low parts count, it's limited to very low power levels. This limitation stems from the significant DC bias current requirement of its

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flyback transformer, resulting in increased transformer size. As a result, there are higher losses at higher power levels in continuous conduction.

Given this perspective, a substantial body of research has been devoted to the design of high-voltage-gain power converters that circumvent the requirement for exorbitant duty ratios. Generally, achieving the desired performance entails leveraging coupled inductors, switched capacitor cells and switched inductors, along with merged configurations [14-19]. These efforts aim to surmount existing technological constraints, such as power switch breakdown voltage limitations and restricted power ratings, to attain the necessary output voltage level with minimal duty ratios, thereby enhancing efficiency. However, in practical scenarios, acquiring the requisite voltage gain and minimizing voltage stress across the power switch often entails the use of multiple switched cells. Additionally, incorporating an impedance network constitutes an alternative topological configuration in addressing these challenges. In this way, efforts have been directed towards enhancing the conventional based impedance source converter by introducing various modified impedance networks. These adaptations include extended Boost, switched capacitor, switched-inductor, merged configurations, and enhanced Boost configurations [20-25]. While these topologies enable achieving high-voltage gain with small duty-cycles (δ), they are characterized by drawbacks such as high part counts. Particularly noteworthy is the fact that most diodes conduct during ($1-\delta$) of the switching period, resulting in elevated power loss and reduced efficiency. From the methods mentioned earlier, employing coupled inductors emerges as a potent technique for augmenting voltage gain without escalating part counts. This approach has the potential to reduce power losses and enhance efficiency. Thus, several works proposed converters with enhanced voltage gain ratios [26-29]. In general, the introduced topologies based on coupled inductors exhibit two primary limitations. Firstly, the utilization of two magnetic elements and the requirement for additional diodes and capacitor cells to substantially increases the voltage ratio diminish power density. In addition, to counteract the negative impact of coupled-inductor leakage inductance, the inclusion of a snubber circuit becomes necessary [30]. Notwithstanding recent advancements in power converter topologies, the integration of multiple converters into multicell configurations offers a compelling approach to achieve elevated voltage gain ratios. This might be accomplished through implementation of series and/or parallel connections of power converter units, cascaded cell structures, or multilevel topologies [31-33]. Undoubtedly, the multicell connection of power converters effectively addresses the need to fulfill the requisite power rating, voltage gain, and to attenuate voltage stress across the power switches". However, the high component count and potential decrease in efficiency may constrain their performance. Hence, it is advisable to initially optimize performance of the topology itself prior to resorting to multicell connections. Another aspect that most Buck-Boost topologies suffer from is that as their voltage gain increases, the range of the Buck region becomes very small.

Based on the preceding discussions, this paper emphasizes a new power converter topology with Buck-Boost characteristics and ultra-high gain. The topology was also designed to minimize the number of switches, since only requires one. Nevertheless, it uses more passive components when compared to other solutions. The characteristics of the proposed topology are validated by key simulation and experimental results. This paper is organized as followed. Subsequent to this introductory section, Section II will delve into the operating principle and steady-state analysis of the proposed dc-dc converter. Subsequently, Section III will present a comprehensive analysis of simulation results. Section IV will show the results of our experiments and the conclusions in section V.

II. Fundamental Principles of Operation and Steady-State Analysis

The structure of the proposed ultra-high voltage gain Buck-Boost configuration is illustrated in Fig. 1. The structure of this converter consists into a switch, five diodes, four capacitors and three inductors.

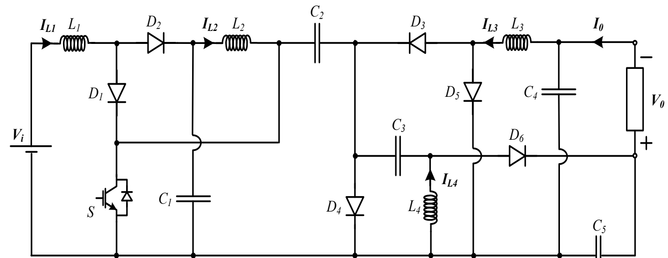

Fig. 1. Proposed power circuit configuration of the transformerless high gain Buck-Boost DC-DC converter.

To conduct an analysis of the converter's operation, various assumptions are considered as outlined below:

- The switch and diodes are considered ideal, meaning that any resistance when the switch and diode is on, was well as the voltage drop across them, is disregarded
- All capacitors that are used are considered sufficiently large, meaning that any voltage ripple experienced by these components is negligible.

Based on these assumptions, each switching cycle is segmented into two operational modes, and hence in continuous conduction mode (CCM), as depicted in Figures 2(a) and (b).

First Mode: In this first segment, switch S and diodes D_1 and D_3 are turned on, while diodes D_2, D_4, D_5, D_6 and D_7 are turned off. As a result of this, the inductors will be charged with the energy that was stored in the capacitors C_1, C_2, C_4 and C_5 and from the input voltage source. From the analysis of the circuits that resulted from the turn-on of the switch, the following equations are deduced:

$$\begin{aligned} &\frac{di_{L1}}{dt} = \frac{V_i}{L_1}; \ \frac{di_{L2}}{dt} = \frac{v_{C1}}{L_2}; \ \frac{di_{L3}}{dt} = \frac{v_{C2} - v_{C4}}{L_3}; \\ &\frac{di_{L4}}{dt} = \frac{v_{C2} - v_{C3}}{L_3}; \frac{dv_{C1}}{dt} = \frac{-i_{L2}}{C_1}; \frac{dv_{C2}}{dt} = \frac{-i_{L3} - i_{L4}}{C_2}; \\ &\frac{dv_{C3}}{dt} = \frac{-i_{L4}}{C_3}; \frac{dv_{C4}}{dt} = \frac{i_{L3} - i_0}{C_4}; \frac{dv_{C5}}{dt} = \frac{-i_0}{C_5} \end{aligned} \quad (1)$$

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<u>Second Mode:</u> In the second segment, switch S and diodes D_1 and D_4 are turned off, while now diodes D_2, D_3, D_5, D_6 and D_7 will change to on. As a result of this, the inductors and capacitor C_3 will be discharged. The other capacitors will be charged. From the analysis of the circuits that resulted from the turn on of the switch, the following equations are deduced:

$$\begin{aligned}&\frac{di_{L1}}{dt}=\frac{V_i-v_{C1}}{L_1};\ \frac{di_{L2}}{dt}=\frac{v_{C1}-v_{C2}}{L_2};\ \frac{di_{L3}}{dt}=\frac{-v_{C4}}{L_3};\\&\frac{di_{L4}}{dt}=\frac{-v_{C3}}{L_3};\frac{dv_{C1}}{dt}=\frac{i_{L1}-i_{L2}}{C_1};\frac{dv_{C2}}{dt}=\frac{i_{L2}}{C_2};\\&\frac{dv_{C3}}{dt}=\frac{-i_{L2}}{C_3};\frac{dv_{C4}}{dt}=\frac{i_{L3}-i_0}{C_4};\frac{dv_{C5}}{dt}=\frac{i_{L2}+i_{L4}}{C_5}\end{aligned}\quad (2)$$

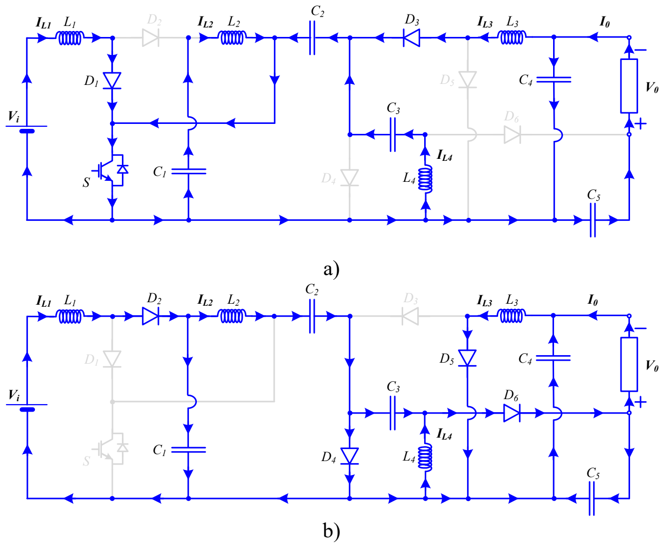

Fig. 2. Equivalent circuits of the proposed transformerless high gain Buck-Boost DC-DC converter that resulted from the two operation modes.

In order to facilitate a simplified steady-state analysis of the proposed converter, the converter is considered as a lossless system, maintaining the relationship $V_i i_i = V_o i_o$, where i_i and i_o represent the input and output currents, respectively. Additionally, let's assume that the voltage ripples across all capacitors are insignificant. Furthermore, losses in the power devices, such as the switch and diodes, are not taken into account. Using these considerations and by applying the volt-second balance principle for the inductors and the principle of ampere-second balance for the capacitors, we can derive the following equations:

$$\begin{cases}\delta V_i+(1-\delta)\left(V_i-V_{C_1}\right)=0\\ \delta V_{C_1}+(1-\delta)\left(V_{C_1}-V_{C_2}\right)=0\\ \delta\left(V_{C_2}-V_{C_4}\right)+(1-\delta)\left(-V_{C_4}\right)=0\\ \delta\left(V_{C_2}-V_{C_3}\right)+(1-\delta)\left(-V_{C_3}\right)=0\\ V_{C_5}=V_{C_3}\\ V_o=V_{C_4}+V_{C_5}\end{cases}\quad (3)$$

Equations (3) allow for the derivation of the ideal output voltage, expressed in relation to the input voltage V_i and the switch duty-cycle δ. In this way, we will have:

$$V_o=\frac{2\delta}{(1-\delta)^2}V_i \quad (4)$$

Based on the last equation and the expression for the ideal voltage conversion ratio of the conventional Buck-Boost converter and quadratic Buck-Boost converter, the correlation between the ideal voltage conversion ratio and the duty-cycle of both the proposed converter and the other traditional Buck-Boost converters is illustrated in Figure 5. It can be observed from Figure 5 that the proposed converter achieves a broader range of voltage gain in comparison with the traditional Buck-Boost converter.

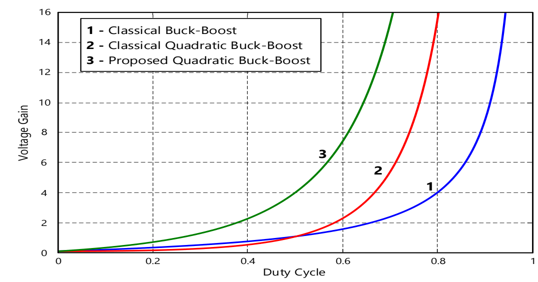

Fig. 3. Evaluation of the suggested converter's optimal voltage conversion ratio in comparison to the conventional Buck-Boost converters.

III. SIMULATION RESULTS

To validate and assess the system's performance, simulations were conducted using the Matlab/Simulink platform. In order to simplify the simulation analysis, it was used the Power System Blockset toolbox which is a cutting-edge design tool for modeling and simulating power systems. The system parameters are outlined in Table I. The system is configured to operate in CCM during simulation, employing a switching frequency of 20 kHz. Two different duty cycles were selected to evaluate the converter's Buck and Boost capabilities.

TABLE I. PARAMETERS OF THE SYSTEM

Parameter	Value
V_i	48 V
$L_1 = L_2 = L_3 = L_4$	10 mH
$C_1 = C_2 = C_3$	100 μF
$C_4 = C_5$	470 μF
R_o (in Boost mode)	2500 Ω
R_o (in Buck mode)	50 Ω
f_{PWM}	20 kHz

At first, the verification of the Boost ability of the converter was tested. In this test, the duty-cycle was set to 0.7. The resulted waveforms are presented in Figs. 4 to 8. The first result allows to confirm the high voltage gain of the converter, since the output voltage presents an increase compared to the input voltage of about 15. The reduced voltage stress at which the switch is subject can also be verified through Fig. 5. This outcome confirms that the voltage stress experienced by the switch is lower than the output voltage. It's worth noting that in conventional Buck-Boost converters, the switch is subjected to voltages equal to the sum of the output and input voltages.

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Another particular aspect that can be confirmed is the fact that the input current of the converter is continuous as shown by Fig. 6. The CCM can be confirmed through the waveforms of the inductors presented in Figs. 7 and 8.

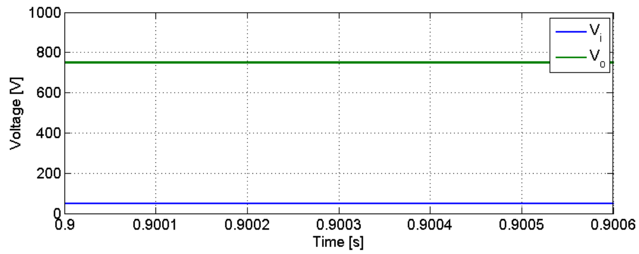

Fig. 5. Results (simulation) of the ultra-high gain step up/down DC-DC converter operating in Boost mode (converter input and output voltages).

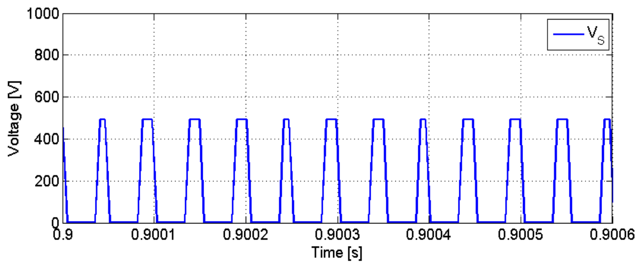

Fig. 6. Results (simulation) of the ultra-high gain step up/down DC-DC converter operating in Boost mode (voltage across the switch).

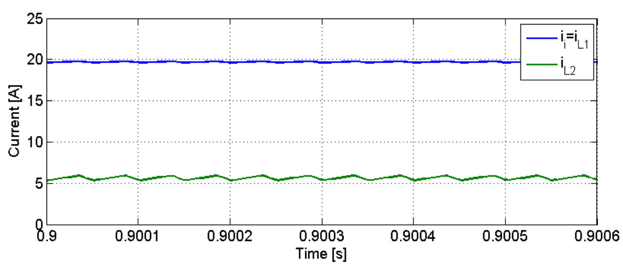

Fig. 7. Results (simulation) of the ultra-high gain step up/down DC-DC converter operating in Boost mode (input and inductors L_1 and L_2 currents).

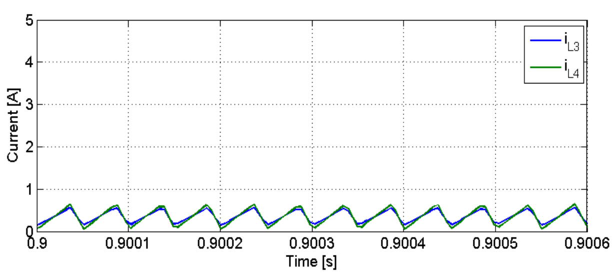

Fig. 8. Results (simulation) of the ultra-high gain step up/down DC-DC converter operating in Boost mode (inductors L_3 and L_4 currents).

With the purpose to verify the Bucking ability of the converter, a test in which the duty-cycle is set to be 0.3 was done. The resulted waveforms are presented in Figs. 9 to 11. The first one presents the input and output voltages of the converter. This result confirms that the generated output voltage is lower than the converter input voltage. The voltage stress applied to the switch is in this case higher than the output voltage as shown in Fig. 10. However, since this aspect only happens in Buck mode, it does not influence the selection of the low voltage stress switch, as it must be chosen for the worst-case scenario, which is the Boost operation. In this way, the requirement of a low voltage stress for the switch is maintained. The converter input current, that can be seen in Fig. 11, still maintain their continuity. Thus, the operation of the circuit does not affect this converter characteristic. Besides that, it is possible to confirm the continuous conduction mode through the waveforms of the inductors presented in this figure.

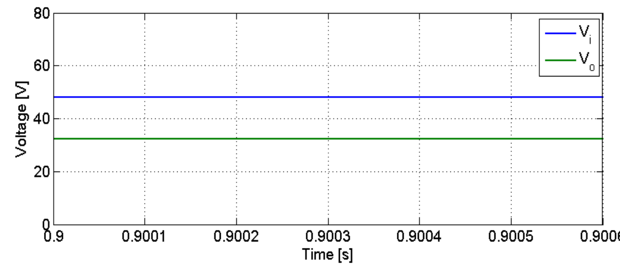

Fig. 9. Results (simulation) of the ultra-high gain step up/down DC-DC converter operating in Buck mode (converter input and output voltages).

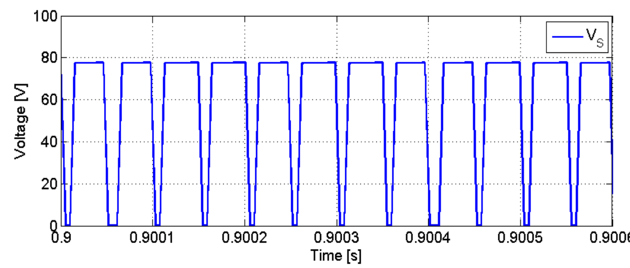

Fig. 10. Results (simulation) of the ultra-high gain step up/down DC-DC converter operating in Buck mode (voltage across the switch).

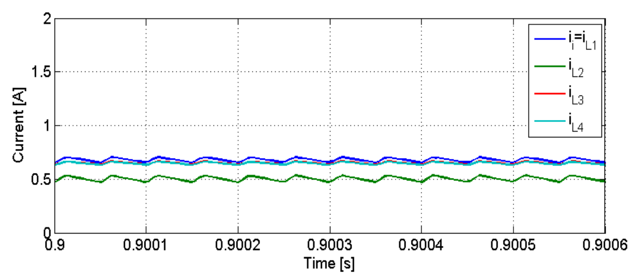

Fig. 11. Results (simulation) of the ultra-high gain step up/down DC-DC converter operating in Buck mode (input and inductors L_1, L_2, L_3 and L_4 currents).

IV. Experimental Results

To confirm the functionality of the proposed design, a hardware prototype was constructed in the lab for testing and validation purposes. For this prototype it was used components with the same parameters as the ones used for simulation purpose. The laboratory tests conducted mirrored those carried out in the simulation. In this way, the testing commenced with the converter operating in Boost mode using a 0.7 duty-cycle. The waveforms from this practical test are depicted in Figs 12 to 16. These results validate those obtained in the simulation. The high voltage gain is confirmed by Fig. 12, while the reduced voltage stress of the switch is verified by Fig. 13. The continuity of the input current is also verified by Fig. 14. Regarding the

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CCM, it can be seen through the inductor currents presented in Figs. 14 and 15.

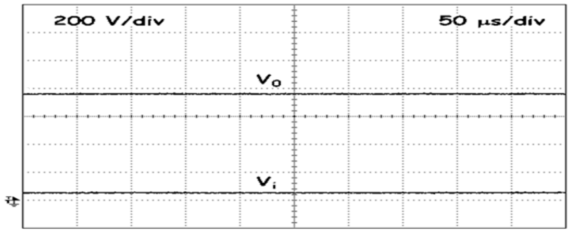

Fig. 12. Results (experimental) of the ultra-high gain step up/down DC-DC converter operating in Boost mode (converter input and output voltages).

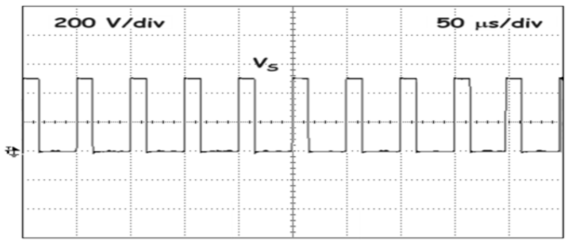

Fig. 13. Results (experimental) of the ultra-high gain step up/down DC-DC converter operating in Boost mode (voltage across the switch).

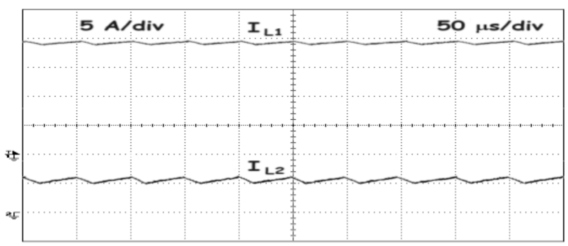

Fig. 14. Results (experimental) of the ultra-high gain step up/down DC-DC converter operating in Boost mode (input and inductors L_1 and L_2 currents).

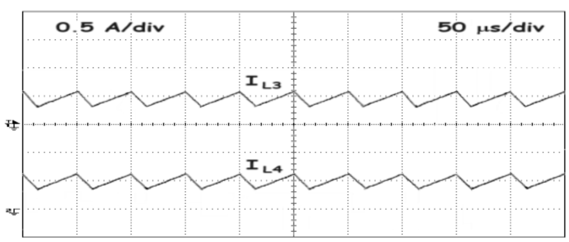

Fig. 15. Results (experimental) of the ultra-high gain step up/down DC-DC converter operating in Boost mode (inductors L_3 and L_4 currents).

The Buck capability of the proposed converter was also tested using the same duty-cycle as in the simulation tests, namely 0.3. The similarity with the simulation results is maintained as shown by Figs. 16 to 18. The first two figures confirm the Buck operation mode and the voltage stress experienced by the switch in this mode. The continuity of the converter input current is once again confirmed by Fig. 18. The efficiency of the proposed topology was also tested using the experimental prototype and a maximum value of 91.4% was achieved. The main advantage of this topology is the ultra-high voltage gain achieved due to higher number of components which becomes a disadvantage regarding the efficiency.

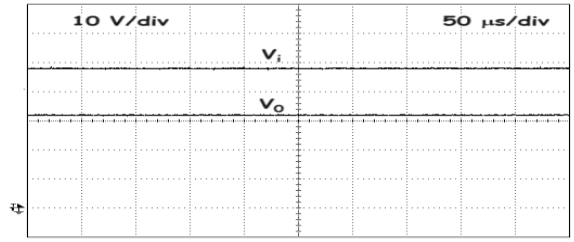

Fig. 16. Results (experimental) of the ultra-high gain step up/down DC-DC converter operating in Buck mode (converter input and output voltages).

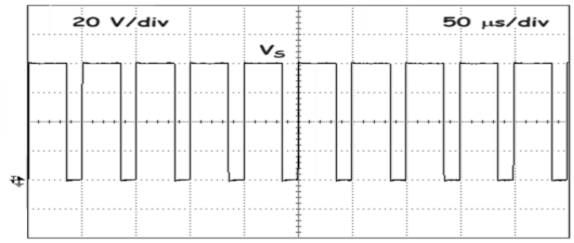

Fig. 17. Results (experimental) of the ultra-high gain step up/down DC-DC converter operating in Boost mode (voltage across the switch).

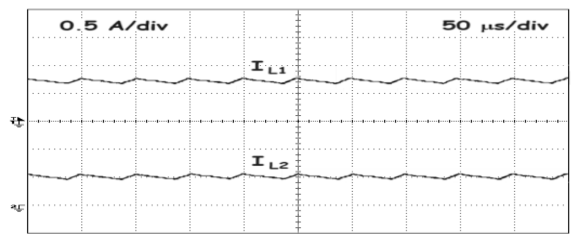

Fig. 18. Results (experimental) of the ultra-high gain step up/down DC-DC converter operating in Boost mode (input and inductors L_1, L_2, L_3 and L_4 currents).

V. Conclusions

This paper introduces a novel transformerless Buck-Boost converter with ultra-high voltage gain. Under the point of view of their configuration, it only requires a single switch. Moreover, the stress imposed on the switch's voltage is minimized. Typically, in a Buck-Boost converter, the voltage stress is the sum of the converter's output voltage and its input voltage. However, in this proposal, the voltage stress is lower than the converter's output voltage. Another particularity that was verified by the tests, is the fact that the converter input current to be continuous. The analysis of the converter's steady state, examined throughout the paper. The paper conducts a comprehensive examination, comparing the voltage gain of the proposed converter with existing topologies outlined in the literature. The results reveal that the proposed converter shows a ultra-voltage gain. The theoretical study was tested by simulation and experimental tests. A diverse range of operating scenarios were considered both in the simulation platform and in the experimental laboratory prototype.

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