Diagnosing Power Transistor Faults in Multilevel T-Type Based Nine Switch Inverter Using Center of Mass Indexes

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***Abstract*— Nine-switch voltage source inverters (NSVSI) are DC-AC converters that utilize a reduced number of switches, making them advantageous for dual or six-phase motors. To enhance the quality of the output voltage and provide fault-tolerant capability, NSVSI topologies, like the T-Type-based NSVSI, have been modified to operate as multilevel converters. However, to ensure fault-tolerant capability, a fault diagnosis algorithm for power transistors must be developed. Therefore, this paper proposes a novel fault detection and diagnosis algorithm to identify faulty transistors in a multilevel T-Type-based NSVSI. This method is based on the development of specific indices derived from the center of mass of the output currents. The proposed technique offers a fast and reliable solution, demonstrating robustness under various load conditions. The effectiveness of this method will be validated through a series of simulation tests.**

Keywords*— Nine-switch inverter; multilevel converters; fault detection and diagnosis; switch fault

I. INTRODUCTION

Over the past few decades, advancements in power converter technology have resulted in a decrease in the number of active and passive components, leading to cost and size reductions. Nine-switch voltage source inverter (NSVSI) is an example of this evolution [1-3]. Because NSVSI topology only provides two voltage levels, it has been adapted to provide multilevel operation (MSVSI). In fact, several topologies based on the NSVSI topology have been proposed, offering improved output voltage quality and reduced harmonic content [4-7]. Another crucial characteristic of the T-Type-based NSVSI is their ruggedness via fault-tolerant capability. This attribute is very important for several industrial applications, as the failure of their power device can led to serious consequences, especially in sensitive areas such as transportation systems, automotive technology, renewable energy systems, electric drives, medical devices and in many other critical equipment [8-10]. Short circuit (SC) and open circuit (OC) are both the most common failures of switching power devices. These components play an important role in power electronic systems, and their failure can lead to significant problems. SC faults may occur due to high temperatures, local thermal runaways, or noise corrupted gate voltage in the switches. OC faults are frequently caused by bond wire fracture, gate drive failure, or solder joint fracture [11]. To achieve fault-tolerant capability it is required to develop a robust fault diagnosis algorithm specifically designed for power transistors. This algorithm must enable the system to detect and respond to faults effectively, ensuring continued emergency operation even under fault conditions [12,13]. Recent works show how fault diagnosis algorithms designed for power transistors improve system reliability by facilitating early fault identification and isolation [14,15]. Moreover, powerful algorithms are essential to guarantee continuity of operation under fault conditions, thereby improving the fault tolerance of the system as a whole [16]. Efficient diagnostic methods, such as real-time monitoring and machine learning techniques, have greatly improved problem identification precision and reduced the impact of transistor failures [14,17]. In this context, several research works and tests have been conducted on open switch faults in electronic power converters, resulting in several fault algorithms proposed for various power converter topologies. In [18] a model-based fault detection and identification (FDI) method to detect and identify faults in components of the power converters. On the other hand, in [19] a fault diagnosis method for three-level NPC inverters based on charge distortion and the currents in the output inverter was presented. A fault detection diagnosis for the T-Type three level inverter based on the voltage pattern is proposed in [20].

As referred, considering the importance of the fault diagnosis, in this work a novel fault detection and diagnosis algorithm specifically designed to identify faulty transistors in a T-Type-based NSVSI, was introduced. The proposed fault detections and diagnosis method is based on the development of specific indexes, derived from the analysis of the center of mass of the output currents in both loads. Using these indexes, the algorithm identifies the faulty transistor, enhancing the reliability and fault-tolerant capability of the multilevel inverter. The proposed fault detection technique provides a rapid and dependable solution, demonstrating robustness for various load conditions. One of the main features of this method is the slight computational effort. To validate its robustness and effectiveness, this method will be validated through a series of simulations tests, under normal and faulty operation conditions. These evaluations will demonstrate its ability to consistently perform in several scenarios of operation.

II. Multilevel T-Type based NSVSI Topology

The T-Type-based NSVSI is one of the several multilevel converter topologies utilized in electrical drives, that has enough degrees of freedom for fault diagnostic and detection methods usage. The T-Type-based NSVSI multilevel topology is characterized by a reduced number of power switches, since the switches in the middle of each arm are shared by the independent dual-output three-phase voltages of the inverter. This type of electrical drive is commonly used in industrial applications requiring independent dual-output three-phase voltages, such as dual motor drives and six-phase induction motor (IM) systems [4, 6].

Fig. 1 shows the simplified power circuit of the T-Type-based NSVSI multilevel topology with two sets of output loads, used to study the power transistor fault diagnosis algorithm.

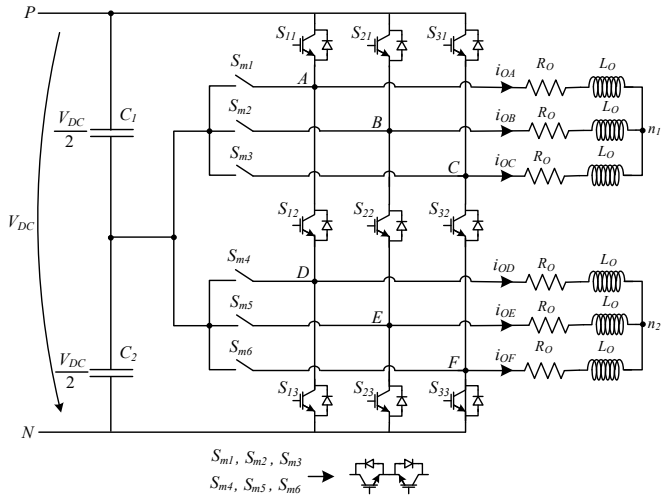


Fig. 1. Multilevel T-Type-based NSVSI, showing the connection to the DC capacitors middle-point.

One of the drawbacks of the traditional T-Type-based NSVSI is that, in the event of a switch failure, fault tolerance for the system is essentially impossible. However, the multilevel T-Type-based NSVSI offers fault tolerance in addition to the capability to apply a lower distortion output under normal operation. To add fault tolerant a fault diagnosis and fault emergency operation are considered in the next sections.

III. A Proposed Algorithm for Fault Detection in Multilevel T-Type Inverter

The fault diagnosis approach relies on the definition of the center of mass indexes that are associated with the pattern of the currents for both loads. To implement this approach for the identification of the faulty patterns, it is necessary to perform the signal acquisition of the load currents through current sensors. A sliding window containing n samples for each current is applied to capture the time behavior of the current patterns. In this way, a generalized current matrix I is considered in accordance with:

$$I = \begin{bmatrix} i_{OA}(t_1) & i_{OB}(t_1) & \cdots & i_{OM}(t_1) \\ i_{OA}(t_2) & i_{OB}(t_2) & \cdots & i_{OM}(t_2) \\ & \cdots & & \\ i_{A}(t_N) & i_{OB}(t_N) & \cdots & i_{OM}(t_N) \end{bmatrix} \quad (1)$$

where $i_{OA}(t_n)$ represents the current of the m-th phase (Fig. 1) at the n-th sampling time, M is the number of phases, and N is the number of sampling points. The sampling period is represented by T_s.

The generalized current matrix can be used to distinguish and detect the distinct current patterns associated with different faulty transistors. In fact, it is possible to define indexes associated to each pattern. In this way, it is defined indexes of average value (IAV_j, IAV_T) that are calculated by the equations (2) and (3).

$$IAV_j = \frac{6\sum_{n=1}^{N} i_{j_n}}{N} \quad (2)$$

$$IAV_T = \frac{\sqrt{\sum_{n=1}^{N}\sum_{j=A}^{M}\left(i_{j_n}\right)^2}}{N}.100 \quad (3)$$

From the previous equations it is possible to obtain the center of mass indexes (SI). Thus, the six SI indexes (A, B, C, D, E and F) are defined, in accordance with (4).

$$SI_j = \frac{IAV_j}{IAV_T}.100 \quad (4)$$

The identification of the faulty switch is determined by the different values that the center of mass indexes (SI) will assume. Hence, if there is a symmetry in the current patterns, all three index values will be equal to zero. In the event of an open switch fault, some or all index values will no longer be zero. For example, in the case of an open-circuit failure in the upper

switch, the diagnostic variables related to the phase of the faulty power device will shift to a negative value, while the other ones will change to positive values. For the other switches, other combinations will appear. In this way, taking into consideration all the transistors that can be subject to a fault in one of the legs, a decision table can be established. Table I displays typical characteristics associated with the various conditions of the phase A switches fault. The presence of two positive and two negative values is one feature that can be seen. The obtained two values roughly represent a ratio of two. Similar tables can be derived for the switches on the remaining legs.

TABLE I. INDEXES ASSOCIATED TO SWITCHES FAULT OF PHASE A

Switch under fault	SI_A	SI_B	SI_C	SI_D	SI_E	SI_F
None	0	0	0	0	0	0
S_{11}	-0.8	0.4	0.4	-1.0	0.5	0.5
S_{12}	1.4	-0.7	-0.7	-1.4	0.7	0.7
S_{13}	1.0	-0.5	-0.5	0.8	-0.4	-0.4
S_{m1}	0.9	-0.4	-0.4	0.0	0.0	0.0
S_{m4}	0.0	0.0	0.0	-0.9	0.4	0.4

Note that table 1 values may vary. In fact, for lighter loads, the current values will be smaller. There are even situations in which there is no impact on one of the load currents (in a situation where previously, with a heavy load, there was an impact). However, the relationship between the values of the indexes maintains their signal and proportionality. There is a relative change in the values, conserving the ratio between values.

IV. NUMERICAL VALIDATION RESULTS

The proposed fault detection approach for NSVSI was validated using a model system built in Matlab/Simulink software using the *SimPowerSystems* library. The Simulink model used includes the semiconductor switching behavior, losses, and all the dynamic behavior of both loads and the multilevel converter. The parameters used in simulation tests are shown in Table II.

TABLE II. PARAMETERS OF THE SYSTEM

Input DC voltage	200 V
Capacitors C_1 and C_2	470 µF
Load resistor per phase	0.1 Ω
Load inductor per phase	5 mH

The control method applied to the NSVSI is based on the Sinusoidal Pulse Width Modulation (SPWM), with sampling time 5.0 kHz. The proposed fault detection method was evaluated using several simulation tests, which included normal operation and an open power switch fault. Initially, the multilevel converter is operating under normal conditions, and suddenly, at t=0.6s, an open switch fault in transistor S_{11} occurs. Fig. 2a) shows the results of the currents in the two loads of the T-Type-based NSVSI, in normal conditions, and after an open switch fault in transistor S_{11} occurs. As shown in Fig. 2b), when there is a switch fault, the center of mass indexes will no longer be zero. The changes of the center of mass indexes values are in accordance with the values presented in Table I.

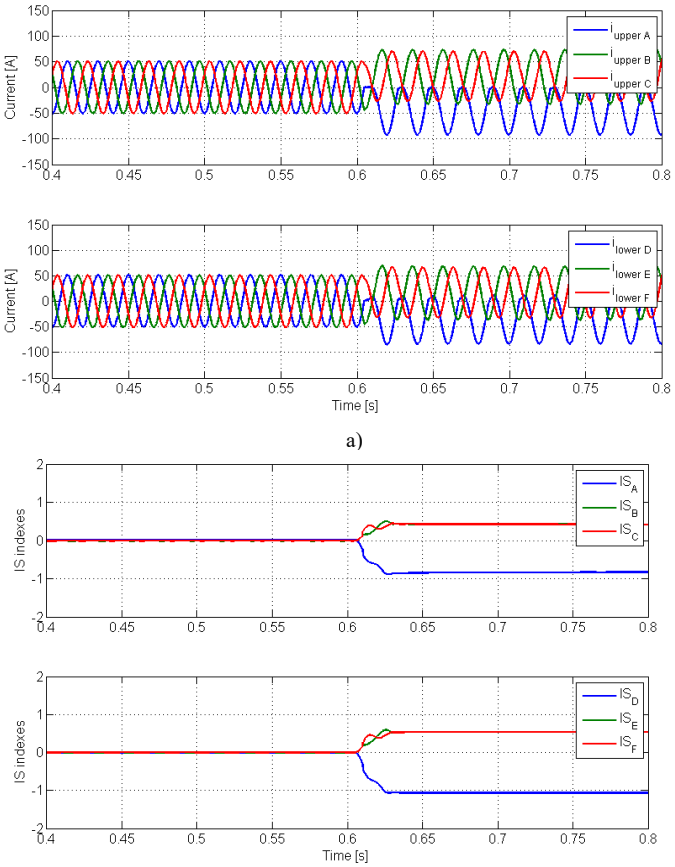
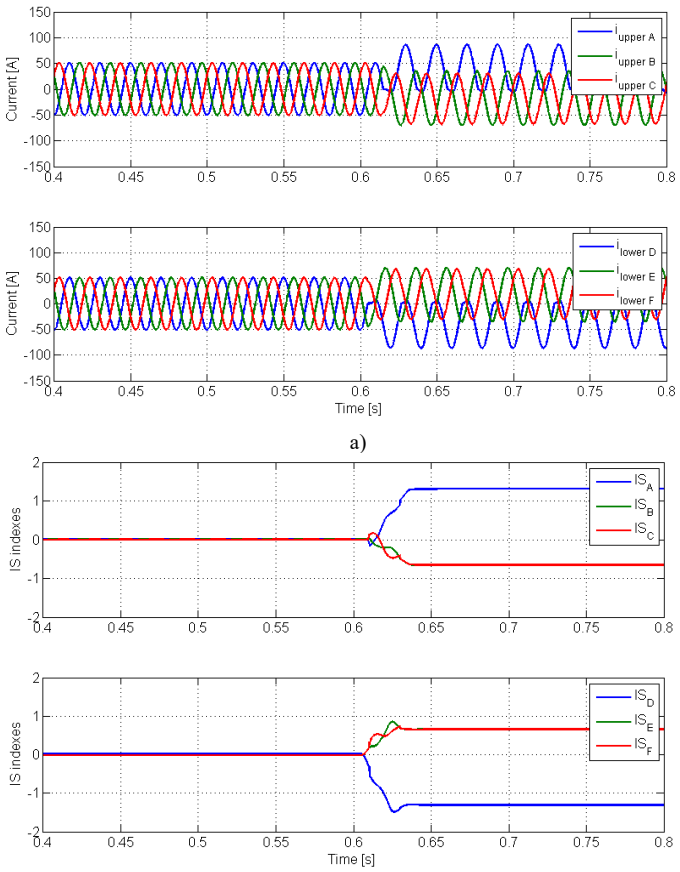


Fig. 2. Waveforms of the output currents of the T-Type-based NSVSI. a) In upper load, and in lower load, b) time behavior of the diagnostic variables S_{11} and index *ISj* (j=A to F) before and after an open switch in transistor S_{11}.

Based on the results shown in Fig. 2, it is clear that the affected phase is directly linked to the fault. This represents a possibility of identifying the faulty transistor. Furthermore, the amplitude of the remaining phase currents can also help the identification of this type of fault. In this case, the current in the load phase associated with the faulty transistor will increase the amplitude after the fault (the upper transistor for a positive value and the lower transistor for a negative value. The remaining phases are also affected but in a more attenuated way. Additionally, it is also evident (in Fig. 2 b)) that the indexes remain at zero before the occurrence of the fault in S_{11}. However, at t=0.6 s after the transistor faults, the indexes assume non-zero values. As expected, the indexes that are more affected are those associated with the leg in which the transistor under fault is located.

Fig. 3 shows the results of the currents in the two loads of the T-Type-based NSVSI, in normal conditions and after an

open switch fault in transistor S_{12} occurs. In the results presented in Fig. 3 a), in normal conditions all currents are the same amplitude until the fault occurs (in t = 0.6s). From the result presented in Fig. 3 b), when there is a switch fault (S_{12}), all the center of mass indexes will no longer be zero.

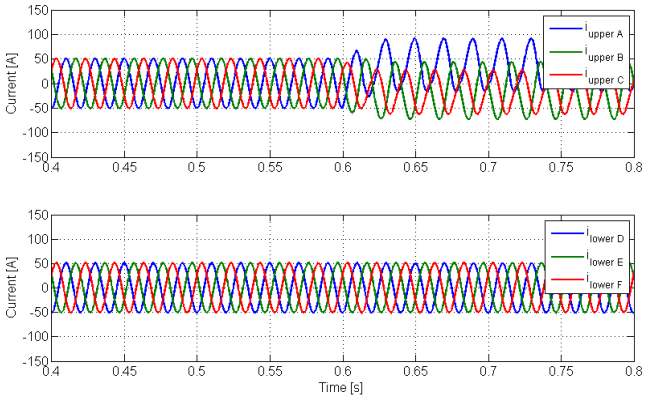


a)

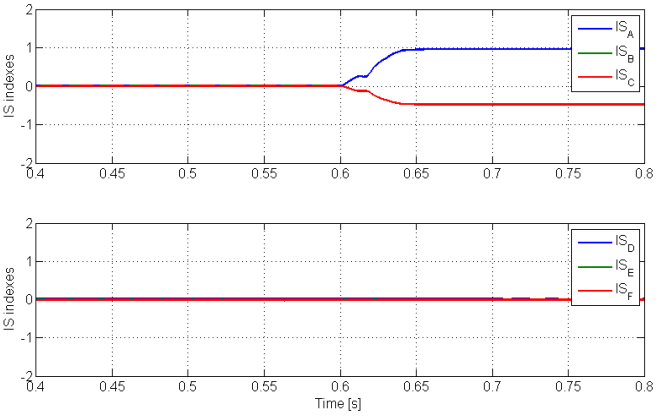
b)

Fig. 3. Waveforms of the output currents of the T-Type-based NSVSI. a) In upper load, and in lower load, b) time behavior of the diagnostic variables S_{12} and index *ISj* (j=A to F) before and after an open switch in transistor S_{12}.

Fig. 4 depicts the time behaviour of the currents into the two loads, operating under normal conditions, and suddenly, at t=0.6s, an open switch fault in transistor S_{m1} arises. This figure confirms that in normal conditions all currents are normalized, while in fault conditions the current in the load phase associated with the faulty transistor will increase the amplitude after the fault. In this case, it is also possible to see that the currents of the lower phases are not affected. It is also visible in Fig. 4 b) that before the fault in S_{m1} occurs, the indexes remain at zero, but when the fault happens at t=0.6 s, the indexes associated with the upper phases take on non-zero values. The most affected index is the one associated with the leg in which the fault switch is located. In this fault, the indexes related to the lower phases are not affected, by which they remain at zero value even after the switch fault.



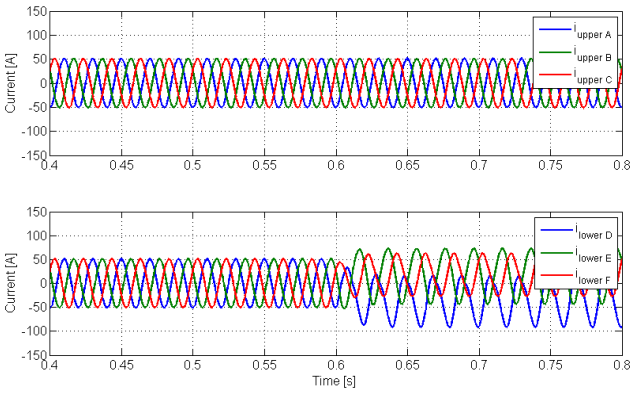
a)



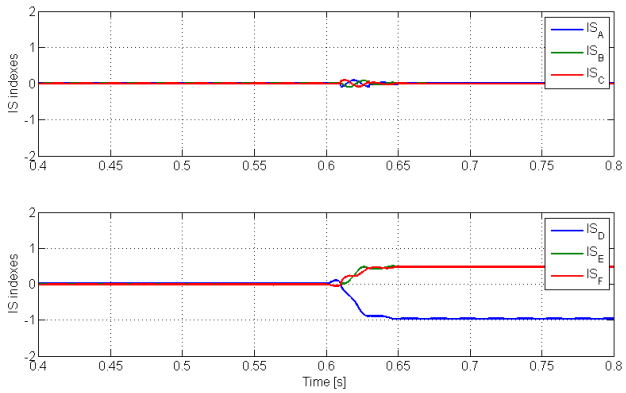
b)

Fig. 4. Waveforms of the output currents of the T-Type-based NSVSI. a) In upper load, and in lower load, b) time behavior of the diagnostic variables S_{m1} and index *ISj* (j=A to F) before and after an open switch in transistor S_{m1}.

The result of another test where the T-Type-based NSVSI operates routinely followed by an open switch fault is shown in Fig. 5. In this case, at 0.6 s an open switch fault is simulated for the transistor S_{m4}. The result confirms that in routine conditions all indexes present the same amplitude, while in fault conditions the index associated with the leg of the faulty transistor will change for the highest amplitude. In Fig. 5 b), before the fault in S_{m1} occurs, the indexes remain at zero, but when the fault happens at t=0.6 s, only the lower load indexes display non-zero values.



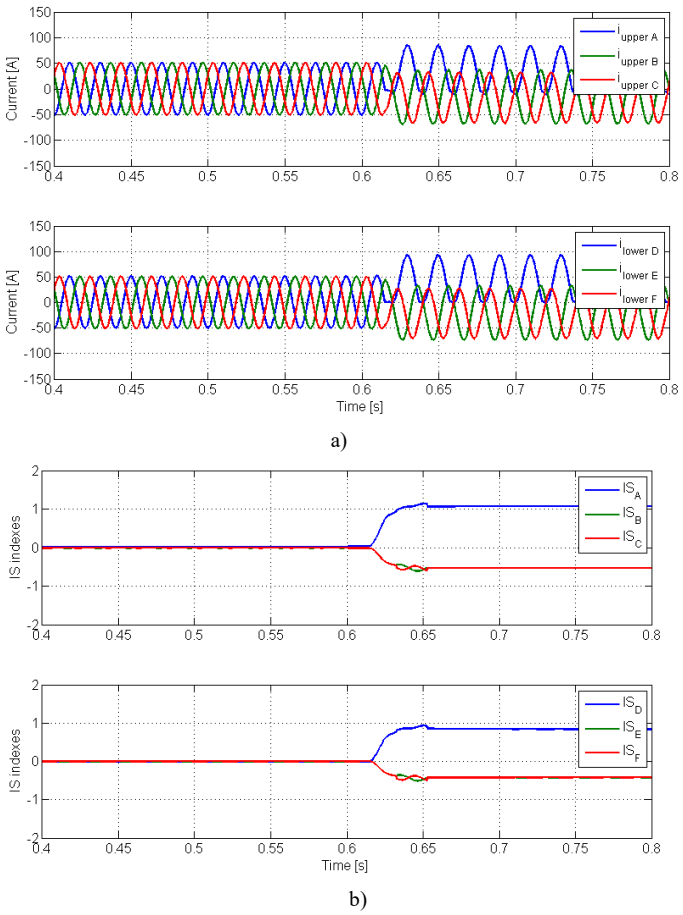
a)



b

Fig. 5. Waveforms of the output currents of the T-Type-based NSVSI. a) In upper load, and in lower load, b) time behavior of the diagnostic variables S_{m4} and index ISj (j=A to F) before and after an open switch in transistor S_{m4}.

The simulation result presented in Fig. 6, show the current waveforms in normal operation and when suddenly a fault occurs at t=0.6s on switch S_{13}. As expected, the diagnostic variable SI_j presents a similar behavior as in the simulation test of Fig. 2. However, index SI_A will now change from zero to the negative value of 0.9 confirming in this way that the fault is related with the lower switch (it now presents a symmetric behavior).



a)

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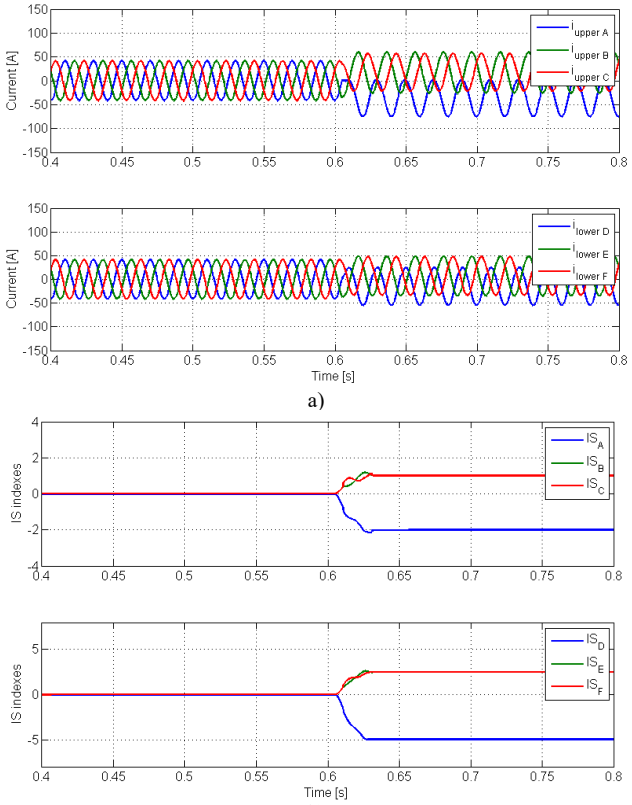
Fig. 6. Waveforms of the output currents of the T-Type-based NSVSI. a) In upper load, and in lower load, b) time behavior of the diagnostic variables S_{13} and index ISj (j=A to F) before and after an open switch in transistor S_{13}.

To assess the performance of the proposed diagnostic method, a simulation test was conducted with a decreased load value. By increasing the load value impedance lower current values are obtained. Thus, in Fig. 7 it is presented the simulation results considering a load step decrease. As in previous tests, initially, the diagnostic system was considered in normal operation, and at t=0.6 s suddenly there was an OC failure in switch S_{11}. The result confirms, as in previous tests, that in normal conditions all currents present the same amplitude, while in fault conditions the phase current associated with the faulty transistor will present a change in their amplitude. The other two currents remain with the same amplitude. In Fig. 7 b), when there is a switch fault (S_{11}), all of the center of mass indexes will no longer be zero. The found behavior is maintained, even for a light load.



a)

b)

Fig. 7. Waveforms of the output currents of the T-Type-based NSVSI. a) In upper load, and in lower load, b) time behavior of the diagnostic variables S_{11} and index ISj (j=A to F) before and after an open switch in transistor S_{11}, for a load reduction.

To evaluate the performance of the proposed diagnostic method, a simulation test was conducted when the frequency and duty cycle decreased in the lower load, from 55 Hz to 30 Hz and from 0.6 to 0.3, respectively. Fig. 8 shows results considering initially the system in normal operation, and at t=0.6 s suddenly there was an OC failure in switch S_{13}. This Fig. shows that under normal conditions, all currents are normalized, but in faulty conditions, the current in the affected load phase increases in amplitude. Additionally, Fig. 8b) illustrates that before the fault in S13, the indexes remain at zero, and after the fault at t=0.6 s, they become non-zero, even for these conditions. This simulation also confirms that the behavior is maintained.

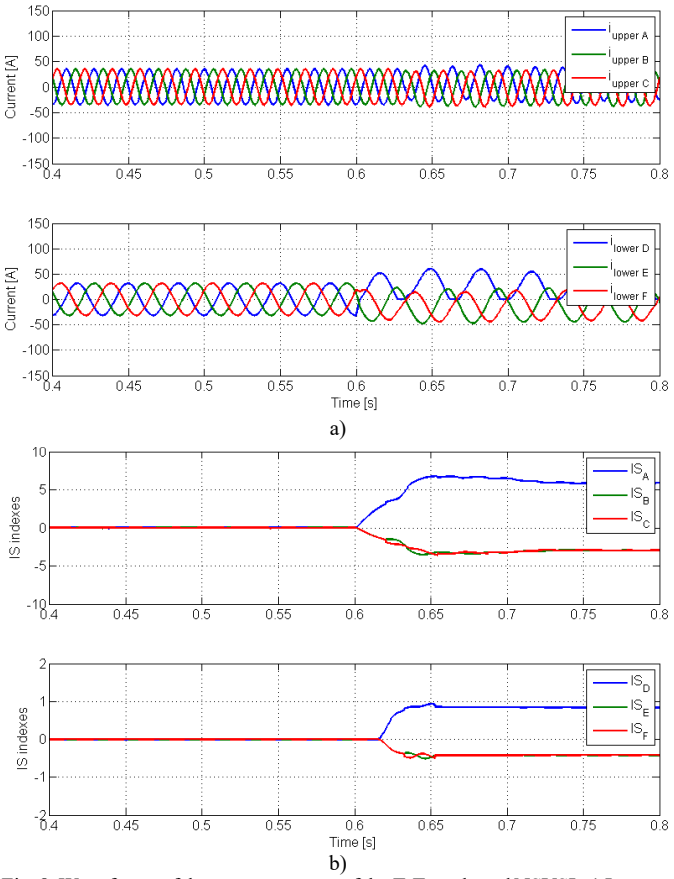


Fig. 8. Waveforms of the output currents of the T-Type-based NSVSI. a) In upper load, b) In lower load, c) time behavior of the diagnostic variables S_{13} and index *ISj* (j=A to F) before and after an open switch in transistor S_{11}, for a load reduction.

V. Conclusions

In this work a novel method for the detection and identification of faults in power transistors within a T-Type-based NSVSI multilevel inverter for a drive system is presented. The proposed approach relies on indexes derived from the analysis of phase current patterns, which are obtained from the behavior of currents in both loads. The values of the indexes are independent of the varying amplitudes of the currents. In fact, by defining a threshold value, it is possible to distinguish between normal and faulty conditions. The features of the proposed methodology were confirmed through several numerical tests. From this numerical analysis, the proposed methodology is a fast, robust solution and independent of the load conditions, confirming the theoretical considerations.

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