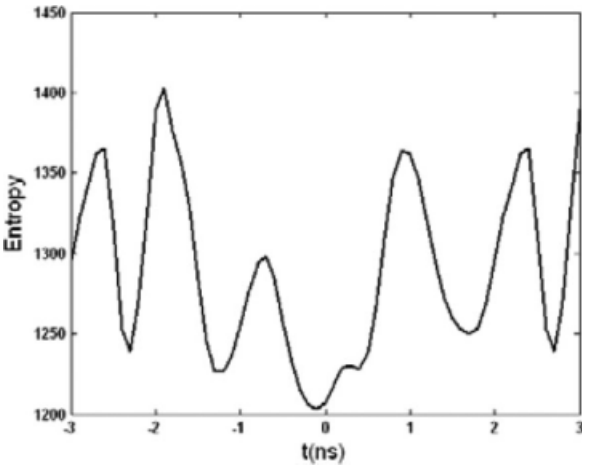

Figure 5 Image entropy at different focusing time, when the wall parameters are estimated as $\varepsilon_b = 6$, $\sigma = 0.05$ S/m, and $d = 0.15$ m

is incorporated in the proposed algorithm. A refocusing time factor is introduced to obtain a dynamic image at different focusing time. The choice of the optimal focusing time and the corresponding image can be determined by the minimum entropy criterion. Numerical and experimental results are presented to show the effectiveness of the proposed algorithm.

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RF RECEIVER FRONT END FOR 28.5 GHz APPLICATIONS ON A 70 GHz F_T SiGe BiCMOS PROCESS

Fernando Fortes,[1] Reza Mahmoudi,[2] and Arthur van Roermund[2]
[1] Instituto de Telecomunicações, Instituto Superior de Engenharia de Lisboa, Lisboa, Portugal; Corresponding author: ffortes@deetc.isel.ipl.pt
[2] Department of Electrical Engineering, MsM Group, Eindhoven University of Technology, Eindhoven, The Netherlands

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ABSTRACT: *This article presents the design and test of a receiver front end aimed at LMDS applications at 28.5 GHz. It presents a system-level design after which the receiver was designed. The receiver comprises an LNA, quadrature mixer and quadrature local oscillator. Experimental results at 24 GHz center frequency show a conversion voltage gain of 15 dB and conversion noise figure of 14.5 dB. The receiver operates from a 2.5 V power supply with a total current consumption of 31 mA.* © 2010 Wiley Periodicals, Inc. Microwave Opt Technol Lett 52: 736–740, 2010; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.25010

Key words: *RF front end; system design; SiGe BiCMOS; low millimeter-waveband*

1. INTRODUCTION

Silicon processes have experienced a continuous improvement in the last years making them suitable for applications in the low microwave range. As SiGe BiCMOS processes become mature and with better quality passive components, they compete with GaAs also in the lower millimeter waveband. In fact, recently reported work [1, 2] show the ability of SiGe BiCMOS in the integration of receivers for the low-millimeter waveband.

This article describes the design and test of an integrated SiGe RF receiver front end from the top level specifications dictated by IEEE 802.16 [3] standards, down to circuit level design and implementation. Part of this work was already presented at APMC 2009 [4], namely the detailed circuit design and experimental data. The current article goes beyond and presents also the system level design, which was performed to find the set of RF parameters for the building blocks design.

The RF receiver front end is aimed at 28.5 GHz center frequency for LMDS applications considering one carrier transmission [3]. The receiver chip was implemented in a 0.25 μm SiGe BiCMOS process [5]. Although this process was optimized for a decade lower than the current application, the passive components have reasonable quality factors at the target frequency of 28.5 GHz. The active devices have 70 GHz peak-f_T, which is just slightly above twice the target frequency. Due to the limited performance of the active devices, the whole receiver is studied according to the system specifications to make the best out of the technology. This is done by dividing the receiver front-end design in two parts: first, a system-level study to translate IEEE

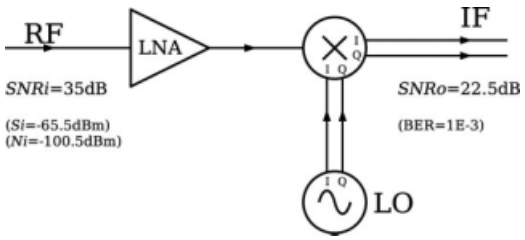

Figure 1 Receiver system

802.16 standard specifications into building blocks RF parameters; second, the design of the building blocks according to their specifications. Experimental data is also presented to validate the circuit design.

2. SYSTEM LEVEL DESIGN

The goal of the system level design is to translate the whole RF receiver specifications into RF parameters for the system building blocks. In this way, it is possible to obtain several solutions for the building blocks specifications enabling a proper choice for the whole system performance. This is especially important for the design of this system where the technology is pushed to the limit.

Figure 1 shows the receiver system with the LNA, quadrature mixer, and oscillator. The design of this receiver front end is aimed at LMDS specifications [3] at 28.5 GHz center frequency and 22.4 MHz symbol rate with 64QAM modulation using one carrier. Under these conditions, the system must provide BER = 1E-3 for an RF input power of −65.5 dBm.

At the input of the receiver, the noise power is imposed by the 22.4 MHz symbol rate becoming Ni = KTB = −100.5 dBm resulting in a 35 dB input signal to noise ratio SNRi. At the output of the receiver, the SNRo is imposed by the value of BER = 1E-3, resulting in 22.5 dB for a 64QAM signal [6]. Therefore, by considering additive white noise as the only impairment, the receiver may have a noise figure of 12.5 dB.

The other impairment considered in this design is the phase noise from the local oscillator, which degrades the noise figure of the receiver. Because the two impairments have different behavior, system simulations were performed to evaluate them simultaneously. The simulations were performed with Agilent's Envelope Simulator from ADS. The system for evaluation consists on a custom designed RF transmitter according the specifications, the receiver, a symbol detector, and comparator.

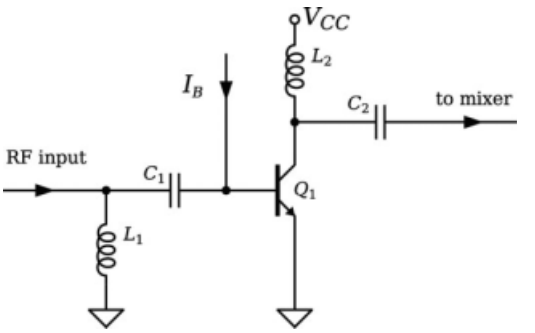

Figure 3 LNA circuit

The RF transmitter generates one carrier with a 22.4 MHz symbol rate 64QAM sequence during 2 ms. Baseband filtering is a square-root raised cosine with 25% excess bandwidth. The receiver is a zero IF similar to the one in Figure 1 with configurable noise figure and gain for the LNA and mixer. The phase noise of the local oscillator is also configurable. At the output of the system, the signal is filtered with the same filter as in the transmitter to recover the symbols. The received sequence is then compared with the transmitted one to find the wrong symbols and compute the BER.

Figure 2 shows the BER as a function of SNRo and phase noise. The phase-noise values are defined at 100 kHz distance from the carrier. As expected, for a low value of the phase noise, the curve approaches the theoretical values of [6]. The curves also enable the definition of a threshold for the phase-noise value above which the oscillator is useless. For the case of this system with this modulation scheme, a phase noise of −95 dBc at 100 kHz degrades *SNRo* by 1 dB. Recalling the initial NF of 12.5 dB for the whole system, the new value has to be 11.5 dB to accommodate the 1 dB degradation.

The distribution of NF and gain of the LNA and mixer depend on their circuit design. A previous design on the same SiGe BiCMOS process [7] has shown the possibility to obtain an LNA with a gain close to 10 dB and a noise figure below 7 dB at the target frequency of 28.5 GHz. With these values and according to Friis formulation, the noise figure of the mixer can be up to 19 dB for a whole system NF close to 11 dB.

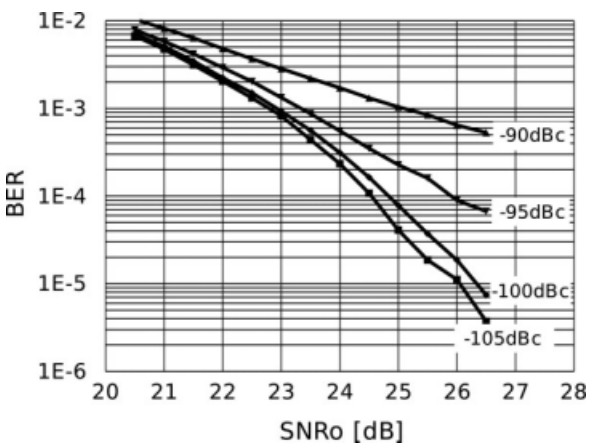

Figure 2 BER dependence on SNR and phase-noise

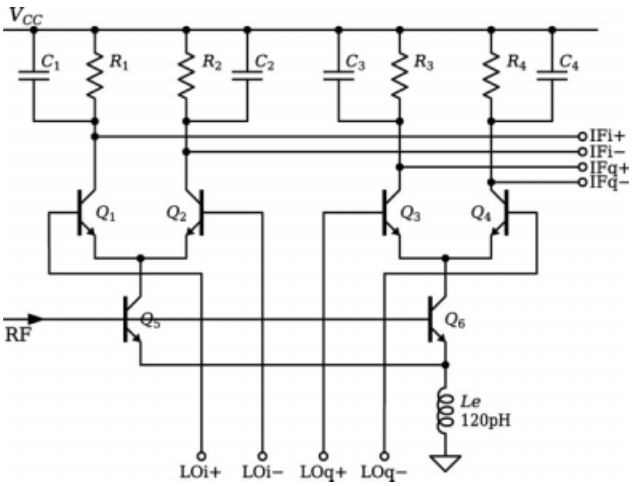

Figure 4 Quadrature mixer circuit

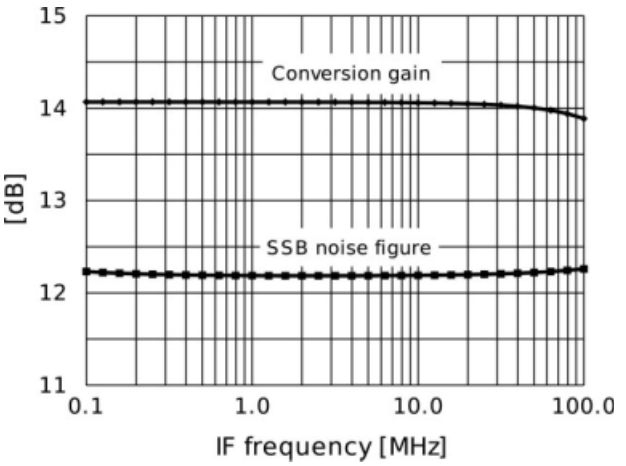

Figure 5 Simulated receiver performance at 28.5 GHz local oscillator frequency, with 4.5 mA LNA bias and 9 mA mixer bias

3. RECEIVER CIRCUIT DESIGN

The design of the RF receiver front end is made according to the system described in Figure 1. It is composed by an LNA, a quadrature mixer, and a quadrature oscillator. The RF parameters for these blocks are the ones described in the previous section.

The LNA circuit is presented in Figure 3, in a common emitter single-ended input and output configuration. The design has taken into account the optimum active device dimensions, its bias, and matching networks. The active device has two base contacts and has the largest emitter length of 20.7 μm and the shortest base width of 0.5 μm. This configuration provides the lowest base resistance [7], which is important in LNA design and an equivalent noise resistance Rn close to 50 Ω. With a bias of $I_C = 4.5$ mA and $V_{CE} = 2.5$ V, the device provides NFmin = 5.0 dB and GMAX = 10 dB. The input port matching for 50 Ω is made with inductor $L_1 = 280$ pH, whereas C_1 is for AC coupling. With this inductor at 28.5 GHz, the base of the device is loaded with an admittance ys = $1-j1$, which is a compromise between gain, input matching, and noise figure [7]. The output matching network for 100 Ω is made with $L_2 = 420$ pH and $C_2 = 100$ fF. The output impedance of the LNA is 100 Ω to conjugately match the input impedance of the quadrature mixer. The LNA was simulated under 2.5 V, 4.5 mA operation point, and provides 9.2 dB gain and 5.6 dB noise figure at 28.5 GHz without the input bond-pad effect. With the input bond-pad effect, the gain shifts to 8.7 dB and the noise figure to 6.1 dB.

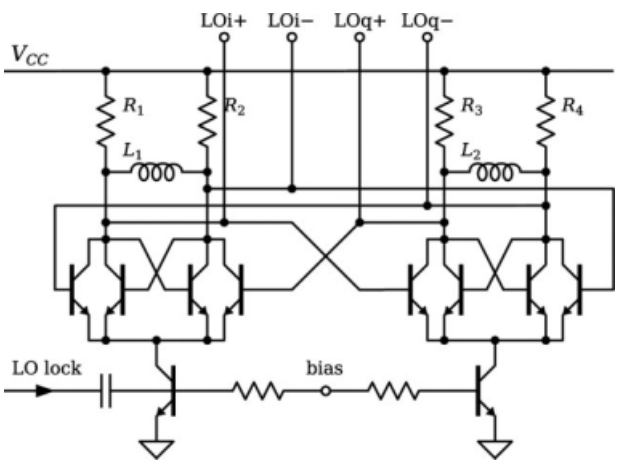

Figure 6 Local oscillator circuit

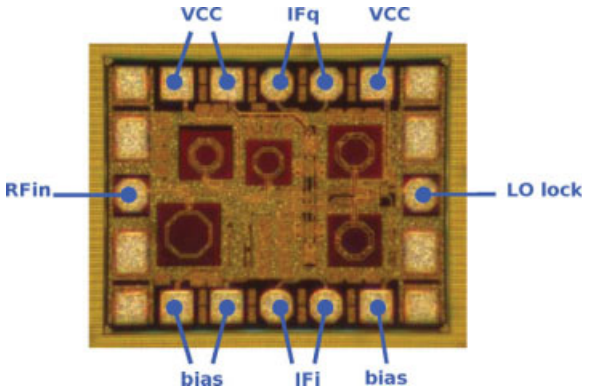

Figure 7 Receiver chip photograph. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

The quadrature mixer circuit is presented in Figure 4. This mixer has single-ended input for the RF signal and differential IQ output for the IF signal. In accordance, it uses two differential pairs as multiplying cells instead of Gilbert-cells to recover the I and Q paths. Devices Q_5 and Q_6 act as current sources steered by the RF signal, whereas devices Q_1–Q_4 switch the RF current according the LO signal. Resistors R_1–R_4 of 150 Ω and capacitors C_1–C_4 of 1.6 pF form a 660 MHz low-pass filter to reject mainly the LO component at the IF output. The disadvantage of using differential pairs instead of Gilbert cells is the lack of LO rejection at the IF output, but it has the advantage of having a single-ended RF input and so no need for a balun. The 120 pH inductor Le is used to degenerate the gain cells of the mixer. This inductor is important because it improves the mixer linearity and places the input impedance of the mixer close to 100 Ω, enabling impedance matching for the LNA. The mixer circuit was simulated under 2.5 V power supply and 9 mA current consumption and provides a single ended to differential conversion gain of 5 dB and a SSB noise figure of 17.5 dB at 28.5 GHz. With the IF outputs open, the mixer has a −3 dB bandwidth larger than 600 MHz.

The simulated conversion gain and SSB noise figure of the complete receiver is represented in Figure 5. The simulation was made with the same bias conditions of the isolated blocks.

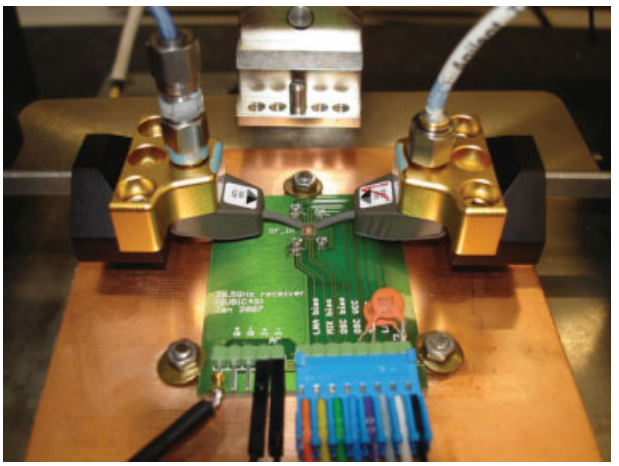

Figure 8 Measurement setup. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

The receiver produces 14 dB conversion gain and 12 dB noise figure at 28.5 GHz local oscillator frequency.

The local oscillator circuit is presented in Figure 6. It has two LC oscillators, which are coupled to obtain proper quadrature for the mixer. Resistors R_1–R_4 create the adequate voltage bias to the mixer, enabling direct connection to it. The oscillator has an input to allow injection lock from an external source with twice the frequency. Simulations predict 1 GHz bandwidth lock centered at 28.5 GHz with an input power of −7 dBm. Lower values of power decrease the lock bandwidth.

The process used to implement the receiver chip was the 0.25 μm BiCMOS process from Philips [5]. This process provides SiGe HBTs with peak f_T/f_{MAX} of 70/100 GHz, MIM capacitors and spiral inductors with reasonable Q-factor up to a few GHz due to the 3 μm thick top metal layer. At higher frequencies, close to the low millimeter waveband, it is possible to obtain inductors with Q-factors close to 20 [5]. The complete receiver chip photograph is shown in Figure 7, with a total die area of 800 μm × 620 μm. The RF input port and oscillator lock input port are located on the left and right side, whereas the upper and lower row of pads are reserved for the DC connections and IF outputs. A mesh grid of metal was included for proper ground connection between components.

4. EXPERIMENTAL RESULTS

Figure 8 shows a photograph of the measurement setup. Due to the large number of connections, the chip was mounted on a printed circuit board, and the low frequency pads (V_{CC}, bias, and IF outputs) were wire bonded to facilitate the measurement setup. The RF input port and oscillator lock input port are located on the left and right side, respectively, and are connected with coplanar ground-signal-ground on-wafer probes.

The conversion gain measurements were made with the setup shown in Figure 9. An Agilent E8267D was used as RF signal generator at the input of the system. The IF output was measured with an Agilent E4446A spectrum analyzer with an external 87405B preamplifier. The required conversion between the mixer differential output and the single-ended measurement system is made with an Agilent 1141A differential probe. The LO external reference was obtained by doubling the frequency of an Agilent E8257D. The doubling process has major losses providing an available power of −23 dBm at the maximum output power from the generator.

The on-chip local oscillator had a free running center frequency of 24 GHz instead of the simulated 28.5 GHz, which affects the whole system performance and limits the measurements. This difference in frequency can be attributed to a less accurate model for inductor or parasitics not considered in the simulations. The external LO reference should be able to lock the divider into a higher frequency; however, the available

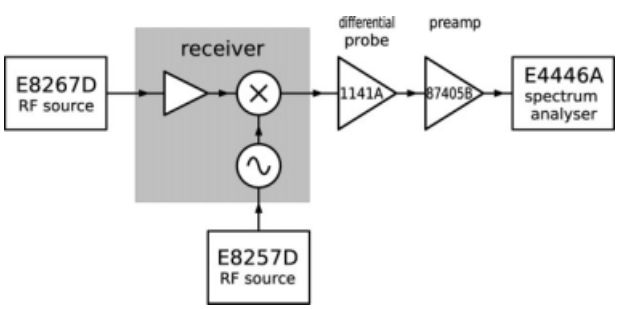

Figure 9 Conversion gain measurement setup

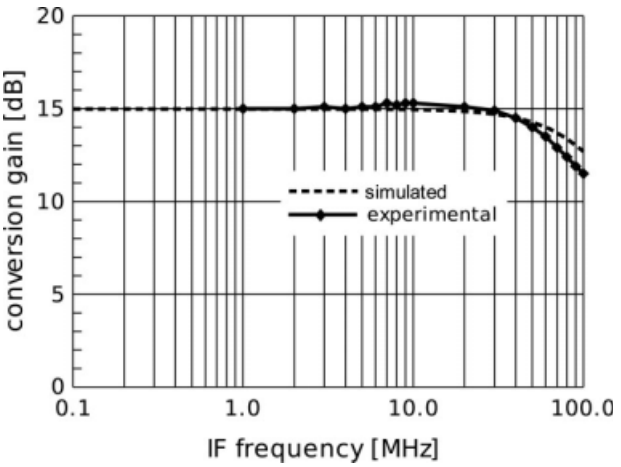

Figure 10 Comparison between simulated and measured conversion gain

power of −23 dBm was not able to lock the oscillator more than a few hundredths of GHz above 24 GHz. Therefore, the measurements and comparison with simulations are presented at 24 GHz, with a power supply of 2.5 V and LNA and mixer bias are 4.5 mA and 9 mA, respectively.

Figure 10 shows the comparison between simulated and measured conversion gain. The comparison shows a good agreement with a gain of 15dB. The IF channel has a −3 dB cuttoff frequency of 90 MHz, which is lower than the expected value from the previous sections, but this is due to the 7 pF input capacitor of the differential probe.

The measurement of the noise figure was made with a test setup similar to the one in Figure 9 but with an Agilent 346C noise source in place of the RF generator, controlled by the spectrum analyzer. Figure 11 shows the comparison between simulated and measured noise figure. The measured noise figure is 14.5 dB from 10 MHz to 20 MHz and is 1 dB higher than predicted. This difference can be attributed to an on-chip temperature higher than expected and not accounted for in the simulations. The measured noise figure increases for low frequencies, but this is due to limitations of the measurement setup as the 87505B preamplifier has a lower cutoff frequency of 10 MHz, which limits the accuracy of noise figure calculations on the spectrum analyzer below this frequency.

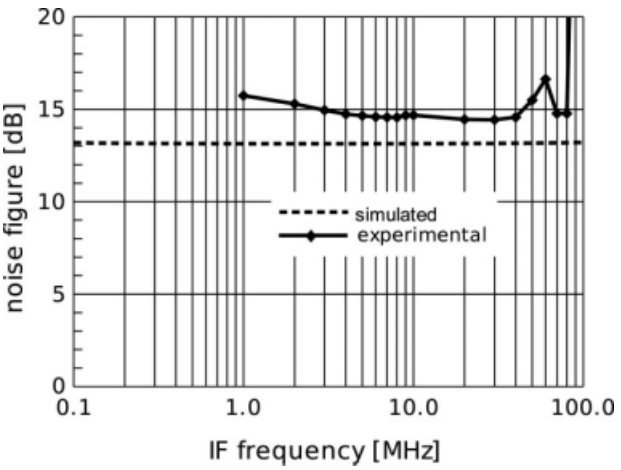

Figure 11 Comparison between simulated and measured conversion SSB noise figure

5. CONCLUSIONS

This article has presented the design of an integrated RF receiver front end for 28.5 GHz applications on a 0.25 μm SiGe process from top level specifications down to the circuit level and chip design and experimental measurements. System calculations and simulations considering additive white noise and phase noise simultaneously were presented to enable the definition of specifications for the building blocks of the receiver. The LNA and quadrature mixer were designed according to the specifications and also the local oscillator. The receiver chip revealed an oscillator running at 24 GHz instead of the design frequency of 28.5 GHz. Accordingly, experimental measurements were taken at 24 GHz; they showed 15 dB conversion gain with -3 dB bandwidth of 90 MHz and a noise figure of 14.5 dB. The values are close to the predicted ones by simulation.

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SIX-PORT TRANSCEIVER FOR 6–9 GHz ULTRAWIDEBAND SYSTEMS

Adriana Serban,[1] Joakim Östh,[1] Owais,[1] Magnus Karlsson,[1] Shaofang Gong,[1] Jaap Haartsen,[2] and Peter Karlsson[2]

[1] Department of Science and Technology (ITN), Linköping University, Norrköping, Bredgatan 33, SE-60174 Norrköping, Sweden; Corresponding author: Adriana.Serban@itn.liu.se

[2] Sony Ericsson Mobile Communications AB, Lund, Sweden, Nya Vattentornet, SE-22188 Lund, Sweden

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ABSTRACT: *An ultrawideband 6–9 GHz six-port correlator is designed and manufactured. Based on this six-port correlator, behavioral models, and true component circuit designs of a transceiver are developed to study the performance of the proposed direct conversion ultrawideband transceiver topology. A new six-port modulator with controllable impedance terminations implemented with a field effect transistor in the linear operation region is presented.* © 2010 Wiley Periodicals, Inc. Microwave Opt Technol Lett 52: 740–746, 2010; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.25021

Key words: *six-port transceiver; six-port transmitter; six-port receiver; UWB systems*

1. INTRODUCTION

The six-port correlator is a passive circuit that has been used for different low-cost measurement applications at microwave frequencies since the 1960s [1–3]. More recently, six-port receivers and transmitters were intensively studied as possible solutions for high-speed wireless communication systems [4–9]. Our interest in six-port radio architecture has concerned to ultrawideband (UWB) radio front-end topologies for short-distance wireless communications. It has firstly resulted in a 3.1–4.8 GHz six-port transmitter and receiver pair implemented in a low-cost printed circuit board (PCB) process [10]. This frequency range corresponds to the Band Group 1 of the multiband orthogonal frequency division multiplexing (OFDM) specification as initially proposed by the WiMedia Alliance [11]. In USA, the authorized UWB spectrum was defined by Federal Communication Commission (FCC) in the range 3.1 to 10.6 GHz [12]. From a regulatory point of view, FCC has only restricted the power levels (maximum mean equivalent isotropic radiated power density of a UWB transmitter is -41.3 dBm/MHz) in the band 3.1–10.6 GHz. In Europe, Asia, and Japan, additional restrictions have been put on the 3.1–4.8 GHz band in the form of LDC (Low Duty Cycle) and DAA (Detect And Avoid) [13]. From an industrial point of view, the telecom world including operators and handset manufacturers is very concerned about coexistence and colocation issues. To avoid interference with other radio systems, the 6–9 GHz band is preferred to be used for UWB. This is also reflected from the strategy of the Bluetooth SIG which only considers UWB as an alternative MAC/PHY layer if it operates in the 6–9 GHz band. Thus, for world-wide interoperability of the UWB devices and in the absence of a UWB radio standard, the 6–9 GHz frequency range is of large interest.

In this article, a 6–9 GHz six-port transceiver for high-speed data transmission is presented. Compared with our previous 3.1–4.8 GHz six-port transmitter-receiver pair [10], the new design requires new circuit solutions and design approaches to fulfill operation with high-bit rates above Gbit/s at high frequency (6–9 GHz). The expected bit rate can be achieved by optimally chosen radio architecture and modulation technique [14]. Using the top-down design methodology, behavioral models of the receiver and transmitter were firstly developed using Advanced Design System (ADS) from Agilent Technologies. Simulation set-ups for QPSK (quadrature phase shift keying), 16- and 64-QAM (quadrature amplitude modulation) modulation/demodulation applications of the six-port transmitter and receiver were developed in ADS Analog/RF and DSP modes. The 6–9 GHz six-port correlator was designed and manufactured on a double-sided Rogers4350B printed circuit board (PCB).

2. SYSTEM ARCHITECTURE AND BEHAVIORAL MODELING

The proposed block diagram of the 6–9 GHz direct conversion radio front-end is shown in Figure 1. It uses a single six-port correlator for both transmitter (Tx) mode and receiver (Rx) mode. In the Rx mode, the modulated RF signal and the local oscillator (LO) signal are fed into the six-port correlator and,