

A Dual-Output NPC-Type Converter with a Model Predictive Controller with Compensation of DC Capacitor Voltage Imbalance

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Abstract— The dual output three-level converter is now important for several applications namely dual motor drives. The recent dual output nine-switch multilevel three-phase inverter, based on the NPC-Type structure, has been studied in open loop at nominal conditions, without closed loop control. Moreover, the dual output nine-switch multilevel inverter may present issues related to load currents control and to the unbalance of two series capacitor voltages in the dc-link. Thus, in this research work the model predictive controller (MPC) is proposed for closed loop current control, as well as for mitigation of the capacitor voltages imbalance. The MPC approach allows the minimization of a cost functional weighing two criteria, the tracking errors of the three-phase AC currents of each inverter output, as well as the two capacitors voltage imbalance. Several simulations showing the performance of the proposed control strategy are presented and discussed.

Keywords— Dual output inverter, nine-switch inverter, NPC-Type converter; multilevel inverter; model predictive control (MPC).

I. INTRODUCTION

In the last years the evolution of the power electronics converters topologies has been mainly focused on reducing the number of active and passive components, allowing a reduction of the converter cost and volume. The multilevel inverter is an example of these improvements, while showing also several advantages when compared with the classical two-level topologies, namely in terms of quality of output voltage waveforms and the reduction of harmonic content [1,2]. Accordingly, the use of multilevel inverters has been extended to many industrial applications, such as AC motor drives, storage systems, renewable energy sources, active power filters, and High Voltage DC transmission among others [3-5].

The most cited multilevel inverter structures, for the aforementioned applications, have been the clamped neutral point inverter (NPC), the cascaded H-bridge inverter (CHB), and the flying capacitor inverter [6-8]. All these topologies have been important for medium and low voltage applications. In addition to these classic topologies, many other variants have appeared which are advantageous for certain applications [9-14]. Among the various proposed multilevel topologies, the dual output multilevel converter deserved attention in this work, as it is based on the NPC-Type structure and uses the common switches the same way as the 9-switch inverter [15]. The dual output multilevel converter has a smaller number of diodes and switches in comparison to equivalent two three-level conventional inverters allowing high performance and reduced switching losses [16,17]. The

industrial applications for this converter are much diversified, already disclosed in many published works. The most useful feature is the ability to have dual-output voltage, suited for many applications, namely in dual motor drives [18-20].

Regarding the control applied to this dual output multilevel (3 level) converter, only open loop control studies under nominal operating conditions were reported, where several modulation pulse-width modulation (PWM) strategies are applied [19,20]. In [19] a dual-output neutral-point clamped three-level inverter with a modulation strategy, combining the time-sharing modulation and virtual space vector pulse-width modulation (VSVPWM) was proposed. In [20] a modified discontinuous PWM scheme is proposed with a dual-output three-level topology to minimize the voltage stress across switches and improve the input current and output voltage quality. However, the proposed modulation techniques show issues related to the control of the AC currents, in both outputs, and also on the balance of the voltages in the DC capacitors.

To solve these issues, one of the control techniques that have been used in power electronics converters, with good results, is the model predictive control (MPC) [21-25]. In fact, this control technique presents several advantages, such as fast dynamic response, simple concept, readiness for multivariable systems while able to deal with nonlinearities and constraints [26-29]. Although MPC has been demonstrated to be interesting and effective to control AC currents in single output multilevel converters, it has not been tested yet in the three-phase with dual output three-level converter, where a relatively high number of voltage vectors must be accounted for. Nevertheless, MPC seems to be an interesting solution to be developed and applied to the dual output three-level converter. The application of MPC to multilevel converter must consider the control of the converter AC currents and the DC capacitors voltage imbalance.

In this paper, a controller for the three-phase dual output multilevel converter based on the MPC approach is proposed. The predictive controller was designed to consider the different variables that need to be controlled in the three-phase dual output multilevel converter specific topology. Thus, a MPC is derived to control not only the converters AC currents but also the DC capacitors voltage imbalance. To check the performance of the control systems used, various simulation tests in stationary and transient states are presented and discussed.

II. MODEL OF THE DUAL-OUTPUT NPC-TYPE CONVERTER

The configuration of the dual output three-level NPC-Type inverter used in this work is presented in Fig. 1. This topology is based on the conventional three-level structure and 9-switch inverter [12]. This three-level structure allows a dual output three-level inverter by using the common switches in the same way as the 9 switch inverter, reducing volume and cost.

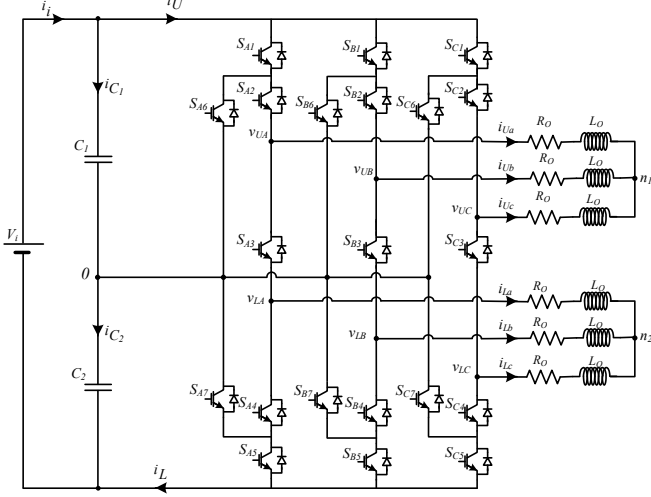


Fig. 1. Circuit of the dual output three-level NPC-Type converter.

From the analysis of the dual output three-level inverter, assuming ideal switches (power semiconductors), the state of each active switch can be represented using a binary variable, being the switch state defined as follows:

$$\begin{cases} d_{ij} = 1 & , \text{ if } S_{ij} \text{ is ON} \\ d_{ij} = 0 & , \text{ if } S_{ij} \text{ is OFF} \end{cases} \quad (1)$$

where $i=A,B,C$ and $j=1..7$.

The voltages between the upper and lower AC terminals of the inverter and the middle point of the capacitors can also be described as functions of the switches states (2).

$$\begin{cases} v_{Ui0} = (d_{i1}d_{i2} + 1 - d_{i3}d_{i4}d_{i5})(1 - d_{i2}d_{i6}) \frac{V_{DC}}{2} \\ v_{Li0} = (d_{i1}d_{i2}d_{i3} + 1 - d_{i4}d_{i5})(1 - d_{i4}d_{i7}) \frac{V_{DC}}{2} \end{cases} \quad (2)$$

In accordance with the previous relationship, the following switching functions will be defined:

$$\begin{cases} \alpha_{Ui} = \frac{(d_{i1}d_{i2} + 1 - d_{i3}d_{i4}d_{i5})(1 - d_{i2}d_{i6})}{2} \\ \alpha_{Li} = \frac{(d_{i1}d_{i2}d_{i3} + 1 - d_{i4}d_{i5})(1 - d_{i4}d_{i7})}{2} \end{cases} \quad (3)$$

The previous equations allow the following mathematical model of the voltages applied to the load:

$$\begin{bmatrix} v_{UA} \\ v_{UB} \\ v_{UC} \\ v_{LA} \\ v_{LB} \\ v_{LC} \end{bmatrix} = \frac{V_{DC}}{3} \begin{bmatrix} 2 & -1 & -1 & 0 & 0 & 0 \\ -1 & 2 & -1 & 0 & 0 & 0 \\ -1 & -1 & 2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 2 & -1 & -1 \\ 0 & 0 & 0 & -1 & 2 & -1 \\ 0 & 0 & 0 & -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} \alpha_{UA} \\ \alpha_{UB} \\ \alpha_{UC} \\ \alpha_{LA} \\ \alpha_{LB} \\ \alpha_{LC} \end{bmatrix} \quad (4)$$

Converting the previous equation from real coordinates abc to $\alpha\beta$ coordinates, equation (5) is obtained:

$$\begin{bmatrix} v_{U\alpha} \\ v_{U\beta} \\ v_{L\alpha} \\ v_{L\beta} \end{bmatrix} = V_{DC} \begin{bmatrix} \sqrt{\frac{2}{3}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} & 0 & 0 & 0 \\ 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} & 0 & 0 & 0 \\ -1 & -1 & 2 & 0 & 0 & 0 \\ 0 & 0 & 0 & \sqrt{\frac{2}{3}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} \\ 0 & 0 & 0 & 0 & \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} \\ 0 & 0 & 0 & -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} \alpha_{UA} \\ \alpha_{UB} \\ \alpha_{UC} \\ \alpha_{LA} \\ \alpha_{LB} \\ \alpha_{LC} \end{bmatrix} \quad (5)$$

Analysing equation (5) and considering the combination of all the states d_{ij} of the power semiconductors, 216 different output voltage space vectors are obtained. Many of these vectors are redundant from the point of view of the load voltages.

III. MODEL PREDICTIVE CONTROL OF THE DUAL-OUTPUT NPC-TYPE CONVERTER

The generic predictive control diagram depicted in fig. 2 is used for the dual output three-level inverter. The proposed control technique uses the converter voltages, defined in the last section, to predict the future behavior of the AC currents and DC capacitor voltages. In MPC the actual values of the AC load current, the capacitors voltages, and the input currents are measured in the $t(h)$ instant. Based on these values, the AC load currents, and the voltages of the capacitors can be predicted in the $t(h+1)$ instant. The sequence of the optimal voltage vector selection is calculated by minimizing a defined cost functional, the minimization giving the optimal switching state, which then ensures the minimum value for the function of the errors between references and their predicted values. The whole process is repeated for each sampling instant, considering new acquired data.

From the previous criteria and the control scheme shown in Fig. 2, the AC load currents, i_{jk} ($k=A,B,C$), of each dual outputs, j , ($j \in \{U, L\}$) at the t_{h+1} instant, can be predicted according the discrete-time approach (6).

$$i_{jk}(h+1) = \left(1 - \frac{R_o}{L_o} T_s\right) i_{jk}(h) + \frac{T_s}{L_o} v(h) \quad (6)$$

where $i_{jk}(h)$ is the AC load currents measured and $i_{jk}(h+1)$ is the AC currents to be predicted for the next $(h+1)$ sampling interval, T_s is the sampling time.

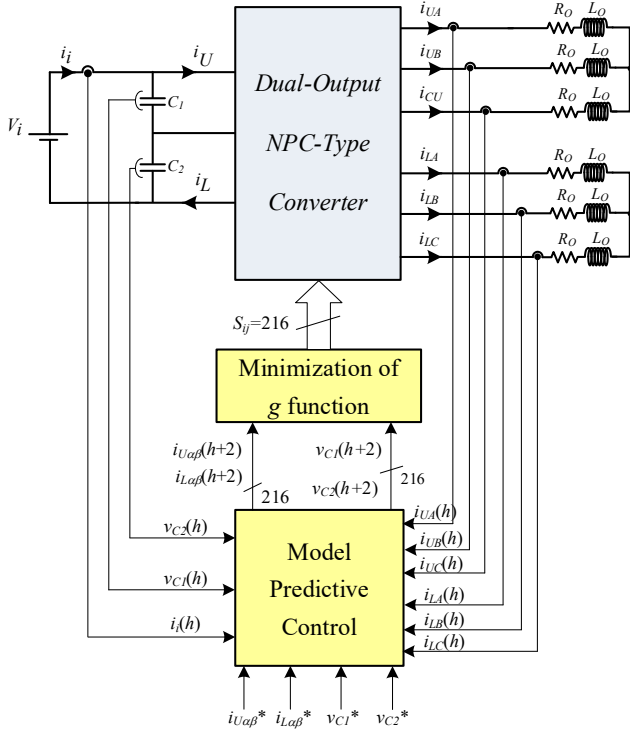


Fig. 2. Circuit of the dual output three-level NPC-Type converter.

The discrete time equations for the capacitors (C_1 and C_2) voltages, using the MPC theory, are obtained according to the expression (7) and (8).

$$v_{C1}(h+1) = v_{C1}(h) + \frac{1}{C_1} i_{C1}(h) T_s \quad (7)$$

$$v_{C2}(h+1) = v_{C2}(h) + \frac{1}{C_2} i_{C2}(h) T_s \quad (8)$$

where the currents $i_{C1}(h)$ and $i_{C2}(h)$ depend on the switching states of the dual output NPC-Type inverter and the value of the AC output currents, according to expression (9) and (10):

$$i_{C1}(h) = i_i(h) - i_U(h) = i_i(h) - [d_{A1} i_{UA} + d_{B6} i_{UB} + d_{C11} i_{UC} + d_{A1} d_{A2} i_{LA} + d_{B6} d_{B7} i_{LB} + d_{C11} d_{C12} i_{LC}] \quad (9)$$

$$i_{C2}(h) = i_i(h) + i_L(h) = i_i(h) - [d_{A3} i_{LA} + d_{B8} i_{LB} + d_{C13} i_{LC} + d_{A2} d_{A3} i_{UA} + d_{B8} d_{B7} i_{UB} + d_{C13} d_{C12} i_{UC}] \quad (10)$$

where $i_i(h)$ is the current from the DC source and $i_U(h)$, $i_L(h)$ are the currents in the upper and lower sides of the converter DC buses, respectively.

To compensate the computational time for the evaluation control algorithm, delay compensation techniques have been introduced. This compensation technique consists of using for the predictive control method the future current at $t(h+2)$ instant.

Thus, the AC load future currents are acquired by time-shifting the model (6) one step forward as:

$$i_{jk}(h+2) = \left(1 - \frac{R_o}{L_o} T_s\right) i_{jk}(h+1) + \frac{T_s}{L_o} v(h+1) \quad (11)$$

Employing the delay compensation technique, for the capacitors voltages, in (7) and (8), the future of the capacitors voltages at the instant $(h+2)$ is obtained as follows:

$$v_{C1}(h+2) = v_{C1}(h+1) + \frac{1}{C_1} i_{C1}(h+1) T_s \quad (12)$$

$$v_{C2}(h+2) = v_{C2}(h+1) + \frac{1}{C_2} i_{C2}(h+1) T_s \quad (13)$$

The main goal of the MPC must be the minimization of the AC load currents errors, the DC bus voltage error and also the imbalance of the capacitors voltage (or the neutral-point voltage), using a suitable cost function for each tracking error. Therefore, the proposed MPC cost functional is actually comprised of two weighted cost terms, one for the output currents another for the capacitors voltage imbalance. For the AC load currents, the cost function is defined as:

$$g_{ji} = |i_{j\alpha}^*(h+2) - i_{j\alpha}(h+2)| + |i_{j\beta}^*(h+2) - i_{j\beta}(h+2)| \quad (14)$$

where $i_{j\alpha}^*(h+1)$, $i_{j\beta}^*(h+1)$ are respectively, the real and imaginary parts, of the output currents references and $i_{j\alpha}(h+2)$, $i_{j\beta}(h+2)$ are respectively, the real and imaginary parts, of the output currents predicted. Similarly, the cost function of the capacitors voltages imbalance can be defined as:

$$g_{vc} = |v_{C1}(h+2) - v_{C2}(h+2)| \quad (15)$$

where $v_{C1}(h+1)$, $v_{C2}(h+1)$ are the predicted voltages of the C_1 and C_2 , capacitors. The proposed cost functional for the dual output three-level inverter MPC control, is given as:

$$g = g_{ji} \gamma_{ji} + g_{vc} \gamma_{vc} \quad (16)$$

where γ_{ji} , γ_{vc} are the weighting factors for the output current cost function, and for the imbalance capacitor voltages cost function, respectively.

To describe the calculation process, used for the control algorithm implemented, a flow chart is presented in Fig. 3. In this graphic representation, the whole process of selection of the optimal switching states is detailed.

IV. SIMULATION RESULTS

To evaluate the performance of the purpose dual output NPC-Type three-phase inverter with the adopted optimal predictive control, several simulation tests have been made with detailed simulation models, implemented in *MATLAB/Simulink* and using the *SimPowerSystems* library. In Table I all the parameters used in the simulation tests are shown.

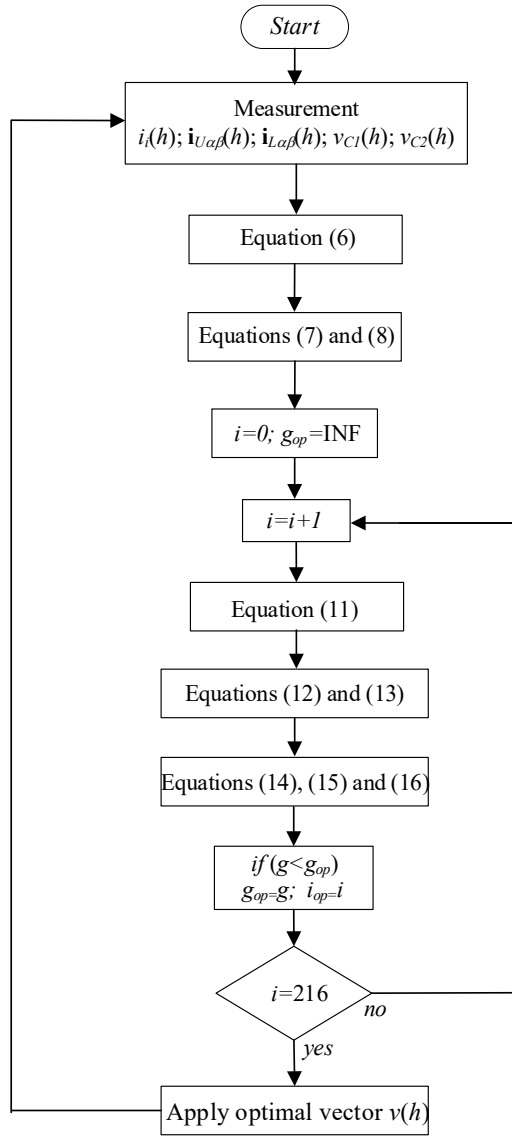


Fig. 3. Flow chart of the MPC for the NPC-Type Inverter

TABLE I. PARAMETERS OF THE SYSTEM

Input DC voltage	200 V
Capacitors C_1 and C_2	470 μ F
Load resistor per phase	0.1 Ω
Load inductor per phase	5 mH

The simulation tests for the proposed MPC were performed first in steady-state conditions and then in transient conditions, under distinct system requirements. Considering the system working in steady-state conditions. Figs. 4 and 5 show, respectively, the dual output three-phase AC load currents, when the reference peak current is equal to 30 A, and the output AC voltages applied between phase A and B of upper and lower loads.

From the results presented in Fig.4 it is seen that the AC currents are balanced with a low distortion. Moreover, it is possible to see that the currents in both outputs are matched, as required. The five line-to-line voltage levels can be seen in results from Fig. 5, in steady-state conditions. This allows to confirm the multilevel operation of this dual output converter. Another important aspect is the balance of the DC capacitors.

This can be seen in Fig. 6 where the voltage at the terminals of capacitors, C_1 and C_2 is presented. From this result, it is possible to verify that these voltages are close to the same value, the measured imbalance between the two capacitors being smaller than 0.05%.

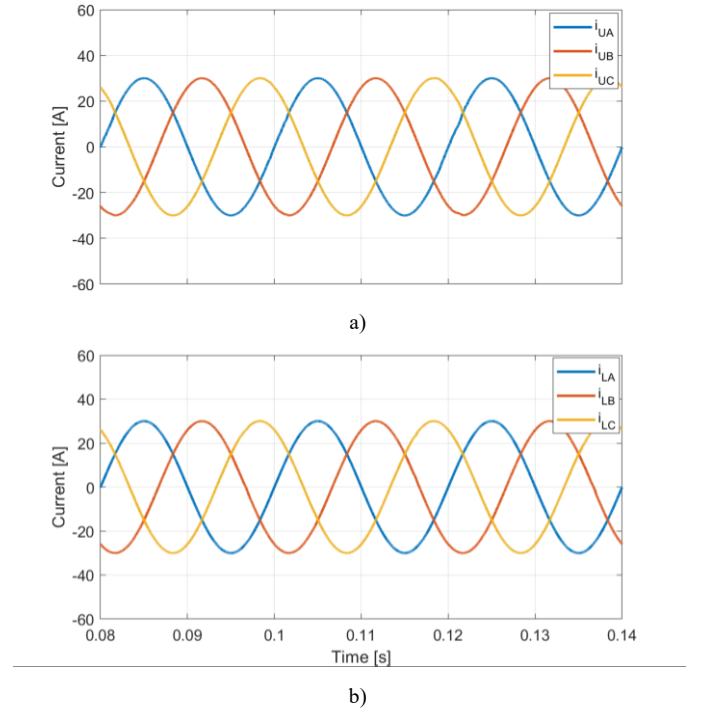


Fig. 4. Simulation results of the AC current waveforms of the dual-output NPC-Type, in steady-state condition: a) in upper output; b) in lower output.

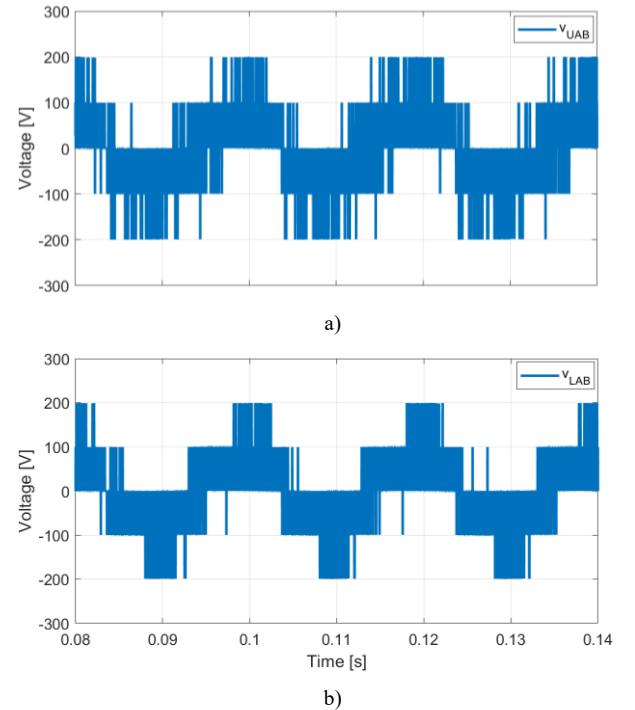


Fig. 5. Simulation results of the AC voltage waveforms (between A and B phase) of the dual-output NPC-Type converter in steady-state condition: a) in upper output; b) in lower output.

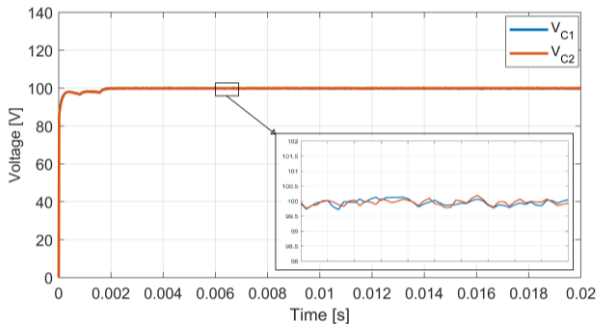


Fig. 6. Results of capacitors C_1 and C_2 voltage, in steady-state condition.

Next figures include detailed simulation results, showing different dynamic conditions based on current references transitions. To show the dynamic behavior of the proposed MPC controller for the three-phase dual output multilevel converter the current and frequency references were initially set to a 30 A and 50Hz, respectively, for both upper and lower outputs. From $t=0.14$ s up to $t=0.2$ s the relationship of current and frequency of the upper output is suddenly decreased by 40% of the initial values 30 A and 50 Hz to become 18A at 30Hz. The same variation was also applied at $t=0.2$ s, this time for the reference of the lower output currents whose references also become 18A at 30Hz. Fig. 7, shows the behavior of the three-phase dual output currents. As expected theoretically, the currents follow the respective references, presenting low distortion and maintaining balanced currents.

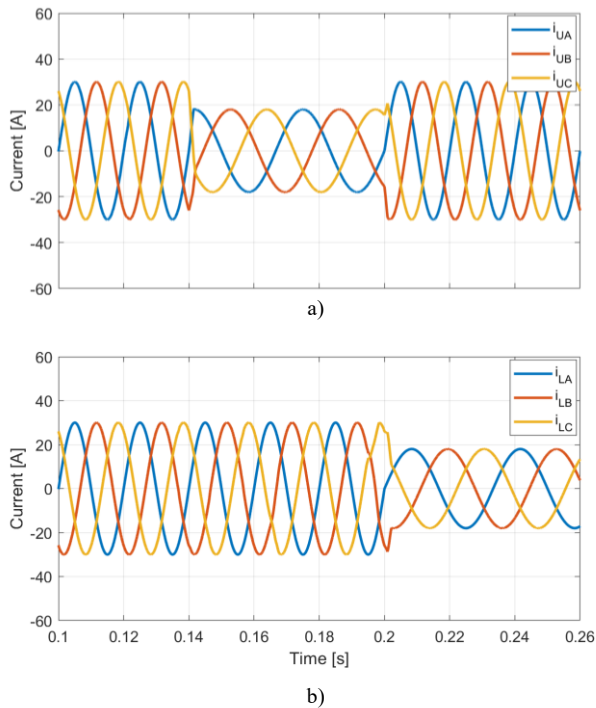


Fig. 7. Simulation results of the AC current waveforms of the dual-output NPC-Type, in transient conditions: a) in upper output; b) in lower output.

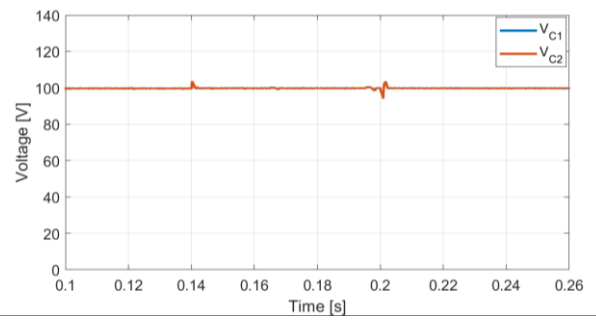


Fig. 8. Results of capacitors C_1 and C_2 voltage, in transient condition.

The balance of the DC capacitor voltages was again verified. These voltages (terminals of capacitors, C_1 and C_2) can be seen in Fig. 8 for the same reference steps ($t=0.14$ s and $t=0.2$ s). From this result it is verified that the capacitors voltages will remain stable and close to the reference values after small disturbances to the fast changing currents. The disturbances are less than 5% showing the capability of the MPC controller to also maintain the capacitor voltages at the defined references, even if the two sets of currents have distinct peak values. These previous results also show that the dynamic response of the controllers is in accordance with the MPC approach.

V. CONCLUSIONS

This paper presented a predictive control system applied to a dual-output NPC-Type three-phase three-level converter. The closed loop control system was derived from using MPC methodology with delay compensation. The MPC was developed with the purpose to independently control not only the AC currents of the dual-output converter two loads, but also to maintain the balance of the DC capacitor voltages. The proposed control strategy allowed to obtain a fast dynamic response, for AC load current control and robust control of the DC capacitor voltages of the dual converter. To design the MPC controller a cost functional of the errors between the reference and the predicted control variables was evaluated, resulting in the weighted sum of two partial cost functions. Simulation results show that the control method enforces AC currents towards their specific set point values. The proposed predictive controller also ensures the voltage balancing of the inverter DC capacitors. The results obtained in steady-state and transient conditions confirm the expected performance of the proposed control method.

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REFERENCES

- [1] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo and M. A. M. Prats, "The age of multilevel converters arrives," in *IEEE Industrial Electronics Magazine*, vol. 2, no. 2, pp. 28-39, June 2008
- [2] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications," *IEEE Transactions on Industry Applications*, vol. 41, no. 3, pp. 855-865, May-June 2005.
- [3] S. Kouro et al., "Recent Advances and Industrial Applications of Multilevel Converters," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553-2580, August 2010.
- [4] Trzynadlowski, Andrzej M. (ed.): "Power Electronic Converters and Systems: Frontiers and Applications" (Energy Engineering, 2015)

- [5] F. Blaabjerg, Y. Yang, K. Ma, X. Wang, "Power electronics - the key technology for renewable energy system integration" Int. Conf. Renewable Energy Research Appl., pp. 1618-1626, Nov. 2015.
- [6] A. Nabae, I. Takahashi and H. Akagi, "A new neutral-point-clamped PWM inverter", IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518-523, Sep./Oct. 1981.
- [7] T. A. Meynard and H. Foch, "Multi-level choppers for high voltage applications", EPE Journal, vol. 2, no. 1, pp. 45-50, March 1992.
- [8] P. W. Hammond, "A new approach to enhance power quality for medium voltage ac drives", IEEE Trans. Ind. Appl., vol. 33, no. 1, pp. 202-208, Jan./Feb. 1997.
- [9] M. Schweizer and J. W. Kolar, "Design and Implementation of a Highly Efficient Three-Level T-Type Converter for Low-Voltage Applications," in IEEE Transactions on Power Electronics, vol. 28, no. 2, pp. 899-907, February 2013.
- [10] V. F. Pires, Daniel Foito, J. F. Silva, "Fault-Tolerant Multilevel Topology Based on Three-Phase H-Bridge Inverters for Open-End Winding Induction Motor Drives", IEEE Transactions on Energy Conversion, vol. 32, Issue 3, pp. 895-902, September 2017.
- [11] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," in IEEE Transactions on Power Electronics, vol. 30, no. 1, pp. 37-53, January 2015.
- [12] D. Casadei, G. Grandi, A. Lega and C. Rossi, "Multilevel Operation and Input Power Balancing for a Dual Two-Level Inverter with Insulated DC Sources," in IEEE Transactions on Industry Applications, vol. 44, no. 6, pp. 1815-1824, Nov.-dec. 2008
- [13] V. F. Pires, A. Cordeiro, D. Foito and J. F. Silva, "A Multilevel Converter Topology for a STATCOM System Based on Four-Leg Two-Level Inverters and Cascaded Scott Transformers," IEEE Transactions on Power Delivery, vol. 37, no. 3, pp. 1391-1402, June 2022.
- [14] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," in IEEE Transactions on Industry Applications, vol. 41, no. 2, pp. 655-664, March-April 2005
- [15] J. Haruna and N. Hoshi, "A Novel Three-level inverter which can drive two PMSMs," 7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014), Manchester, UK, 2014, pp. 1-6, doi: 10.1049/cp.2014.0376.
- [16] T. Kominami, Y. Fujimoto, "A Novel Nine-Switch Inverter for Independent Control of Two Three-phase Loads," Industry Applications Conference, 2007, pp.2346-2350 (2007).
- [17] T. Kominami, Y. Fujimoto, "Inverter with Reduced Switching-Device Count for Independent AC Motor Control," Industrial Electronics Society 2007, pp.1559- 1564 (2007).
- [18] F. Gao, L. Zhang, D. Li, P. C. Loh, Y. Tang and H. Gao, "Optimal Pulsewidth Modulation of Nine-Switch Converter," in IEEE Transactions on Power Electronics, vol. 25, no. 9, pp. 2331-2343, Sept. 2010, doi: 10.1109/TPEL.2010.2047733.
- [19] R. Wang, L. Ai and C. Liu, "A Novel Three-Phase Dual-Output Neutral-Point-Clamped Three-Level Inverter," in IEEE Transactions on Power Electronics, vol. 36, no. 7, pp. 7576-7586, July 2021, doi: 10.1109/TPEL.2020.3032124.
- [20] S. M. Dabour, A. S. Abdel-Khalik, S. Ahmed and A. Massoud, "An Optimal PWM Technique for Dual-Output Nine-Switch Boost Inverters With Minimum Passive Component Count," in IEEE Transactions on Power Electronics, vol. 36, no. 1, pp. 1065-1079, Jan. 2021, doi: 10.1109/TPEL.2020.3001372.
- [21] S. Bayhan, H. Abu-Rub, R. S. Balog, "Model Predictive Control of Quasi-Z-Source Four-Leg Inverter," IEEE Transactions on Industrial Electronics, vol. 63, no. 7, pp. 4506-4516, July 2016.
- [22] S. Bayhan, M. Trabelsi, H. Abu-Rub, M. Malinowski, "Finite-Control-Set Model-Predictive Control for a Quasi-Z-Source Four-Leg Inverter Under Unbalanced Load Condition," IEEE Transactions on Industrial Electronics, vol. 64, no. 4, pp. 2560-2569, April 2017.
- [23] J. Monteiro, V. F. Pires, J. F. Silva and S. Pinto, "Multilevel Bipolar Back-to-Back HVDC Transmission System Based on the Dual Inverter Converter Structure with Model Predictive Control," IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society, pp. 1-6, October 2022.
- [24] S. Bayhan, P. Kakosimos, H. Abu-Rub, J. Rodriguez, "Finite-Control-Set Model-Predictive Control for a Quasi-Z-Source Four-Leg Inverter Under Unbalanced Load Condition," 42nd Annual Conference of the IEEE Industrial Electronics Society, pp. 5971-5976, Oct. 2016.
- [25] J. Monteiro, V. F. Pires, J. F. Silva and S. Pinto, "A Model Predictive Controller for a Buck-Boost Rectifier of an Electric Vehicle Integrated Battery Charger with a Dual-Inverter Drive," 2022 IEEE 8th International Conference on Energy Smart Systems (ESS), pp. 258-263, October 2022.
- [26] S. Vazquez, J. Leon, L. Franquelo, J. Rodriguez, H. Young, A. Marquez, P. Zanchetta, "Model Predictive Control: A Review of Its Applications in Power Electronics," IEEE Ind. Electron. Mag., vol. 8, no. 1, pp. 16-31, Mar. 2014.
- [27] M. Rivera, V. Yaramasu, A. Llor, J. Rodriguez, B. Wu, M. Fadel, "Digital predictive current control of a three-phase four-leg inverter," IEEE Trans. Ind. Electron., vol. 60, no. 11, pp. 4903-4912, Nov. 2013.
- [28] J. Monteiro, V. F. Pires, J. F. Silva, "A Model Predictive Control for the T-Type qZS Inverter with Capacitor Imbalance Compensation", 45th Annual Conference of the IEEE Industrial Electronics Society, pp. 4575-4580, 2019.
- [29] J. D. Barros and J. F. Silva, "Multilevel Optimal Predictive Dynamic Voltage Restorer," in IEEE Transactions on Industrial Electronics, vol. 57, no. 8, pp. 2747-2760, Aug. 2010, doi: 10.1109/TIE.2009.2034172.