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Photo-Induced Instability of Nanocrystalline Silicon TFTs

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***Abstract*—We examine the instability behavior of nanocrystalline silicon (nc-Si) thin-film transistors (TFTs) in the presence of electrical and optical stress. The change in threshold voltage and sub-threshold slope is more significant under combined bias-and-light stress when compared to bias stress alone. The threshold voltage shift (ΔV_T) after 6 h of bias stress is about 7 times larger in the case with illumination than in the dark. Under bias stress alone, the primary instability mechanism is charge trapping at the semiconductor/insulator interface. In contrast, under combined bias-and-light stress, the prevailing mechanism appears to be the creation of defect states in the channel, and believed to take place in the amorphous phase, where the increase in the electron density induced by electrical bias enhances the non-radiative recombination of photo-excited electron-hole pairs. The results reported here are consistent with observations of photo-induced efficiency degradation in solar cells.**

***Index Terms*—Nanocrystalline silicon (nc-Si:H), photo-induced instability, thin-film transistors (TFTs).**

I. Introduction

ALTHOUGH amorphous silicon (a-Si:H) is widely used as a channel material in thin-film transistors (TFTs) [1], it has a number of drawbacks such as poor electrical stability and low field-effect mobility. While these naturally restrict its use in new application areas, the newly emerging nanocrystalline silicon (nc-Si:H) technology offers superior material attributes and yet maintains the economic advantages of a-Si:H technology. Furthermore, nc-Si:H can be deposited at low temperature on low cost, lightweight and flexible substrates. More importantly, it has more than an order of magnitude higher field-effect mobility compared to a-Si:H [2], and its dark electrical stability has been reported to be much better than a-Si:H [3], [4] due to the absence of defect state creation in the material [4], [5]. But in applications, such as active-matrix organic light-emitting diode (AMOLED) displays or digital projectors, the nc-Si:H TFT may be subjected to extended light exposure. While the effect of light exposure on the stability of nc-Si:H thin films and solar cells has been reported [6], [7], its effect on TFTs has not been studied hitherto. This constitutes the primary focus of the present work.

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II. Measurement Procedure

We consider bottom-gated nc-Si:H TFTs in a back channel passivated configuration (see inset of Fig. 1 for the device cross section). A detailed description of the fabrication process has been reported elsewhere [8]. A Keithley SCS-4200 semiconductor characterization system was used for the electrical stressing and measurements. Long-term bias-stress measurements were performed at $V_{\rm G} = V_{\rm D} = 15$ V. At every 30 min intervals, the bias-stress was interrupted to sample the transfer characteristics of the TFT for device parameter extraction. A broad spectrum halogen lamp was used for light exposure. The light intensity was 30 mW/cm^2 on the sample surface, as measured with a silicon photodiode detector.

As-deposited TFT had threshold voltage ($V_{\rm T}$) of 2.3 $\pm$ 0.05 V, sub-threshold slope (S) of 0.44 $\pm$ 0.04 V/dec and field effect mobility of 0.4 cm^2/V $\cdot$ s at 15 V. Three different stress experiments were performed on the nc-Si:H TFT, namely, bias-only, light-only, and combined bias-and-light stress. Before every experiment, the TFTs were annealed to the pre-stress conditions in order to avoid any residual stress effect. This was confirmed by measuring transfer characteristics after every annealing. Threshold voltage shift ($\Delta V_{\rm T}$) in all instances is defined as $V_{\rm T} - V_{\rm T0}$, where $V_{\rm T0}$ is 2.3 V (i.e., pre-stress level), unless specified otherwise.

III. Results and Discussion

The shift in the threshold voltage as a function of stress duration under different stressing conditions is shown in Fig. 1. Under gate bias stress alone, the threshold voltage initially increases and then stabilizes with stress duration, and is consistent with results reported earlier [4], [5]. However, under light exposure, the time dependence of $\Delta V_{\rm T}$ is substantially different. The threshold voltage initially decreases under light stress, albeit gradually, before stabilizing at -0.2 V. In addition, we observed a persistent photo-current (PPC) after removal of light stress that is believed to be caused by hole trapping at/near the nc-Si/SiN$_x$ interface. This hole-trapping effect can also account for the negative $\Delta V_{\rm T}$ observed. There was no noticeable change in the sub-threshold slope (S) in both (bias or light stress) measurements indicating an absence of defect state creation; this is supported by the fact that the behavior of drain current in

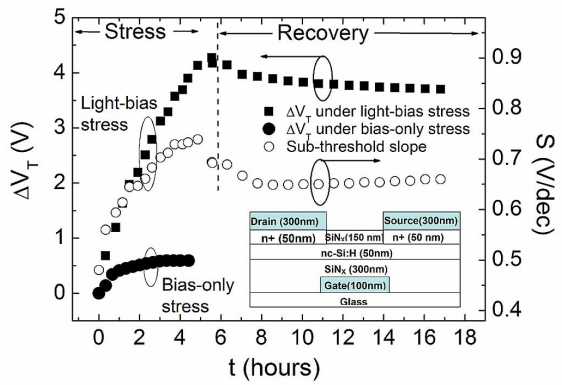

Fig. 1. Threshold voltage shift and sub-threshold slope of nc-Si:H TFTs as a function of time during concurrent bias-and-light stress (6 hours) and after stress removal in the recovery (12 hours) phase. Also shown is the shift in $V_{\rm T}$ under gate bias stress alone. Inset shows the schematic cross section of the device.

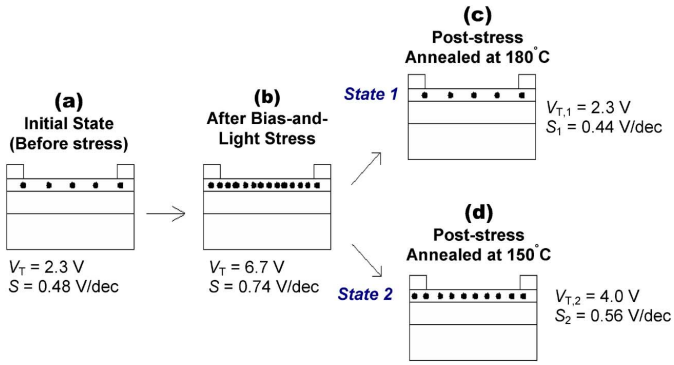

Fig. 2. Illustration of the state of TFT throughout different phases of the stress experiment, where solid circles represent the relative density of defect states. TFTs in (a) initial state are subjected to 6 hours of bias-and-light which increases (b) the defect density. The devices are subsequently annealed for 6 hours at (c) 180°C and (d) 150°C, which provokes different rates of recovery of the defect state density.

the sub-threshold regime is proportional to the density of defect states [9].

The nc-Si:H TFTs were subjected to combined bias-and-light stress for 6 hours, and then followed by a recovery period in which both bias and light stress were removed (see Fig. 1). The recovery of the TFT was monitored by sampling its transfer characteristics for a period of 12 h. During the combined bias-and-light stressing period, the increase in $V_{\rm T}$ and S is very pronounced (as shown in Fig. 1) when compared to that under independent bias or light stress. The change in $\Delta V_{\rm T}$ after 6 h of bias stress is nearly 7 times higher in the case with illumination than in the dark (Fig. 1). During the recovery phase, there is an initial decay before $\Delta V_{\rm T}$ and sub-threshold slope saturate to 3.7 V and 0.66 V/dec, respectively. The recovery could be explained by charge detrapping from gate dielectric or the relaxation of defect states created in the channel, where the former tends to occur at a faster rate. It has been reported that the characteristic time of charge detrapping for nc-Si:H TFTs after stress in the dark is several days [4], [5]. As observed in Fig. 1, there is an initial recovery of $\Delta V_{\rm T}$ by 15% within a 12-h post-stress period, which can be attributed to charge detrapping. Most of the remaining $\Delta V_{\rm T}$ is believed to be linked to stress-induced creation of defect states. In addition, there is an increase in S and it appears to be correlated with $\Delta V_{\rm T}$, suggesting that creation of defect states in the channel and at the interface could be the main mechanism of instability due to the combined bias-and-light stress. This can be further substantiated if we consider the recovery time of $\Delta V_{\rm T}$ displayed in Fig. 1. The relaxation of the created defect states follows a stretched exponential model [10]

$$\Delta V_{\rm T} = \Delta V_{\rm T0} \exp\left(-\left(\frac{t}{\tau}\right)^{\beta}\right) \tag{1}$$

where $\Delta V_{\rm T0}$ is the initial $V_{\rm T}$ shift, τ is the relaxation constant and β is the stretching exponent. Using the common values for bottom gate nc-Si TFTs, $\tau = 5{\cdot}10^6$ s and $\beta = 0.45$ [10], [11], a 90% recovery of the threshold voltage would take about a year, thus supporting the argument that defect generation is dominant in our case.

To verify the prevalence of defect state creation, the TFTs that were subjected to bias-and-light stress were subsequently annealed at 180 °C and at 150 °C for 6 h in air. No impurities are expected to be introduced due to the SiN_x passivation layer. After annealing at 180 °C, the sub-threshold slope and $V_{\rm T}$ returned to their pre-stress values ($V_{\rm T,1} = 2.3$ V, $S_1 = 0.44$ V/dec), indicating a removal of the excess stress-induced defect states and trapped charges. In contrast, the sample annealed at 150 °C exhibits V_T and a sub-threshold slope of ($V_{T,2} = 4.0$ V, $S_2 = 0.56$ V/dec), which is slightly larger than its pre-stress value, indicating the excess defect states were only partially removed in this case. Fig. 2 provides an illustration of the state of the TFT before stress, after bias-and-light stress, and after annealing at 180 °C (State 1) and at 150 °C (State 2). The different TFT recovery behavior (State 1 versus State 2) observed at the different annealing temperatures (180 °C versus 150 °C), in particular the change in S, suggests that there is a different defect density upon different annealing conditions, as S is related to the defect density [9].

To seek further insight on the defect state creation argument, the TFTs, annealed at 180 °C (State 1) and at 150 °C (State 2), were then bias stressed in the dark with $V_{\rm G} = V_D = 15$ V. Fig. 3 shows that the variation of $\Delta V_{\rm T}$ with time. Here $V_{\rm T} - V_{\rm T0}$ for the TFT annealed at 150 °C was defined using $V_{T0} = 4.0$ V. The trend of $\Delta V_{\rm T}$ versus time is similar in both State 1 and State 2, indicating that only charge trapping is taking place in both cases (as consistent with previous observation in Fig. 1 and in [4]). The minor discrepancy in $\Delta V_{\rm T}$ between the 180°C and 150°C annealed samples (see Fig. 3) is solely due to a difference in the stress conditions; the effective bias stress $(V_{\rm G} - V_{\rm T0})$ is 12.6 and 10.9 V, respectively.

While S remains constant with stress time in both cases (see Fig. 3), the magnitude is different, reflecting a difference in the defect density. It was observed that the trend in $\Delta V_{\rm T}$ and S with bias stress is different in dark (Fig. 3) and under light (Fig. 1). This suggests that device instability under bias stress occurs through the different channels depending on the light conditions. Thus, we confirm that the instability in nc-Si:H TFTs after combined light-bias stress is due to the prevalence of defect state creation.

As illustrated by the above investigation, nc-Si:H TFTs exhibit different bias stress-induced instability behavior under illumination versus in the dark, where the former leads to a more dramatic change in threshold voltage shift and in sub-threshold slope. Here, we attempt to understand the observed instability behavior by considering charge transport

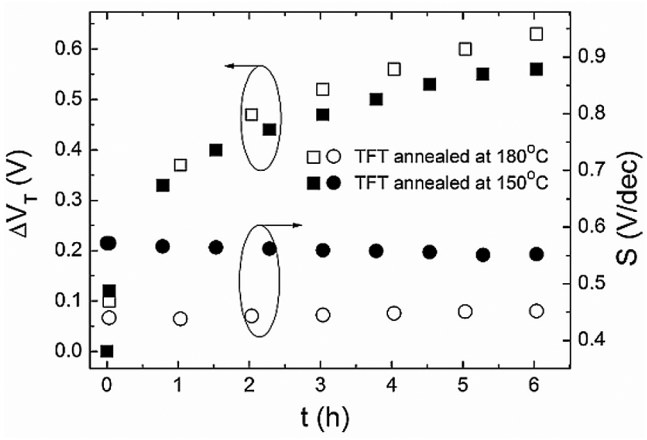

Fig. 3. Evolution of threshold voltage shift and sub-threshold slope with stress time for nc-Si:H TFT samples upon bias-stress in the dark, where these TFTs were previously subjected to 6 hours of bias-and-light stress followed by annealing at 180 °C (State 1, hollow symbols) and 150 °C (State 2, filled symbols). In both cases, $V_{\rm D}$ is 15 V, while $(V_{\rm G} - V_{\rm T0})$ for State 1 and State 2 is 12.6 and 10.9 V, respectively.

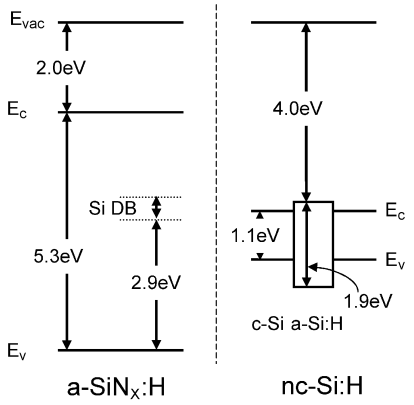

Fig. 4. Energy band diagrams for silicon nitride and nanocrystalline silicon indicating crystallites (c-Si) embedded in an amorphous (a-Si:H) matrix. Here, DB refers to dangling bonds.

mechanisms in nc-Si:H TFTs. First, recall that nc-Si:H can be generally described as composing of small grains of crystalline silicon (c-Si) embedded in an amorphous phase (a-Si:H), thus the band energy diagram of nc-Si:H can be roughly represented as a combination of two phases (c-Si and a-Si) as shown in Fig. 4. It has been reported that the dominant charge transport mechanism in nc-Si:H TFTs in the dark or under weak illumination conditions is tunnelling through the barriers between the nano-crystallite (c-Si) phases, where the band tails states in the a-Si:H grain boundaries do not participate in the conduction [2], [12]. Consequently, the bias-induced instability of nc-Si:H TFTs (in dark) stems mainly from charge trapping in the a-SiN$_x$:H gate dielectric, likely due to the tunnelling of gate-field-dependent carriers from the nano-crystallites in nc-Si:H film into the defect states created by Si dangling bonds (DBs) in the a-SiN$_x$:H gate dielectric, as illustrated in Fig. 4. Thus, the instability of these TFTs are determined largely by the composition of the a-SiN$_x$:H gate dielectric (e.g., nitrogen-rich versus silicon-rich nitride) which influences the density of Si dangling bonds in the gate dielectric layer [4].

In contrast, the observed bias-stress instability under illumination (i.e., combined bias-and-light stress) is believed to stem from the a-Si:H matrix, in which a high concentration of excess electron–hole pairs is photo-generated. The high electron density favors bimolecular recombination with nearby holes [13], which has been shown to create dangling bonds (distribution of deep states in the bandgap) in the amorphous phase [14]. This can also explain the increase in sub-threshold slope after the combined bias-and-light stress. These results are consistent with the findings reported for the instability observed in the nc-Si:H solar cells [15].

IV. Conclusion

We have shown that nc-Si:H TFTs exhibit different bias-stress-induced instability when under illumination and in the dark. The changes in threshold voltage and sub-threshold slope are more significant under combined bias-and-light stress when compared to bias-stress alone. Under illumination, the prevailing bias stress induced instability mechanism appears to be the creation of defect states in the channel, which takes place in the amorphous phase where the increase in the electron density induced by electrical bias enhances the non-radiative recombination of photo-excited electron-hole pairs. In contrast, the TFTs are relatively more stable upon bias-stress in the dark, and the primary instability mechanism is related to charge trapping at the semiconductor/insulator interface.

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