**INSTITUTO SUPERIOR DE ENGENHARIA DE LISBOA**

**Departamento de Engenharia Eletrotécnica de Energia e Automação**

# Three-Winding Transformer with DC Microgrid and Active Power Filter

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## DEDICATÓRIA

Ao meu querido avô,

Joaquim Nunes (*in memoriam*)

## ABSTRACT

This thesis takes a different approach to the classic distribution transformer topology. These transformers usually contain only two windings (input and output) and, for this reason, the addition of DC microgrids onto them requires additional planning and designing. This work aims to create a device in which a DC microgrid can be seamlessly integrated into the system.

This device would be composed by two main components:

- A three-winding transformer – instead of the classical two-winding transformer used in typical distribution transformers.
- A bi-directional AC/DC converter which function is to interface between the DC microgrid and the transformer.

The idea is that both primary and secondary windings of the transformer work as commonly known in a distribution transformer – power flows from the grid to the loads – while the terciary winding interconnects the AC/DC converter to the system.

As mentioned above, the converter is bi-directional which means it can direct the power to the system itself (e.g.: vehicle-to-X topology) or to the DC microgrid (e.g.. charging an electric vehicle).

Furthermore, the converter is also capable of working as an active power filter, softening the reactive power and harmonic content present in the grid, which is generated by the loads.



## KEYWORDS

DC microgrid, Three-Winding Transformer, Active power filter, SVPWM

## RESUMO

Esta tese procura estudar uma nova arquitetura para postos de transformação. Estes são, na grande maioria dos casos, constituídos por transformadores de apenas dois enrolamentos (entrada e saída) e, por essa razão, a implementação de microrredes DC requere planeamento e dimensionamento extra. Este trabalho procura criar um dispositivo que facilite a interligação de postos de transformação com microrredes DC.

Este dispositivo é composto por dois componentes principais:

- Um transformador de três enrolamentos – em vez do transformador de dois enrolamentos clássico, usualmente usado nos postos de transformação;
- Um conversor AC/DC bidirecional que interliga a microrrede DC com o transformador.

A ideia é que tanto o primário, como o secundário do transformador estão ligados como normalmente encontrado nos postos de transformação – a potência flui da rede para a carga – enquanto o terciário está ligado a ao conversor AC/DC (microrrede).

Como referido anteriormente, o conversor é bidirecional o que significa que este pode direcionar a potência para o sistema (e.g.: veículo-para-X) ou para o microrrede (e.g.: carregamento de um veículo elétrico).

Adicionalmente, o conversor também funciona como filtro ativo de potência, suavizando a potência reativa e o conteúdo harmónico presente na rede, gerado pelas cargas.



## KEYWORDS

Microrrede DC, Transformador de Três Enrolamentos, Filtro Ativo de Potência, SVPWM

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## SIMBOLOGY

| | |
|---|---|
| $a_0$ | Fourier coefficient of the DC component |
| $a_n; b_n$ | Fourier coefficients of the n$^{th}$ harmonic |
| $C_u(s); C_i(s)$ | Transfer function of the voltage and current controllers |
| $\mathbf{C_{\alpha\beta}}$ | Concordia matrix |
| $\mathbf{C_{dq}}$ | Park matrix |
| C | Capacitance [F] |
| $D$ | Deformed power [VAr] |
| $f_1; f_2; f_3$ | Gate signals for the converter |
| $f_c$ | Switching frequency [Hz] |
| $f_d; f_q$ | Approximation of the gate signals of the converter in dq coordinates |
| $\mathbf{i_{\alpha\beta}}$ | Current vector in αβ coordinates |
| $\mathbf{i_{123}}$ | Current vector in 123 coordinates |
| $i_{G_1}; i_{G_2}; i_{G_3}$ | Grid currents in 123 coordinates [A] |
| $i_{C_1}; i_{C_2}; i_{C_3}$ | Converter currents in 123 coordinates [A] |
| $i_{C_d}; i_{C_q}$ | Converter currents in dq coordinates [A] |
| $i_c$ | DC microgrid's capacitor current [A] |
| $i_o$ | Microgrid's current [A] |
| $i_{dc}$ | Microgrid's DC current injected/consumed in/by the AC side of the converter [A] |
| $\mathbf{i_{dq}}$ | Current vector in dq coordinates |
| $i_{L_1}; i_{L_2}; i_{L_3}$ | Loads currents in 123 coordinates [A] |
| $i_{L_d}; i_{L_q}$ | Loads currents in dq coordinates [A] |
| $i_{d_{ref}}$ | Reference current's direct component [A] |
| $k_p; k_i$ | Control loop's proportional and integral gains |

| | |
|---|---|
| $\overline{I_d}; \overline{I_q}$ | Continuous components of the currents in the dq reference frame [A] |
| $\widetilde{I_d}; \widetilde{I_q}$ | Alternating components of the currents in the dq reference frame [A] |
| $L$ | Inductance [H] |
| $m$ | Module of the reference vector of the voltage applied by the converter |
| $mag$ | Magnitude of the module of the reference vector of the voltage applied by the converter |
| $OLTF_i; CLTF_i$ | Open and closed loop transfer functions of the current control loop |
| $OLTF_u; CLTF_u$ | Open and closed loop transfer functions of the voltage control loop |
| $OLTF_i; CLTF_i$ | Open and closed loop transfer functions of the current control loop |
| $P$ | Active power [W] |
| $p$ | Instantaneous active power [W] |
| $Q$ | Reactive power [VAr] |
| $q$ | Instantaneous reactive power [VAr] |
| $R$ | Resistance [Ω] |
| $r$ | Ratio between the primary winding and the secondary and tertiary winding of the three-winding transformer |
| $S$ | Apparent Power [VA] |
| $S(t)$ | Temporal function |
| $S_{n_{RMS}}$ | RMS value of the n$^{th}$ harmonic |
| $S_{RMS}$ | Total RMS value of a sinusoidal signal and its harmonic components |
| $T_1; T'_1; T_2; T'_2; T_3; T'_3$ | Gate signals for the converter |
| $T_d; T_u$ | Statistic delays [s] |
| $u_{G_1}; u_{G_2}; u_{G_3}$ | Grid voltages in 123 coordinates [V] |
| $U_{d_{ref}}; U_{q_{ref}}$ | Reference voltages for the converter to apply, in the dq reference frame [V] |
| $U_{dc}$ | Microgrid's DC voltage [V] |
| $U_{dc_{ref}}$ | Microgrid's DC voltage's setpoint for the controller [V] |

| | |
|---|---|
| $u_k$ | Instantaneous phase to neutral voltage of the $k^{th}$ phase [V] |
| $V_1; V_2; V_3; V_4;$ $V_5; V_6; V_7; V_8$ | SVPWM's space vectors |
| $\mathbf{W}$ | Auxiliary matrix used in Park transformation of the converter mathematical model |
| $\mathbf{X_{\alpha\beta}}$ | State vector in αβ coordinates |
| $\mathbf{X_{123}}$ | State vector in 123 coordinates |
| $\mathbf{X_{dq}}$ | State vector in dq coordinates |
| $\mathbf{R/L_{123}}$ | State matrix in 123 coordinates |
| $\mathbf{1/L_{\alpha\beta}}$ | Input matrix in αβ coordinates |
| $\mathbf{1/L_{123}}$ | Input matrix in 123 coordinates |
| $\mathbf{1/L_{dq}}$ | Input matrix in dq coordinates |
| $\mathbf{R/L}_{\alpha\beta}$ | State matrix in αβ coordinates |
| $\mathbf{R/L_{dq}}$ | State matrix in dq coordinates |
| $\theta_G$ | Angle of the grid's voltages in the αβ plane [rad] |
| $\theta_C$ | Angle of the converter's currents in the αβ plane [rad] |
| $\xi$ | Damping factor |
| $\omega_n$ | Control loop's natural frequency [rad/s] |

## ABBREVIATIONS

AC – Alternated Current

APF – Active Power Filter

CLTF – Closed Loop Transfer Function

DC – Direct Current

DC/AC – Transformation from direct current to alternated current or vice-versa.

dq – Direct-Quadrature reference plane

OLTF – Open Loop Transfer Function

MCU – Microcontroller Unit

PF – Power Factor

RL – Resistive and Inductive

SAF – Shunt Active Filter

THD – Total Harmonic Distortion

TDD – Total Demand Distortion

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# Chapter 1

# Introduction

## 1.1 – Background and motivation

In modern electrical power systems, the efficient distribution and utilization of energy play a pivotal role in ensuring reliability, sustainability, and optimal performance. Transformers are indispensable components within these systems, facilitating the transmission of electricity across different voltage levels. Among the various transformer configurations, the three-winding transformer has gained significance due to its ability to interconnect multiple voltage levels within a single unit. This capability becomes particularly relevant when dealing with complex power distribution scenarios such as those found in microgrids.

Microgrids, as localized energy distribution networks, have garnered attention as innovative solutions to address challenges posed by the integration of renewable energy sources and the need for improved power quality. Unlike conventional AC grids, DC microgrids offer advantages such as higher efficiency, reduced losses, and greater flexibility in incorporating renewable resources.

Furthermore, the integration of renewable energy sources, such as solar and wind, while environmentally advantageous, introduces variability and intermittency into power generation. This integration, along with the proliferation of non-linear loads, have raised concerns about power quality [1]. Non-linear loads introduce harmonics and reactive power injection into the grid, leading to power quality degradation. The adverse effects range from equipment malfunctions to increased energy losses and reduced system efficiency.

Active Power Pilters (APFs) have emerged as a powerful solution to mitigate power quality issues. APFs are dynamic devices that monitor the grid's current waveform and inject compensating currents to eliminate harmonics, correct power factor imbalances, and maintain voltage stability. Through advanced control algorithms and rapid response capabilities, APFs can significantly improve the quality of electrical power distribution, thereby enhancing the reliability and performance of both local microgrids and larger interconnected networks.

While the potential of active power filters is widely recognized, the integration of DC microgrids in distribution grids using three-winding transformers has not been extensively explored. The synergies between these technologies, such as coordinated control strategies and load sharing mechanisms, remain relatively unknown. The literature demonstrates a clear gap in understanding the interactions between these three subjects. By addressing this gap, this research aims to drive advancements in both power quality management and the effective integration of renewable energy in modern power distribution systems.

This dissertation aims to address this gap by interconnecting an AC distribution grid and a DC microgrid using a three-winding transformer. The DC microgrid is connected to the AC system by a bi-directional DC/AC power converter which also functions as an active power filter. By doing so, relevant data can be taken from the synergy of these systems.

## 1.2 – Objectives

The objective of this thesis is to assemble, in a laboratory, a three winding transformer connecting the grid – with a stepped down voltage of up to 100 $V_{RMS}$ with a series of loads and a DC microgrid which doubles as an active power filter.

For the completion of this, it is necessary:

a) To model the power converter and the power quality compensation system.

b) To numerically simulate the system to assemble.

c) To implement the obtained control algorithms in a microprocessor.

d) Validate experimentally, the results obtained in the simulation.

## 1.3 – Thesis' structure

This thesis is structured into six chapters which include this introduction.

In the second chapter, a review of the literature is made where it is highlighted the current usage of DC microgrids and three-winding transformers as well as the current state of power quality.

The third chapter is dedicated to the study of the active power filter where the current architectures to integrate APFs in power systems are reviewed and the dynamic models in 123,

αβ and dq coordinates of the converter are deduced. It is also explained how the reference currents for the converter are obtained, followed by the control loops design for both the DC voltage and the converter currents. After this, the switching algorithm, SVPWM, is described.

In the fourth chapter, the numerical simulation in MATLAB/Simulink is described and the results obtained from the simulation are presented and commented on.

The fifth chapter is dedicated to the experimental work done in the laboratory. Starting with referencing the hardware used and going on to the results obtained from the experiments conducted.

The sixth chapter presents the final conclusions of these work as well as some improvements that can be implemented to the work done.

# Chapter 2

# Literature Review

## 2.1 – DC microgrid

Semiconductor-based transistors, which are the building blocks of most consumer electronics, require DC power to function. Meanwhile, the shift towards sustainability has resulted in the widespread adoption of renewable energy sources, such as photovoltaics and fuel cells, that produce DC power. However, the current electrical power distribution infrastructure is based on AC power, so direct utilization of these renewable energy sources is not possible without incurring efficiency losses due to the DC-AC conversion.

To overcome this mismatch, power converters are commonly used to convert AC power from outlets to DC power loads. This is achieved through rectifiers, which are typically built into consumer electronics. However, this conversion process is not without its drawbacks. A study conducted by the Lawrence Berkeley National Laboratory found that the average loss in external power supplies was 32% [2], highlighting the impact of this conversion process on overall energy efficiency.

Since no adequate means of energy transportation currently exist within the grid, ideally, electricity is simultaneously produced and consumed. To accommodate the power demands of modern technology and the increased utilization of DC generation, the DC microgrid provides unique solutions to the present AC grid inefficiencies while simultaneously providing robust reliability without the need of phase synchronization [3].

In recent years, due to the wide utilization of direct current (DC) power sources, such as solar photovoltaic (PV), fuel cells, different DC loads, high-level integration of different energy storage systems such as batteries, supercapacitors, DC microgrids have been gaining more importance.

### 2.1.1 – Microgrids in photovoltaic power generation

DC microgrid systems are especially fit to overcome the issues associated with transmitting electricity generated from large scale photovoltaic (PV) plants to demand sites [4]. The DC microgrid system enables the integration of multiple small-scale PV units near demand sites, thereby reducing transmission losses, improving grid stability and reliability, and reducing the cost of energy storage.

The use of DC microgrid systems can help to address the economic efficiency issues associated with large scale PV plants in remote sites. By integrating multiple small-scale PV units near demand sites, the system reduces the need for large transmission and distribution systems, reducing the cost and complexity of the power transmission network. Furthermore, the ability to control the output of multiple PV units can provide grid stability and improve the reliability of the power supply [5].

While DC microgrid systems offer a promising solution for increasing the amount of photovoltaic generation, further research and development are needed to optimize the system performance and reduce costs. Additionally, standardization of the technology, interconnection standards, and regulations for DC microgrid systems are necessary to ensure widespread adoption and growth of the technology.

## 2.2 – Multiwinding winding transformer

Multiple winding transformers, also known as a multi-coil, or multi-winding transformer, contain more than one primary or more than one secondary coil on a common laminated core. Multi-winding transformers are beneficial when connecting three or more circuits with varying voltages. They are a more cost-effective and efficient solution compared to using multiple two-winding transformers. This is because you can use a single multi-winding transformer instead of several two-winding transformers to achieve the same result.

The way a multiple winding transformer operates is similar to that of a regular two-winding transformer. The calculation of primary and secondary voltage, current, and turns ratio remains the same [6].

## 2.2.1 – Equivalent circuit

The equivalent circuits of multi-winding transformers are more complicated than in the two-winding case because they must consider the leakage impedances associated with each pair of windings. Typically, in these equivalent circuits, all quantities are referred to a common base, either by use of the appropriate turns ratios as referring factors or by expressing all quantities in per unit. The exciting current usually is neglected [7] ($Z_0 = \infty$).

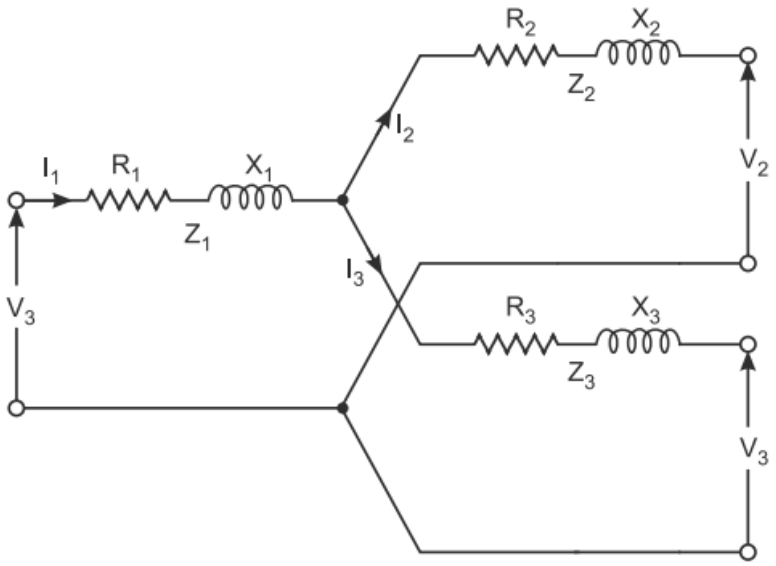



Figure 2.1 – Equivalent circuit of a three-winding transformer [8].

$Z_1$, $Z_2$, $Z_3$ are the impedances of each winding and can be determined from the data of three short-circuit tests performed on the transformer.

## 2.2.2 – Drawbacks

When using multi-winding transformers, several issues can arise that are associated with the effects of leakage impedances on voltage regulation, short-circuit currents, and the division of load among circuits [7].

The leakage impedances present in multi-winding transformers can affect voltage, leading to fluctuations in the output voltage.

Another issue is the distribution of short-circuit currents, which occur when a fault or other malfunction causes the normal flow of current to be interrupted. If leakage impedances are not

properly managed in a multi-winding transformer, the short-circuit currents can cause damage to the transformer and other components.

Finally, the division of load among circuits can also pose a challenge in multi-winding transformers. The multiple windings and their associated leakage impedances can result in unequal distribution of load, leading to imbalanced currents and reduced efficiency.

### 2.2.3 – Applications

Sometimes, Delta-connected tertiary windings are used on three-phase banks to provide a low-impedance path for third harmonic components of the exciting current to reduce third-harmonic components of the neutral voltage [7], as shown in Figure 2.2.

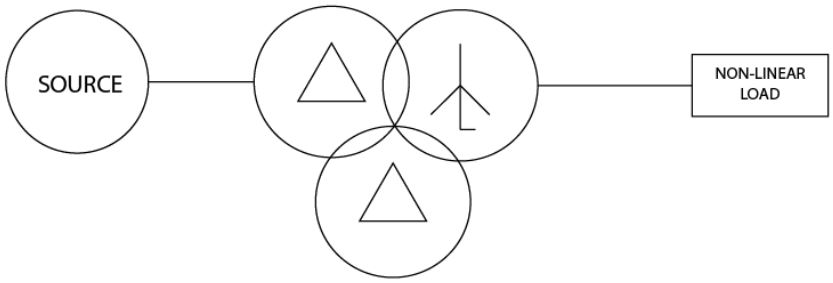



Figure 2.2 - Delta-Star-Delta transformer connection for 3rd harmonic reduction.

Distribution transformers play a crucial role in the supply of electricity for residential use. These transformers may feature two secondary windings [7], each with a specific rated voltage. The secondary windings are connected in series, providing double the voltage for high power devices. Meanwhile, the individual windings are utilized to supply domestic low-powered AC loads. This design allows for efficient and effective distribution of electricity to meet the varying power requirements of domestic settings.

Similarly, a large distribution system may be supplied through a three-phase bank of three-winding transformers from two or more transmission/generation systems having different voltages [7], as shown in Figure 2.3.

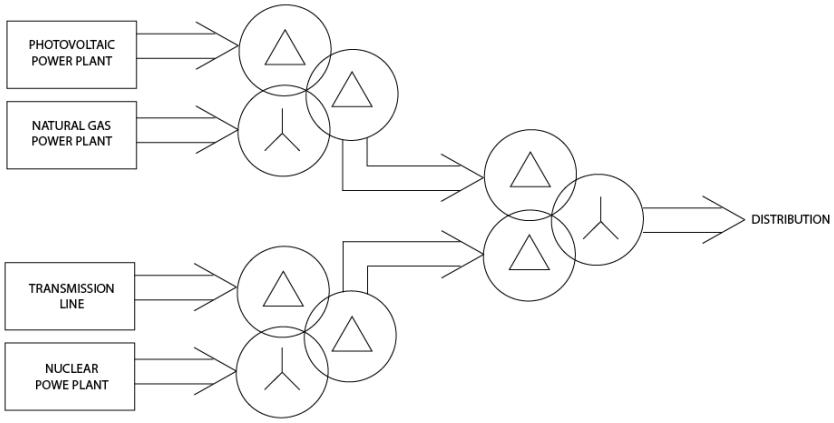



Figure 2.3 – Example of a bank of three three-winding transformers.

Furthermore, three-phase transformer banks utilized for interconnecting two transmission systems of differing voltages often incorporate a tertiary set of windings [7]. These tertiary windings serve a dual purpose, providing voltage for auxiliary power needs in substations or for the local distribution system. Additionally, static capacitors may be linked to the tertiary windings for the purpose of power factor correction or voltage regulation. This results in an enhanced and optimized power transmission system.

Transformers with a primary winding and multiple secondary windings can also be utilized in multiple-output DC power supplies for electronic applications. This type of application provides a compact solution for galvanically isolation between different loads and the grid. Additionally, three-winding transformers are commonly employed in transportation traction systems, such as in trams. Usually, the primary and secondary windings are connected in star formation and the tertiary winding is connected in delta formation (Figure 2.4).

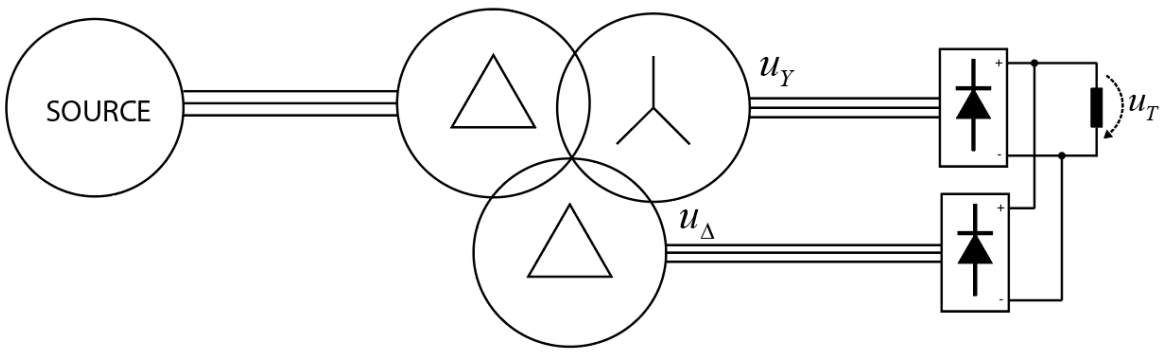



Figure 2.4 - 12-pulse rectifier.

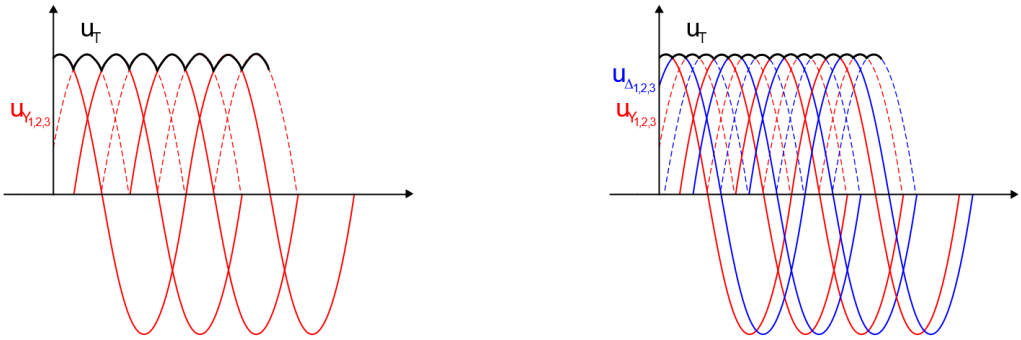



Figure 2.5 - Output voltages of a 6-pulse rectifier (a) and a 12-pulse rectifier (b).

This configuration results in two 3-phase systems, phase shifted 30º. When paired with 3-phase bridge rectifiers, this system is called 12-pulse rectifier (Figure 2.4). These systems offer a bigger pulsation index than the common 6-pulse system (Figure 2.5).

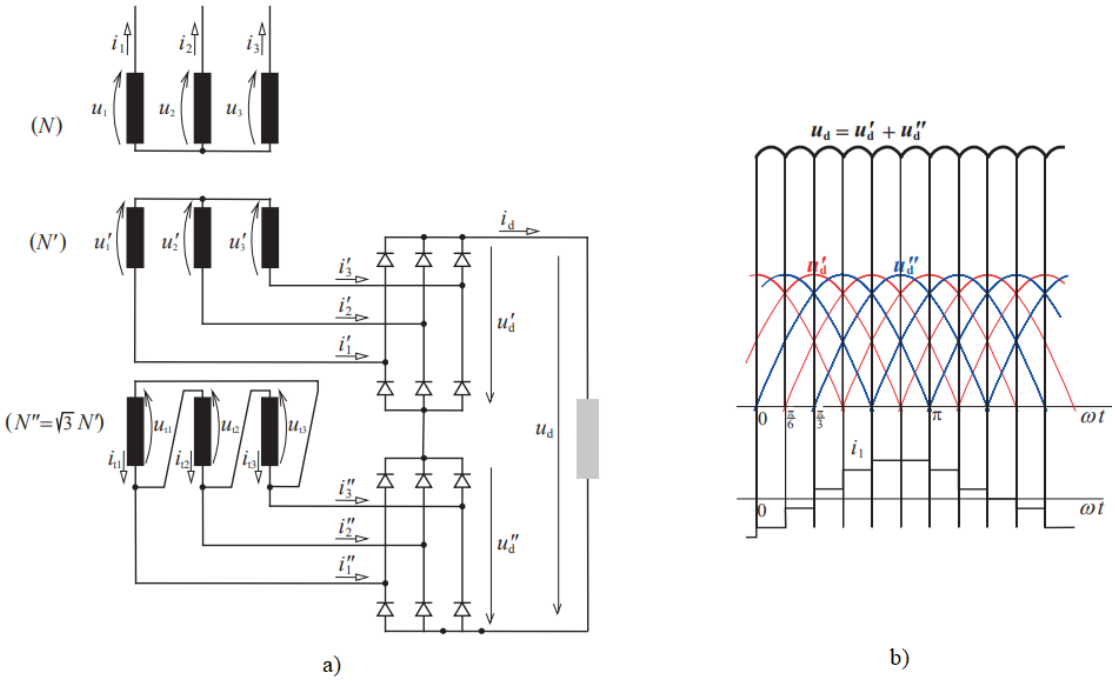



Figure 2.6 – a) Schematic of the association of a three-winding transformer and two three-phase rectifiers; b) resulting rectified voltage and current in one phase of the rectifier [9].

## 2.3 – Power quality of AC grids

Power quality's concept has evolved gradually the past 60 years. When it was first introduced, service continuity was the focus. However, voltage amplitude, frequency, phase unbalances and harmonic distortion quickly became important due to the proliferation of non-linear electronic devices.

Ideally, the grid delivers the power to its loads while maintaining its voltage and frequency between a certain interval. Under the EN 50160 standard, for voltages under 1000 V, frequency and voltage must be comprised between the intervals shown in Table 2.1.

Another standard utilized for power quality issues is the IEEE 519-2022. Among other things, this standard defines two requirements on harmonic content – an absolute maximum in voltage THD levels, and a variable maximum TDD level, as shown in

Table 2.2 and Table 2.3.

Table 2.1 - Acceptable voltage and frequency intervals under the EN 50160 standard [10].

| | |
|---|---|
| Power Frequency | Mean value of fundamental measured of ver 10s:<br>±1% deviation from nominal value for 99.5% of the week.<br>-6%/+4% deviation from nominal value for 100% of the week. |
| Voltage magnitude variations | Mean value of rms values for 10 minutes:<br>±10% deviation from nominal value for 95% of the week. |

Table 2.2 – Voltage distortion limits under the IEEE 519-2022 standard [11].

| Voltage interval | Individual harmonic (%) | THD (%) |
|---|---|---|
| ≤ 1 kV | 5.0 | 8.0 |
| 1 kV to 69 kV | 3.0 | 5.0 |
| 69 kV to 161 kV | 1.5 | 2.5 |
| ≥161 kV | 1.0 | 1.5 |

In Europe, nominal values of voltage and frequency are 230/400 V and 50 Hz, respectively.

The main problems Power Quality (PQ) faces are:

- Interruptions – grid unavailability;
- Voltage drops – mainly caused by isolation defects or large power consumption;
- Overvoltage – mainly caused by atmospheric discharge;
- Voltage flicker – mainly caused by voltage fluctuations in lighting devices;
- Phase unbalances – power is not distributed heavenly between phases;
- Harmonic distortion – mainly caused by non-linear electronic devices;

In this dissertation, current harmonic distortion, phase balancing and power factor correction are the focused subjects.

Table 2.3 – Current harmonic distortion limits under the IEEE 519-2022 standard [11]

| | Maximum THD for each harmonic order, h, interval | | | | | |
|---|---|---|---|---|---|---|
| Maximum current | $2 \leq h < 11$ | $11 \leq h < 17$ | $17 \leq h < 23$ | $23 \leq h < 35$ | $35 \leq h < 50$ | TDD |
| <20 | 4.0 | 2.0 | 1.5 | 0.6 | 0.3 | 5.0 |
| 20<50 | 7.0 | 3.5 | 2.5 | 1.0 | 0.5 | 8.0 |
| 50<100 | 10.0 | 4.5 | 4.0 | 1.5 | 0.7 | 12.0 |
| 100<1000 | 12.0 | 5.5 | 5.0 | 2.0 | 1.0 | 15.0 |
| >1000 | 15.0 | 7.0 | 6.0 | 2.5 | 1.4 | 20.0 |

## 2.3.1 – Harmonic components

For the voltage and current waveforms to follow perfect sinusoidal shapes, harmonic components induced in the grid by, for example, the switching transients in power electronic controllers should not be present [12].

Simply put, harmonics are voltages or currents which frequencies are multiples of the fundamental component and are classified by order, frequency, and sequence. The Table 2.4 depicts an example of harmonic components for a 50Hz power grid.

Table 2.4 - Harmonic classification.

| **Order** | **Fund.** | $\mathbf{2^{nd}}$ | $\mathbf{3^{rd}}$ | $\mathbf{4^{th}}$ | $\mathbf{5^{th}}$ | $\mathbf{6^{th}}$ | **…** | $\mathbf{n^{th}}$ |
|---|---|---|---|---|---|---|---|---|
| **Frequency (Hz)** | 50 | 100 | 150 | 200 | 250 | 300 | … | n x 50 |
| **Sequence** | + | – | 0 | + | – | 0 | … | … |

Sequence is related to the direction of the rotating field created by the respective harmonic relatively to the fundamental component's magnetic field. This is particularly important in induction motors since:

- harmonics with direct sequence (+) induce magnetic fields in the same direction of that of the fundamental component producing torque. These harmonics circulate between phases;
- inverse harmonics (-) induce magnetic fields in the opposite direction of that of the fundamental component producing opposing torque. These harmonics circulate between phases;
- homopolar harmonics (0) induce magnetic fields that cancel each other. These harmonics circulate between phases and neutral.

In summary, voltage unbalance in a three-phase system can cause an opposing torque, proportional to the inverse sequence voltage component. Figure 2.7 illustrates a case in which the $7^{th}$ harmonic torque can cause problem during start-up, where the characteristic torque and the braking torque curves cross.

Usually, harmonics with odd orders are more significant than those with even orders. Even order harmonics are mainly results of asymmetry caused by the presence of a DC component.

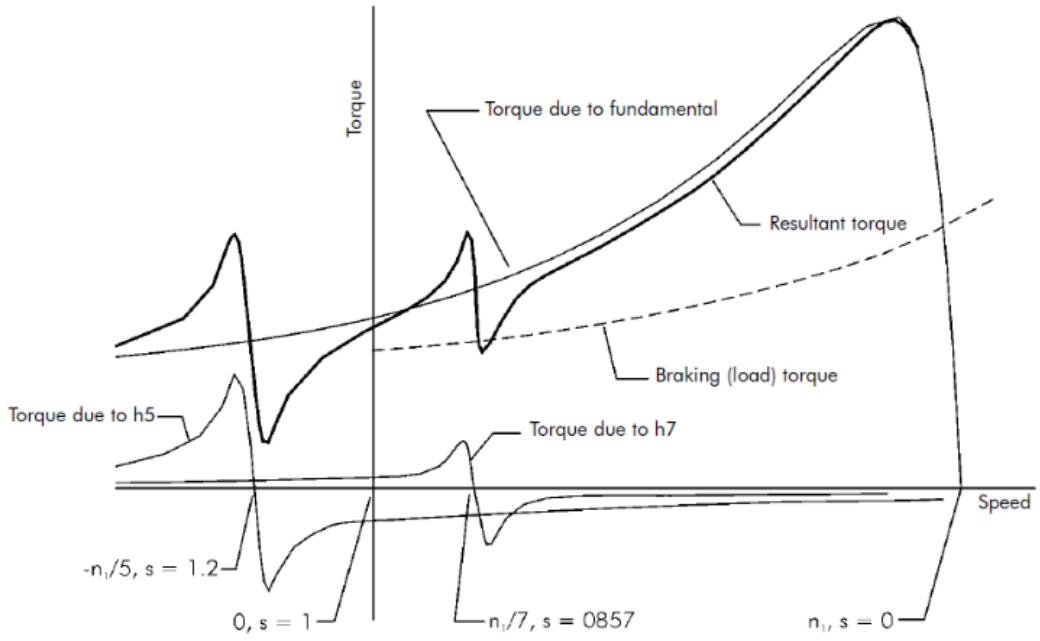



Figure 2.7 - Influence of asynchronous torque produced by harmonics on the main torque characteristic of an asynchronous motor [10].

Using the Fourier series, we can decompose currents or voltages into a summatory of sinusoidal currents or voltages which frequencies are multiples:

$$S(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(n\omega t + \varphi_n) + \sum_{n=1}^{\infty} b_n \sin(n\omega t + \varphi_n) \tag{2.1}$$

Where

$$\begin{cases} a_0 = \frac{1}{\pi}\int_{-\pi}^{\pi} S(t)d(\omega t) \\ a_n = \frac{1}{\pi}\int_{-\pi}^{\pi} S(t)\cos(n\omega t)d(\omega t) \\ b_n = \frac{1}{\pi}\int_{-\pi}^{\pi} S(t)\sin(n\omega t)d(\omega t) \end{cases} \tag{2.2}$$

The RMS values of each harmonic component are given by:

$$S_{n_{RMS}} = \frac{1}{2}\sqrt{a_n^2 + b_n^2} \tag{2.3}$$

And the total RMS value by:

$$S_{RMS} = \sqrt{\sum_{n=1}^{\infty} S_{n_{RMS}}^2} \tag{2.4}$$

To quantify harmonic distortion, Total Harmonic Distortion (THD) was introduced. THD corresponds to the fraction between RMS values of harmonic content and the RMS value of the fundamental component:

$$THD = \sqrt{\sum_{n=2}^{\infty} \frac{S_{n_{RMS}}^2}{S_{1_{RMS}}}} \tag{2.5}$$

To visualize the significance of each harmonic, we can plot the harmonic spectrum.

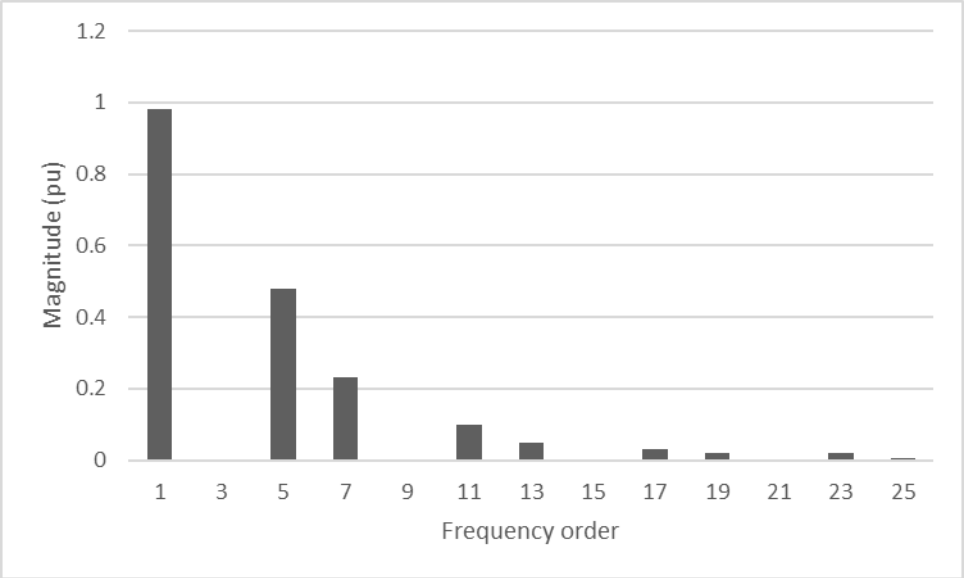



Figure 2.8 - Example of a harmonic spectrum.

The harmonic spectrum, represented in Figure 2.8, refers to the distribution of harmonic frequencies present in an alternating current waveform. In other words, it is the spectral representation of the harmonic content in a periodic waveform. The harmonic spectrum can be obtained using a Fourier analysis, which decomposes a periodic waveform into its constituent sine and cosine components. The harmonic spectrum shows the relative magnitudes of the harmonics present in the waveform and provides a mean of assessing the level of harmonic distortion in the system.

### 2.3.2 – Power factor and its correlation with harmonic distortion

Power factor is defined by the fraction between apparent power ($S$) and active power ($P$):

$$PF = \frac{P}{S} \tag{2.6}$$

For voltages which are perfectly balanced and contain no harmonic content, apparent power is the resulting vector of the summatory of the active power, reactive power ($Q$) and deformed power ($D$) vectors.

$$S = \sqrt{P^2 + Q^2 + D^2} = \sqrt{(UI\cos\phi)^2 + (UI\sin\phi)^2 + U^2\left(I_2^2 + I_3^2 + I_4^2 + ...\right)} \tag{2.7}$$

This equation can be represented in a three-axis diagram (Figure 2.9).

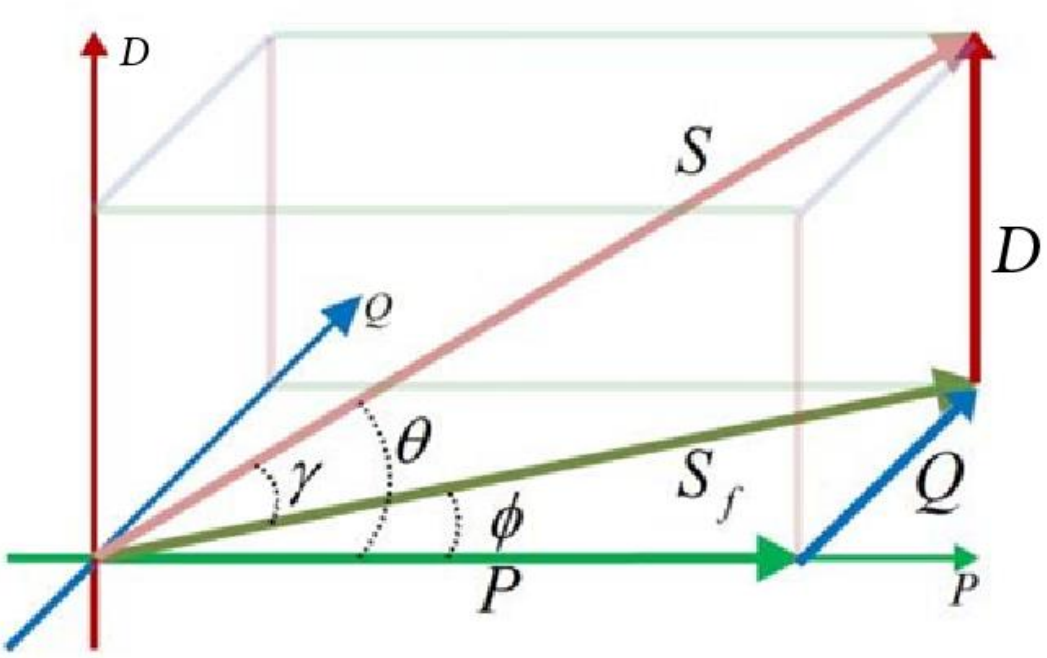



Figure 2.9 - Power tetrahedron [13].

For a power system where voltage and current follow perfect sinusoidal waves ($D$ = 0), power factor is equal to the cosine of the angle between apparent power of the fundamental component, $S_f$, and $P$ – $cos(\Phi)$. This angle represents phase shift between voltage and current.

The presence of harmonic content in the power system will increase vector $D$, causing apparent power to also increase, decreasing power factor.

# Chapter 3

# Active Power Filter – Mathematical Model and Design

## 3.1 – Introduction

In an attempt to increase power quality in electrical energy grids, passive filters were introduced. Passive filters consist of inductance, capacitance and resistance elements configured and tuned to control specific harmonic components. Although fairly simple and cheap, the passive filter inherits several downsides. The filter components can be very bulky because the harmonics that need to be suppressed are usually of low order. Furthermore, the compensation characteristics of these filters are influenced by the source impedance and, as such, the filter design is highly dependent on the power system in which it is connected to. Passive filters are also known to cause resonance, thus affecting the stability of the power system. In addition, frequency variation of the power system and tolerances in components values can affect the filtering characteristics. As the regulatory requirements become more stringent, the passive filters might not be able to meet future revisions of a particular standard and, in the worst-case scenario, it may be required a retrofit of new filters.

On the other hand, remarkable progress in power electronics has spurred interest in Active Power Filters (APF) for harmonic distortion mitigation. The basic principle of APF is to utilise power electronics technologies to produce specific currents components that cancel the harmonic currents components caused by the load. The information regarding the harmonic currents and other system variables are passed to the compensation current/voltage reference signal estimator. The compensation reference signal from the estimator drives the overall system controller. This in turn provides the control for the gating signal generator.

APFs have a number of advantages over the passive filters. First of all, they can suppress not only the supply current harmonics, but also the reactive currents. Moreover, unlike passive filters, they do not cause harmful resonances with the power distribution systems. Consequently, the APFs performances are independent on the power distribution system properties. On the other hand, APFs have some drawbacks. Active filtering is a relatively new

technology, practically less than four decades old. There is still a need for further research and development to make this technology well established. An unfavourable but inseparable feature of APF is the necessity of fast switching of high currents in the power circuit of the APF. This results in a high frequency noise that may cause an electromagnetic interference (EMI) in the power distribution systems. In order to mitigate this interference, passive filters are often used at the output of the APF. APFs can be connected in several power circuit configurations. In general, they are divided into three main categories, namely shunt APF, series APF and hybrid APF.

## 3.2 – Typical APF architectures

The most widely used topology for APFs is parallel active filters. This class of filters is highly significant and commonly used in industrial processes [14]. These filters are connected to the main power circuit and serve the purpose of eliminating any harmonic distortions caused by the load current that is fed to the power supply. These filters can also help in balancing and compensating for the reactive power in three-phase currents. It is possible to connect multiple filters in parallel to handle higher currents, making them suitable for a broad range of power ratings. In this configuration (Figure 3.1), the usual name is shunt active filter, SAF [15].

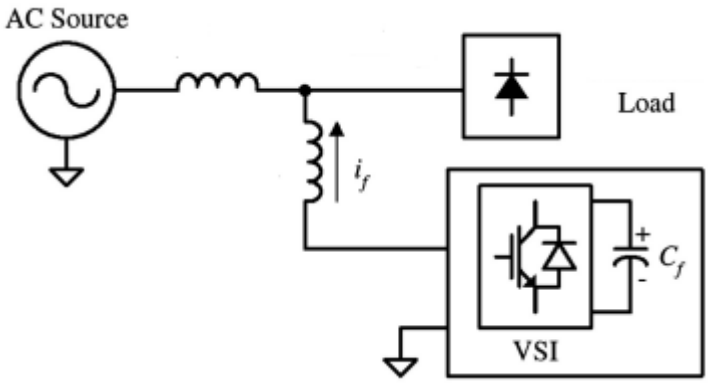



Figure 3.1 – Shunt APF [16].

Similar to shunt APF, there is the series APF. In this configuration (Figure 3.2), the APF is connected in series to the power system through a transformer. The inverter is still working as in the previous configuration, but the interfacing is done through a transformer rather than with

a short-circuit. Because this configuration is mounted in series with the power system, it is best suited for correcting voltage-related harmonic distortion.

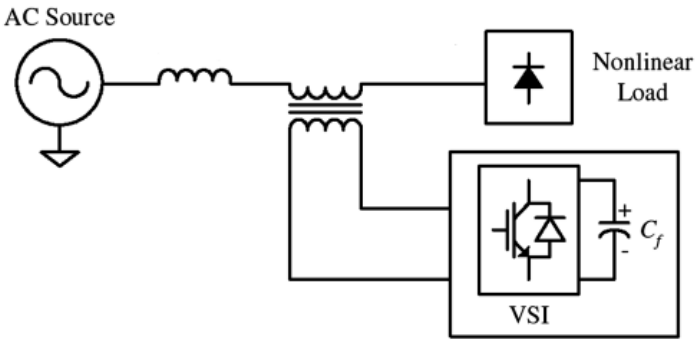



Figure 3.2 – Series APF [16].

This work uses the shunt APF but with a three-winding transformer interconnecting the three branches of the system.

## 3.3 – Dynamic model of the power converter in the 123 reference frame

The dynamic model of the three-phase power electronic converter is obtained from the circuit of Figure 3.3. By assuming the semiconductors are ideal, we can relate the switching variables, and the state variables.

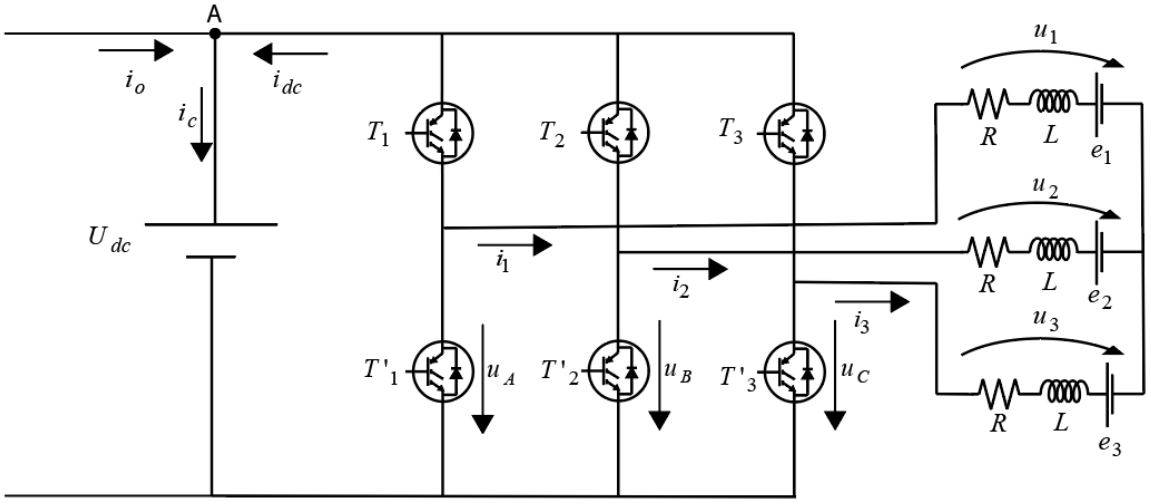



Figure 3.3 - Schematic of the power converter.

The signals $T_k$ and $T'_k$ control the semiconductors and are the opposite. This means that when $T_k$ is ON, $T'_k$ is OFF and vice versa. Knowing this, we can define a new variable $f_k$:

$$f_k = \begin{cases} 1 & \rightarrow T_k = 1 \wedge T'_k = 0 \\ 0 & \rightarrow T_k = 0 \wedge T'_k = 1 \end{cases} \tag{3.1}$$

Considering the relation between the voltages $u_k$ and the commutation variables $f_k$ we have:

$$u_k = \begin{cases} U_{dc} \rightarrow f_k = 1 \\ 0 \quad \rightarrow f_k = 0 \end{cases}, k = \{1,2,3\} \tag{3.2}$$

By applying the Kirchoff's law on the AC side we get:

$$u_k = Ri_k + L\frac{di_k}{dt} + e_k \tag{3.3}$$

Assuming only passive loads, $e_k = 0$, the state model is obtained as:

$$\frac{di_k}{dt} = -\frac{Ri_k}{L} + \frac{u_k}{L} \tag{3.4}$$

For the DC side, if we apply Kirchhoff's joint law on the DC side on the A node we get:

$$i_C = i_{dc} + i_o \tag{3.5}$$

The capacitor's current is defined by:

$$i_C = C\frac{dU_{dc}}{dt} \tag{3.6}$$

We can also relate the DC current with the phases' currents:

$$i_{dc} = f_1 i_1 + f_2 i_2 + f_3 i_3 \tag{3.7}$$

Joining (3.5), (3.6) and (3.7) we get the state model from the DC side:

$$\frac{dU_{dc}}{dt} = \frac{f_1 i_1 + f_2 i_2 + f_3 i_3 + i_o}{C} \tag{3.8}$$

With (3.3) and (3.8) we can obtain the full state space model of the converter in the 123 reference frame:

$$\frac{d}{dt}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ U_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & 0 & 0 & 0 \\ 0 & -\frac{R}{L} & 0 & 0 \\ 0 & 0 & -\frac{R}{L} & 0 \\ \frac{f_1}{C} & \frac{f_2}{C} & \frac{f_3}{C} & 0 \end{bmatrix}\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ U_{dc} \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} & 0 & 0 & 0 \\ 0 & -\frac{1}{L} & 0 & 0 \\ 0 & 0 & -\frac{1}{L} & 0 \\ 0 & 0 & 0 & \frac{1}{C} \end{bmatrix}\begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ i_0 \end{bmatrix} \tag{3.9}$$

## 3.4 – Dynamic model of the power converter in the αβ reference frame

In this sub-section, the power converter's state model in the $\alpha\beta$ reference is obtained. In other words, the 123 reference frame state model – which is a model where voltages and currents constitute a three-phase, balanced system – is transformed in a model where the variables represent a two-phase equivalent system. This transformation is called Clarke transformation and is defined by the relation below:

$$\mathbf{X_{123}} = \mathbf{C_{\alpha\beta}}\mathbf{X_{\alpha\beta}} \tag{3.10}$$

Where:

$$\mathbf{C_{\alpha\beta}} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{3.11}$$

The AC side of the model in (3.9) can be simplified in:

$$\frac{d}{dt}\mathbf{X_{123}} = \frac{\mathbf{R}}{\mathbf{L_{123}}}\mathbf{X_{123}} + \frac{1}{\mathbf{L_{123}}}\mathbf{U_{123}} \tag{3.12}$$

Using (3.10) we get:

$$\frac{d}{dt}\mathbf{C_{\alpha\beta}}\mathbf{X_{\alpha\beta}} = \frac{\mathbf{R}}{\mathbf{L_{123}}}\mathbf{C_{\alpha\beta}}\mathbf{X_{\alpha\beta}} + \frac{1}{\mathbf{L_{123}}}\mathbf{C_{\alpha\beta}}\mathbf{U_{\alpha\beta}} \tag{3.13}$$

Because this is an orthogonal matrix, the transpose and inverse of it are equal:

$$\mathbf{C}^{T}_{\alpha\beta} = \mathbf{C}^{-1}_{\alpha\beta} \tag{3.14}$$

Advantage can be taken from this, adding $C^{T}_{\alpha\beta}$ to both sides of (3.13):

$$\mathbf{C}^{T}_{\alpha\beta}\frac{d}{dt}\mathbf{C}_{\alpha\beta}\mathbf{X}_{\alpha\beta} = \mathbf{C}^{T}_{\alpha\beta}\frac{\mathbf{R}}{\mathbf{L_{123}}}\mathbf{C}_{\alpha\beta}\mathbf{X}_{\alpha\beta} + \mathbf{C}^{T}_{\alpha\beta}\frac{1}{\mathbf{L_{123}}}\mathbf{C}_{\alpha\beta}\mathbf{U}_{\alpha\beta} \tag{3.15}$$

From which the result is:

$$\frac{d}{dt}\mathbf{X}_{\alpha\beta} = \frac{\mathbf{R}}{\mathbf{L}_{\alpha\beta}}\mathbf{X}_{\alpha\beta} + \frac{1}{\mathbf{L}_{\alpha\beta}}\mathbf{U}_{\alpha\beta} \tag{3.16}$$

Where:

$$\begin{cases} \dfrac{\mathbf{R}}{\mathbf{L}_{\alpha\beta}} = \mathbf{C}^{T}_{\alpha\beta}\dfrac{\mathbf{R}}{\mathbf{L_{123}}}\mathbf{C}_{\alpha\beta} \\ \dfrac{1}{\mathbf{L}_{\alpha\beta}} = \mathbf{C}^{T}_{\alpha\beta}\dfrac{1}{\mathbf{L_{123}}}\mathbf{C}_{\alpha\beta} \end{cases} \tag{3.17}$$

Which results in:

$$\begin{aligned} \frac{\mathbf{R}}{\mathbf{L}_{\alpha\beta}} &= \begin{bmatrix} -\dfrac{R}{L} & 0 \\ 0 & -\dfrac{R}{L} \end{bmatrix} \\ \frac{\mathbf{1}}{\mathbf{L}_{\alpha\beta}} &= \begin{bmatrix} -\dfrac{1}{L} & 0 \\ 0 & -\dfrac{1}{L} \end{bmatrix} \end{aligned} \tag{3.18}$$

Therefore, the state model in $\alpha\beta$ is given by:

$$\frac{d}{dt}\begin{bmatrix} i_\alpha \\ i_\beta \\ U_{dc} \end{bmatrix} = \begin{bmatrix} -\dfrac{R}{L} & 0 & 0 \\ 0 & -\dfrac{R}{L} & 0 \\ \dfrac{f_\alpha}{C} & \dfrac{f_\beta}{C} & 0 \end{bmatrix}\begin{bmatrix} i_\alpha \\ i_\beta \\ U_{dc} \end{bmatrix} + \begin{bmatrix} -\dfrac{1}{L} & 0 & 0 \\ 0 & -\dfrac{1}{L} & 0 \\ 0 & 0 & \dfrac{1}{C} \end{bmatrix}\begin{bmatrix} U_\alpha \\ U_\beta \\ i_o \end{bmatrix} \tag{3.19}$$

## 3.5 – Dynamic model of the power converter in the dq reference frame

A time-independent model is only achieved through a Park transform. Park transforms are defined by:

$$\mathbf{X_{\alpha\beta}} = \mathbf{C_{dq}} \mathbf{X_{dq}} \tag{3.20}$$

The matrix $\mathbf{C_{dq}}$ is defined by:

$$\mathbf{C_{dq}} = \begin{bmatrix} \cos(\omega t + \varphi) & -\sin(\omega t + \varphi) \\ \sin(\omega t + \varphi) & \cos(\omega t + \varphi) \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \tag{3.21}$$

Because this is an orthogonal matrix, the transpose and inverse of it are equal.

$$\mathbf{C^T_{dq}} = \mathbf{C^{-1}_{dq}} \tag{3.22}$$

By applying (3.20) to the (3.16) model, we can rewrite into:

$$\frac{d}{dt}\mathbf{C_{dq}}\mathbf{X_{dq}} = \frac{\mathbf{R}}{\mathbf{L_{\alpha\beta}}}\mathbf{C_{dq}}\mathbf{X_{dq}} + \frac{1}{\mathbf{L_{\alpha\beta}}}\mathbf{C_{dq}}\mathbf{U_{dq}} \tag{3.23}$$

Developing the left term of this equation we get:

$$\frac{d}{dt}\left(\mathbf{C_{dq}}\right)\mathbf{X_{dq}} + \mathbf{C_{dq}}\frac{d}{dt}\left(\mathbf{X_{dq}}\right) \tag{3.24}$$

In order to be possible to multiply these matrixes, it is necessary to increase $\mathbf{C^T_{dq}}$. By developing (3.24) we get:

$$\underbrace{\begin{bmatrix} -\omega\sin(\omega t) & -\omega\cos(\omega t) & 0 \\ \omega\cos(\omega t) & -\omega\sin(\omega t) & 0 \\ 0 & 0 & 0 \end{bmatrix}}_{\mathbf{W}} \begin{bmatrix} i_d \\ i_q \\ U_{dc} \end{bmatrix} + \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) & 0 \\ -\sin(\omega t) & \cos(\omega t) & 0 \\ 0 & 0 & 0 \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_d \\ i_q \\ U_{dc} \end{bmatrix} \tag{3.25}$$

Adding this to (3.23):

$$\mathbf{W}\mathbf{X_{dq}} + \mathbf{C_{dq}}\frac{d}{dt}\left(\mathbf{X_{dq}}\right) = \frac{\mathbf{R}}{\mathbf{L_{\alpha\beta}}}\mathbf{C_{dq}}\mathbf{X_{dq}} + \frac{1}{\mathbf{L_{\alpha\beta}}}\mathbf{C_{dq}}\mathbf{U_{dq}} \tag{3.26}$$

Rearranging this equation in the form of $\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u}$ we get:

$$\mathbf{C_{dq}}\frac{d}{dt}\mathbf{X_{dq}} = \left(\frac{\mathbf{R}}{\mathbf{L_{\alpha\beta}}}\mathbf{C_{dq}X_{dq}} - \mathbf{WX_{dq}}\right) + \frac{1}{\mathbf{L_{\alpha\beta}}}\mathbf{C_{dq}U_{dq}} \tag{3.27}$$

The term $\frac{\mathbf{R}}{\mathbf{L_{\alpha\beta}}}\mathbf{C_{dq}X_{dq}} - \mathbf{WX_{dq}}$ can be condensed into:

$$\mathbf{F} = \begin{bmatrix} -\frac{R}{L}\cos(\omega t) + \omega\sin(\omega t) & \frac{R}{L}\sin(\omega t) + \omega\cos(\omega t) & 0 \\ -\frac{R}{L}\sin(\omega t) + \omega\cos(\omega t) & -\frac{R}{L}\cos(\omega t) + \omega\sin(\omega t) & 0 \\ \frac{f_\alpha}{C}\cos(\omega t) + \frac{f_\beta}{C}\sin(\omega t) & -\frac{f_\alpha}{C}\cos(\omega t) + \frac{f_\beta}{C}\sin(\omega t) & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ U_{dc} \end{bmatrix} \tag{3.28}$$

By attributing this matrix the name $\mathbf{F}$, we can rewrite (3.27) into:

$$\mathbf{C_{dq}}\frac{\mathrm{d}}{\mathrm{dt}}\mathbf{X_{dq}} = \mathbf{F} + \frac{1}{\mathbf{L_{\alpha\beta}}}\mathbf{C_{dq}U_{dq}} \tag{3.29}$$

By multiplying $\mathbf{C}_{dq}^{T}$ on both sides of the equation:

$$\mathbf{C_{dq}^{T}C_{dq}}\frac{d}{dt}\mathbf{X_{dq}} = \mathbf{C_{dq}^{T}F} + \mathbf{C_{dq}^{T}}\frac{1}{\mathbf{L_{\alpha\beta}}}\mathbf{C_{dq}U_{dq}} \tag{3.30}$$

Where:

$$\begin{aligned} \mathbf{C_{dq}^{T}F} = \frac{\mathbf{R}}{\mathbf{L_{dq}}}\mathbf{X_{dq}} &= \begin{bmatrix} -\frac{R}{L} & \omega & 0 \\ \omega & -\frac{R}{L} & 0 \\ \frac{f_d}{C} & \frac{f_q}{C} & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ U_{dc} \end{bmatrix} \\ \mathbf{C_{dq}^{T}}\frac{\mathbf{1}}{\mathbf{L_{\alpha\beta}}}\mathbf{C_{dq}U_{dq}} = \frac{\mathbf{1}}{\mathbf{L_{dq}}}\mathbf{U_{dq}} &= \begin{bmatrix} -\frac{1}{L} & 0 & 0 \\ 0 & -\frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{C} \end{bmatrix} \begin{bmatrix} U_d \\ U_q \\ i_o \end{bmatrix} \end{aligned} \tag{3.31}$$

Jointing the equations of (3.31) with (3.30), the model in the dq reference frame is obtained:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ U_{dc} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & \omega & 0 \\ \omega & -\frac{R}{L} & 0 \\ \frac{f_d}{C} & \frac{f_q}{C} & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ U_{dc} \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} & 0 & 0 \\ 0 & -\frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{C} \end{bmatrix} \begin{bmatrix} U_d \\ U_q \\ i_o \end{bmatrix} \tag{3.32}$$

Having the dynamic model of the power converter in the dq reference frame, PID controllers can now be designed.

## 3.6 – Active power filter

The active power filter decreases harmonic penetration and increases power factor on the grid side by injecting active and reactive power which will cancel unwanted components on the load side by superposition. We can think of it as if the filter is sourcing the load with the harmonic components and reactive power it needs so that the grid doesn't have to.

Furthermore, the active power filter can also direct power onto the grid when the available power in the DC microgrid side is enough.

### 3.6.1 – Reference current determination

In order to control active and reactive power, the electrical signals must be transformed into a reference frame that makes it easier to analyse and control the power flow. One such reference frame is the rotating dq reference frame, which is a coordinate system that rotates with the same frequency as the fundamental component of the electrical signal.

In a system with no harmonic components and a unitary power factor, the direct-quadrature components of voltages and currents will be constant over time – we can think of it as a DC approximation of a three phase AC system.

However, in practical power systems, there are often harmonic components present, which cause fluctuations in the voltage and current waveforms. Additionally, the power factor may not be unitary, meaning that the power is not being consumed optimally. These distortions can cause instability in the system and reduce efficiency.

To mitigate these effects, the active filter described in this dissertation is used to control both the active and reactive power. The active filter is designed to cancel out the harmonic components and improve the power factor by injecting signals into the system that counteract the distortions.

Active and reactive power in the dq plane can be obtained from the instantaneous power p-q theory [17]:

$$p = u_\alpha i_\alpha + u_\beta i_\beta \tag{3.33}$$

$$q = u_\beta i_\alpha - u_\alpha i_\beta \tag{3.34}$$

From here, we can apply equation (3.20):

$$\begin{aligned} p = &\left(u_d \cos\theta - u_q \sin\theta\right)\left(i_d \cos\theta - i_q \sin\theta\right) + \\ &\left(u_d \sin\theta + u_q \cos\theta\right)\left(i_d \sin\theta + i_q \cos\theta\right) \end{aligned} \tag{3.35}$$

$$\begin{aligned} q = &\left(u_d \sin\theta + u_q \cos\theta\right)\left(i_d \cos\theta - i_q \sin\theta\right) - \\ &\left(u_d \cos\theta - u_q \sin\theta\right)\left(i_d \sin\theta + i_q \cos\theta\right) \end{aligned} \tag{3.36}$$

From which we can simplify into (3.37) and (3.38):

$$p = u_d i_d + u_q i_q + 2u_0 i_0 \tag{3.37}$$

$$q = -u_d i_q + u_q i_d \tag{3.38}$$

Because we are assuming voltages in the system do not contain harmonic components and are all phased 120º, the quadrature and zero components of the voltages are null.

$$u_q = 0; u_0 = 0 \tag{3.39}$$

Simplifying (3.37) and (3.38) we get:

$$p = u_d i_d \tag{3.40}$$

$$q = -u_d i_q \tag{3.41}$$

Grid synchronization

The first step for the current control method is to synchronize the inverter's reference frames with the grid's reference frame ($\Theta_S$). The grid's reference frame is detected applying Clarke transformation to its voltages (Figure 4.1).

$$\mathbf{u}_{\mathbf{G}\alpha\beta\gamma} = \mathbf{C}_{\alpha\beta}\mathbf{u}_{\mathbf{G}123}$$

$$\begin{bmatrix} u_{G\alpha} \\ u_{G\beta} \\ u_{G\gamma} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} u_{G_1} \\ u_{G_2} \\ u_{G_3} \end{bmatrix} \tag{3.42}$$

Because we are assuming voltages on the grid side are all balanced, phased perfectly and have no harmonic components, we can assume that the sum of all phases is null.

$$u_{G_1} + u_{G_2} + u_{G_3} = 0 \tag{3.43}$$

Therefore, the gamma component is also null.

$$u_{G_\gamma} = 0 \tag{3.44}$$

The grid's reference frame can then be obtained through the following expression.

$$\theta_G = \arctan\left(\frac{v_{G\beta}}{v_{G\alpha}}\right) \in [-\pi, +\pi] \tag{3.45}$$

$\theta_G$ now represents where the system is in the $\alpha\beta$ reference frame, as showcased in Figure 3.4.

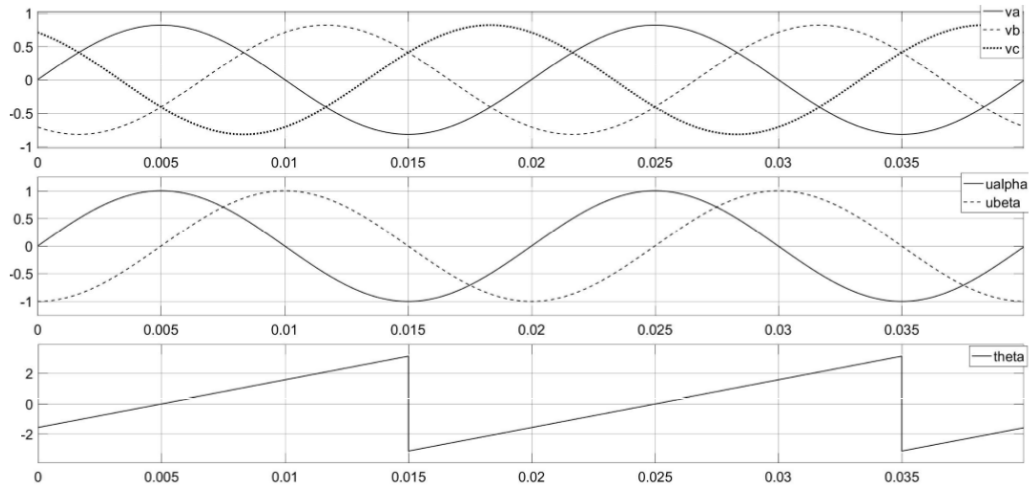



Figure 3.4 – abc, $\alpha\beta$ and $\theta_G$ in a balanced system.

For the active power filter to be able to control harmonic penetration and power factor, *d* and *q* components of the load's current must be calculated, $i_{L_d}$ and $i_{L_q}$ respectively.

The dq reference frame components of currents are defined by the expression below.

$$\mathbf{i}_{\mathbf{dq0}} = \mathbf{P}\mathbf{i}_{\boldsymbol{\alpha\beta\gamma}} \Leftrightarrow \begin{bmatrix} i_d \\ i_q \\ i_d \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) & 0 \\ -\sin(\theta) & \cos(\theta) & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ i_\gamma \end{bmatrix} \tag{3.46}$$

Where components α, β and γ of the current are calculated the same way as done in (3.42).

$$\mathbf{i}_{\boldsymbol{\alpha\beta\gamma}} = \mathbf{C}_{\boldsymbol{\alpha\beta}}^{\mathbf{T}} \mathbf{i}_{\mathbf{abc}} \tag{3.47}$$

Power factor correction

Simplifying the schematic in Figure 4.1, Figure 3.5 is obtained.

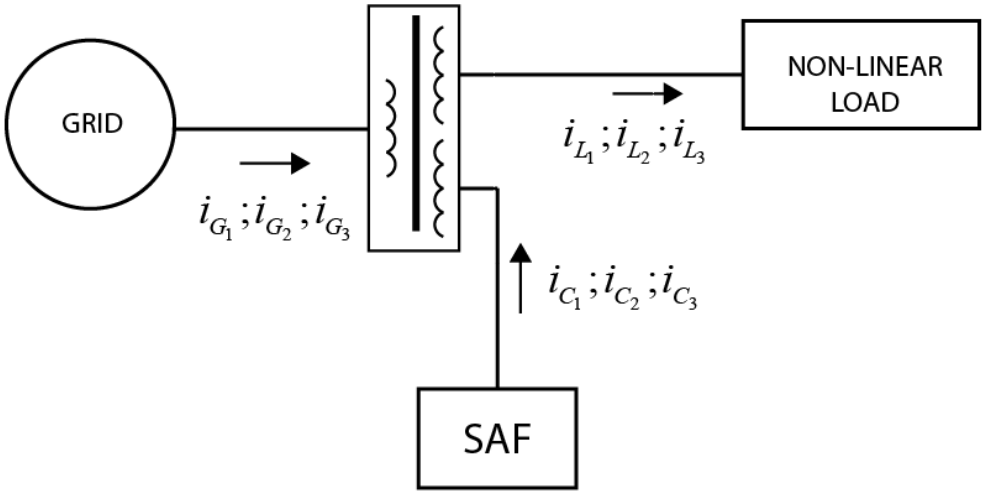



Figure 3.5 - Schematic simplification of the full system.

Generalizing, the currents in all the transformer's windings can be related through the following expression.

$$i_{G_k} = \frac{1}{r}\left(i_{L_k} - i_{C_k}\right) \tag{3.48}$$

Where *r* is the winding ration between the primary winding and the other windings (secondary and tertiary).

We can rewrite (3.41) with:

$$q_G = -u_d \underbrace{\frac{1}{r}\left(i_{L_q} - i_{C_q}\right)}_{i_{G_q}} \tag{3.49}$$

For power factor to be unitary, reactive power must be null. For reactive power to be null, the converter must follow the quadrature components of the load.

$$i_{L_q} = i_{C_q} \Rightarrow q_G = 0 \tag{3.50}$$

Harmonic content mitigation

In the direct-quadrature frame, current harmonic content represents itself in an alternating component in the direct component.

There are now two components of $i_d$, a constant one which is related to the "clean" active power, $\overline{i_d}$, and an alternating other which is related to the harmonic components, $\widetilde{i_d}$.

$$i_d = \overline{i_d} + \widetilde{i_q} \tag{3.51}$$

By applying (3.48) we get

$$i_{G_d} = \frac{1}{r}\left(-i_{C_d} + i_{L_d}\right) \tag{3.52}$$

$$i_{G_d} = \frac{-i_{C_d} + \overline{i_{L_d}} + \widetilde{i_{L_d}}}{r} \tag{3.53}$$

By observing the equation (3.53), it is possible to conclude that, in order for the grid to only source the active power-related component of the current in the load, $\overline{i_{L_d}}$, the converter must follow the alternating component of the direct component of the current in the load, as show cased in the equation (3.54).

$$i_{C_d} = \widetilde{i_{L_d}} \Rightarrow i_{G_d} = \frac{\overline{i_{L_d}}}{r} \tag{3.54}$$

### 3.6.2 – DC voltage control

Considering the model of the converter in the dq reference frame (3.32) for the state variable $U_{dc}$.

$$\frac{d}{dt}U_{dc} = \frac{f_d}{C}i_d + \frac{f_q}{C}i_q + \frac{i_o}{C} \tag{3.55}$$

From here results Figure 3.6.

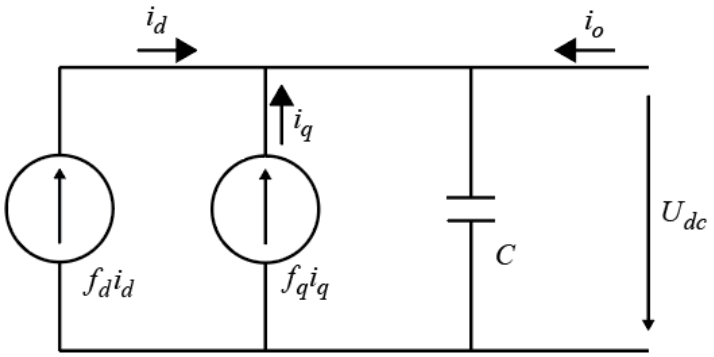



Figure 3.6 – Equivalent circuit converter in the dq reference frame.

Considering the power factor is unitary ($i_q = 0$) and $i_o$ is the current which results from a resistor, *R*, placed in parallel with the capacitor:

$$i_o = -\frac{U_{dc}}{R} \tag{3.56}$$

With this simplification, it is possible to rewrite (3.55) into:

$$\frac{d}{dt}U_{dc} = \frac{f_d}{C}i_d - \frac{U_{dc}}{RC} \tag{3.57}$$

From here, the equivalent circuit of the converter in the dq reference frame is obtained (Figure 3.7).

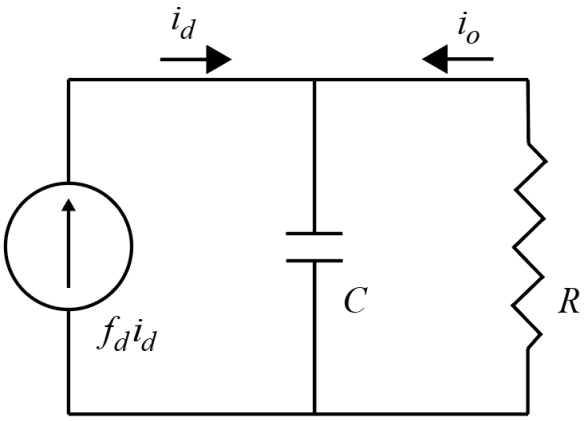



Figure 3.7 - Equivalent circuit of the converter in the dq reference frame.

Applying the Laplace transform and rearranging the equation above:

$$\frac{U_{dc}}{i_{dref}} = \frac{f_d R}{RCs + 1} \tag{3.58}$$

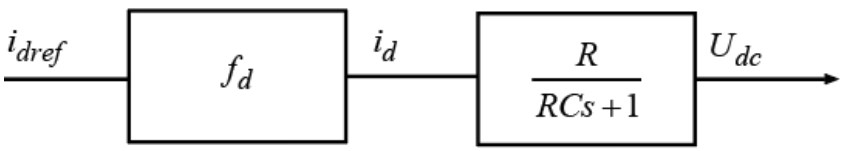



Figure 3.8 – Block diagram of the correlation between $U_{dc}$ and $i_{dref}$.

Considering a statistical delay, $T_d$, associated to the switching of the semiconductors.

$$i_d \approx \frac{i_{dref}}{1+sT_d} \tag{3.59}$$

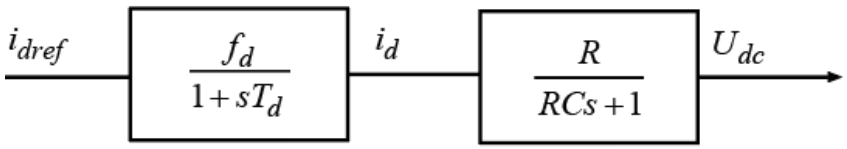



Figure 3.9 - Block diagram of the correlation between $U_{dc}$ and $i_{dref}$, with $i_d$ delay.

Because we intend to control the $U_{dc}$ voltage, a controller is included in the block diagram:

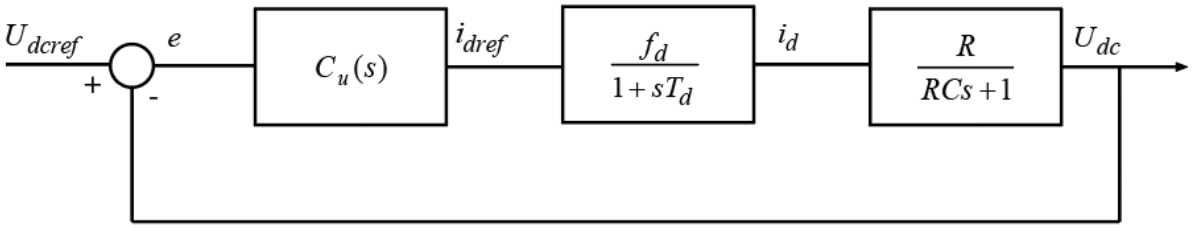



Figure 3.10 – Block diagram in a closed-loop of the DC voltage control system.

$$C_u(s) = k_p + \frac{k_i}{s} = \frac{k_i\left(\frac{k_p}{k_i}s+1\right)}{s} \tag{3.60}$$

If a PI controller – with its transfer function given by (3.60), where $k_p$ and $k_i$ are the proportional and integral gains – the open loop transfer function is given by:

$$OLTF_{dc} = \frac{k_i\left(\frac{k_p}{k_i}s+1\right)f_d}{s(1+sT_d)(RCs+1)} \tag{3.61}$$

The controller's zero is placed in order to cancel the most dominant pole of the transfer function, $-1/(RC)$.

$$\frac{k_p}{k_i} = RC \tag{3.62}$$

The closed loop transfer function for this system is given by:

$$\frac{U_{dc}(s)}{U_{dcref}(s)} = \frac{\frac{k_i f_d R}{T_d}}{s^2 + \frac{s}{T_d} + \frac{k_i f_d R}{T_d}} \tag{3.63}$$

From here we obtain the following correlations:

$$\begin{cases} \frac{k_p}{k_i} = RC \\ 2\xi\omega_n = \frac{1}{T_d} \\ \omega_n{}^2 = \frac{k_i f_d R}{T_d} \end{cases} \Rightarrow \begin{cases} \omega_n = \frac{1}{2\xi T_d} \\ k_i = \frac{T_d \omega_n{}^2}{f_d R} \\ k_p = k_i CR \end{cases} \tag{3.64}$$

The controller is designed around the dampening factor $(\xi = 2)$. The natural frequency is then obtained $\omega_n = 5000$ rads$^{-1}$.

In order to determine a value for $f_d$, it is assumed that the power flowing through the AC and the DC side of the converter are the same $(P_{AC} = P_{DC})$:

$$U_{dc}(-i_o) = U_d i_d \tag{3.65}$$

By applying Kirchhoff's joint law in the node A of Figure 3.3, the equation below is obtained:

$$f_d i_d + i_o = i_c \tag{3.66}$$

For mean values, it is assumed that the current in the capacitor is null$(i_c = 0)$. Joining the two previous equations, $f_d$ is determined:

$$\left.\begin{cases} U_{dc}(-i_o) = U_d i_d \\ f_d i_d = -i_o \end{cases}\right\rangle f_d = \frac{U_d}{U_{dc}} = \frac{122.5}{130} = 1.225 \tag{3.67}$$

The value of the direct component of the voltages on the converter side, $U_d$, is obtained from assuming phase to neutral voltages on the 123 reference frame on the grid side to be 100 $V_{RMS}$ and ideal which, transformed via a transformer with a Dy configuration and 2:1 winding ratio, will result to be 122.5 V.

For control purposes, $T_d$ is defined as half the commutation period.

$$T_d = \frac{\frac{1}{f_c}}{2} = \frac{\frac{1}{10000}}{2} = 50\,\mu s \tag{3.68}$$

The capacitance is defined according to what is used on the laboratory, 410 mF, and the resistance is defined as 2 kΩ. This resistor is not used on the laboratory and are only used in the simulation.

The controller's parameters are then obtained:

$$\begin{cases} k_p = 28.76 \\ k_i = 0.04 \end{cases} \tag{3.69}$$

### 3.6.3 – Converter current control

Considering the model of the converter in the dq reference frame (3.32) for the state variables $i_d$ and $i_q$.

$$\begin{cases} \frac{d}{dt} i_d = -\frac{R}{L} i_d + \omega i_q - \frac{U_d}{L} \\ \frac{d}{dt} i_q = -\frac{R}{L} i_q + \omega i_d - \frac{U_q}{L} \end{cases} \tag{3.70}$$

For control design purposes, it is supposed the currents in both axes are independant $\left(\omega i_d = \omega i_q = 0\right)$.

$$\begin{cases} \frac{d}{dt} i_d = -\frac{R}{L} i_d - \frac{U_d}{L} \\ \frac{d}{dt} i_q = -\frac{R}{L} i_q - \frac{U_q}{L} \end{cases} \tag{3.71}$$

Applying the Laplace Transform to the equations above and rearranging them

$$\begin{cases} \frac{i_d}{U_d} = \frac{1}{sL + R} \\ \frac{i_q}{U_q} = \frac{1}{sL + R} \end{cases} \tag{3.72}$$

Considering a delay, $T_u$, between the reference voltages and the real voltages.

$$\begin{cases} U_d \approx \dfrac{U_{dref}}{1+sT_u} \\ U_q \approx \dfrac{U_{qref}}{1+sT_u} \end{cases} \tag{3.73}$$

Because the transfer function for both axes is the same, the controller used in each of the axes is the same, $C_i$ (s).

The block diagram that correlates $i_d$ and $U_{dref}$ is defined by

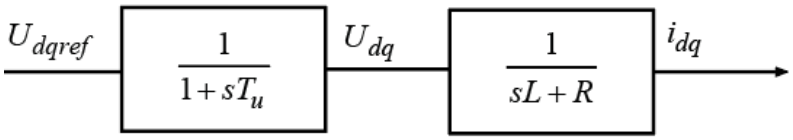



Figure 3.11 - Block diagram of the correlation between the currents $i_d$, $i_q$ and the voltages $U_d$, $U_q$.

Because we intend to control the currents $i_d$ and $i_q$, a controller is included in the block diagram:

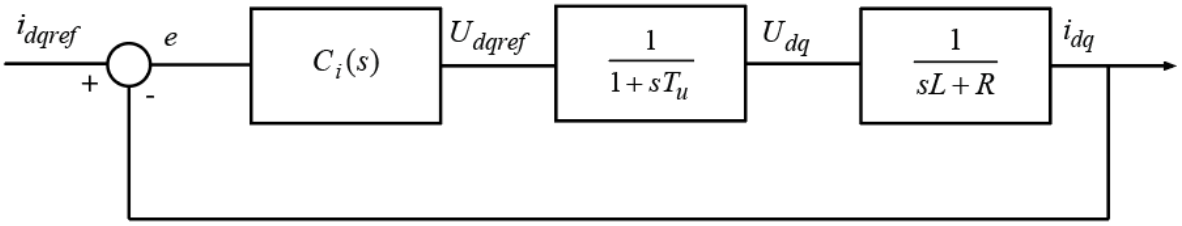



Figure 3.12 – Closed-loop block diagram of the current control system.

$$C_i(S) = k_p + \frac{k_i}{s} = \frac{k_i\left(\frac{k_p}{k_i}s+1\right)}{s} \tag{3.74}$$

Assuming a PI controller with the (3.74) transfer function, the open loop transfer function is given by:

$$OLTF_i = \frac{k_i\left(\frac{k_p}{k_i}s+1\right)}{s(1+sT_u)(sL+R)} \tag{3.75}$$

The controller's zero is placed in order to cancel the most dominant pole of the transfer function, $-R/L$.

$$\frac{k_p}{k_i} = \frac{L}{R} \tag{3.76}$$

The open-loop transfer function (3.75) can then be simplified into

$$OLTF_i = \frac{k_i}{sR(1+sT_u)} \tag{3.77}$$

The closed-loop transfer function can now be obtained:

$$CLTF_i = \frac{k_i}{T_u R s^2 + Rs + k_i} \tag{3.78}$$

Comparing the system's closed-loop transfer function (3.78) with the standard closed-loop transfer function (3.79):

$$\frac{Y(s)}{X(s)} = \frac{{\omega_n}^2}{s^2 + 2\xi\omega_n s + {\omega_n}^2} \tag{3.79}$$

$$\frac{i_{dq}(s)}{i_{dqref}(s)} = \frac{\frac{k_i}{T_u R}}{s^2 + \frac{s}{T_u} + \frac{k_i}{T_u R}} \tag{3.80}$$

From here we obtain the following correlations:

$$\begin{cases} \frac{k_p}{k_i} = \frac{R}{L} \\ 2\xi\omega_n = \frac{1}{T_u} \\ {\omega_n}^2 = \frac{k_i}{T_u R} \end{cases} \Rightarrow \begin{cases} \omega_n = \frac{1}{2\xi T_u} \\ k_i = T_u R {\omega_n}^2 \\ k_p = \frac{R k_i}{L} \end{cases} \tag{3.81}$$

The controller is designed around the dampening factor $(\xi = 3)$. The natural frequency is then obtained $\omega_n = 3333.3 \text{ rads}^{-1}$.

For control purposes, $T_d$ is defined as half the switching period.

$$T_d = \frac{\frac{1}{f_c}}{2} = \frac{\frac{1}{10000}}{2} = 50\,\mu s \tag{3.82}$$

The inductance is defined as 3 mH, and the resistance is defined as 20 mΩ. These components are not used in the laboratory and are only used in the simulation.

The resistor and inductance are defined as:

$$\begin{cases} R = 20 \ \ \text{m}\Omega \\ L = 3 \ \ \text{mH} \end{cases} \tag{3.83}$$

The controller's gains are then obtained:

$$\begin{cases} k_p = 74.07 \\ k_i = 11.11 \end{cases} \tag{3.84}$$

## 3.7 – SVPWM applied to three-phase power electronic converter

The currents generated by the AC/DC converter are obtained with Space Vector Pulse Width Modulation (SVPWM). This method is based on the concept that it is possible to represent a three-phase system in a 2D plane. This plane is created with $2^n$ vectors – with n being the number of legs of the converter, considering the two states (on and off) for each semiconductor. The studied system possesses 3 switched states and, therefore, 8 $(2^3)$vectors.

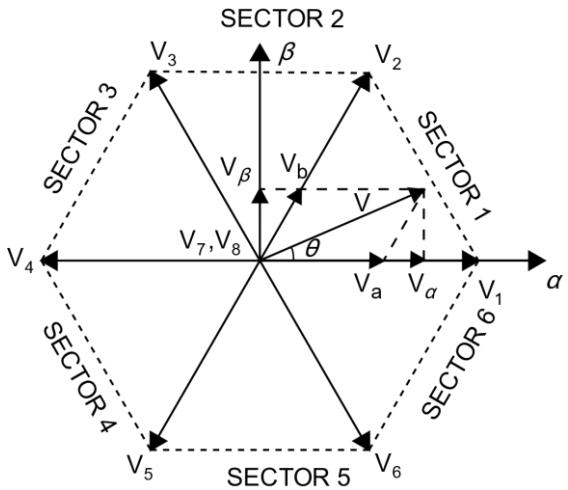



Figure 3.13 - Space-Vector Plane.

Having Figure 3.3 and Figure 3.12 in mind, Table 3.1 is obtained.

Table 3.1 – Phase to phase and phase to neutral voltages of each vector.

| State | $f_1$ | $f_2$ | $f_3$ | $u_A$ | $u_B$ | $u_C$ | $u_1$ | $u_2$ | $u_3$ | $u_{12}$ | $u_{23}$ | $u_{31}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_1$ | 1 | 0 | 0 | $U_{dc}$ | 0 | 0 | $\frac{2}{3}U_{dc}$ | $-\frac{1}{3}U_{dc}$ | $-\frac{1}{3}U_{dc}$ | $U_{dc}$ | 0 | $-U_{dc}$ |
| $V_2$ | 1 | 1 | 0 | $U_{dc}$ | $U_{dc}$ | 0 | $\frac{1}{3}U_{dc}$ | $\frac{1}{3}U_{dc}$ | $-\frac{2}{3}U_{dc}$ | 0 | $U_{dc}$ | $-U_{dc}$ |
| $V_3$ | 0 | 1 | 0 | 0 | $U_{dc}$ | 0 | $-\frac{1}{3}U_{dc}$ | $\frac{2}{3}U_{dc}$ | $-\frac{1}{3}U_{dc}$ | $-U_{dc}$ | $U_{dc}$ | 0 |
| $V_4$ | 0 | 1 | 1 | 0 | $U_{dc}$ | $U_{dc}$ | $-\frac{2}{3}U_{dc}$ | $\frac{1}{3}U_{dc}$ | $\frac{1}{3}U_{dc}$ | $-U_{dc}$ | 0 | $U_{dc}$ |
| $V_5$ | 0 | 0 | 1 | 0 | 0 | $U_{dc}$ | $-\frac{1}{3}U_{dc}$ | $-\frac{1}{3}U_{dc}$ | $\frac{2}{3}U_{dc}$ | 0 | $-U_{dc}$ | $U_{dc}$ |
| $V_6$ | 1 | 0 | 1 | $U_{dc}$ | 0 | $U_{dc}$ | $\frac{1}{3}U_{dc}$ | $-\frac{2}{3}U_{dc}$ | $\frac{1}{3}U_{dc}$ | $U_{dc}$ | $-U_{dc}$ | 0 |
| $V_7$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $V_8$ | 1 | 1 | 1 | $U_{dc}$ | $U_{dc}$ | $U_{dc}$ | 0 | 0 | 0 | 0 | 0 | 0 |

Where

$$\begin{cases} u_1 = \frac{1}{3}\left(2u_A - u_B - u_C\right) \\ u_2 = \frac{1}{3}\left(-u_A + 2u_B - u_C\right) \\ u_1 = \frac{1}{3}\left(-u_A - u_B + 2u_C\right) \end{cases} \tag{3.85}$$

$$\begin{cases} u_{12} = u_A - u_B \\ u_{23} = u_B - u_C \\ u_{31} = u_C - u_A \end{cases} \tag{3.86}$$

Table 3.2 - Phase to neutral and αβ voltages of each vector.

| State | $u_1$ | $u_2$ | $u_3$ | $u_\alpha$ | $u_\beta$ | $\angle\alpha\beta$ |
|---|---|---|---|---|---|---|
| $V_1$ | $\frac{2U_{dc}}{3}$ | $-\frac{U_{dc}}{3}$ | $-\frac{U_{dc}}{3}$ | $\frac{2U_{dc}}{3}$ | 0 | 0º |
| $V_2$ | $\frac{U_{dc}}{3}$ | $\frac{U_{dc}}{3}$ | $-\frac{2U_{dc}}{3}$ | $\frac{U_{dc}}{3}$ | $\frac{4U_{dc}}{7}$ | 60º |
| $V_3$ | $-\frac{U_{dc}}{3}$ | $\frac{2U_{dc}}{3}$ | $-\frac{U_{dc}}{3}$ | $-\frac{U_{dc}}{3}$ | $\frac{4U_{dc}}{7}$ | 120º |
| $V_4$ | $-\frac{2U_{dc}}{3}$ | $\frac{U_{dc}}{3}$ | $\frac{U_{dc}}{3}$ | $-\frac{2U_{dc}}{3}$ | 0 | 180º |
| $V_5$ | $-\frac{U_{dc}}{3}$ | $-\frac{U_{dc}}{3}$ | $\frac{2U_{dc}}{3}$ | $-\frac{U_{dc}}{3}$ | $-\frac{4U_{dc}}{7}$ | 240º |
| $V_6$ | $\frac{U_{dc}}{3}$ | $-\frac{2U_{dc}}{3}$ | $\frac{U_{dc}}{3}$ | $\frac{U_{dc}}{3}$ | $-\frac{4U_{dc}}{7}$ | 300º |
| $V_7$ | 0 | 0 | 0 | 0 | 0 | N/A |
| $V_8$ | 0 | 0 | 0 | 0 | 0 | N/A |

Each of the reference voltages in the plane represent one of the switching states represented in the Table 3.2.

Because the reference values for the converter are obtained in the rotating frame dq, these values are then reconverted into Cartesian $(\alpha\beta)$ and then into a polar value (defined by magnitude, $mag$, and angle, $\theta_C$):

$$\begin{cases} mag = \sqrt{\left\|\overrightarrow{U_\alpha}\right\|^2 + \left\|\overrightarrow{U_\beta}\right\|^2} \\ \theta_C = arctg\left(\frac{\left\|\overrightarrow{U_\beta}\right\|}{\left\|\overrightarrow{U_\alpha}\right\|}\right) \end{cases} \tag{3.87}$$

For computational purposes, *mag* cannot be used as represented in the equation above. As a result, the modulation index, $m \in [0,1]$, is introduced. Because the maximum value of *mag* is $\frac{2U_{dc}}{3}$, we obtain:

$$m = \frac{mag}{\frac{2U_{dc}}{3}} = \frac{3\sqrt{\left\|\overrightarrow{U_\alpha}\right\|^2 + \left\|\overrightarrow{U_\beta}\right\|^2}}{2U_{dc}} \tag{3.88}$$

# Chapter 4

# Simulation

## 4.1 – Introduction

To prove the concept of this work, a simulation was made in Matlab/Simulink. The simulation, schematized in Figure 4.1, comprises the grid bus, Simulink's three phase three-winding transformer model (with a Dy11 configuration), DC microgrid (represented as a DC current source), and a range of linear and non-linear loads.

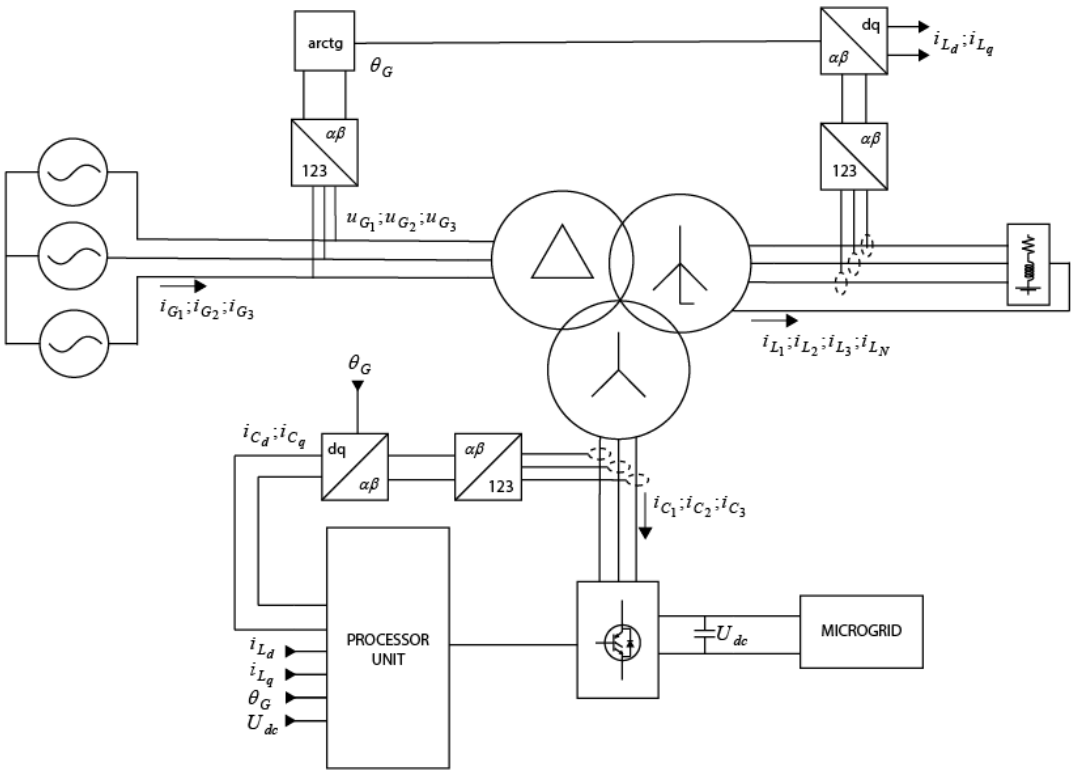



Figure 4.1 – Global schematic of the simulation.

Instantaneous voltages from the grid are measured and transformed to αβ in order to find the position of the system in the referential, $\theta'_G$. At the same time, instantaneous values of currents

from the loads $(i_{L_1}, i_{L_2}, i_{L_3})$ and the converter $(i_{C_1}, i_{C_2}, i_{C_3})$ are also obtained and transformed into αβ and then into dq (using $\theta'_G$, which is the position of the voltages in the grid shifted 30º due to delay caused by the transformer which is connected in a Dy11 configuration) in order to determine the reference currents for the converter to inject/be injected with. These values are then fed into a control loop managed by a processor unit.

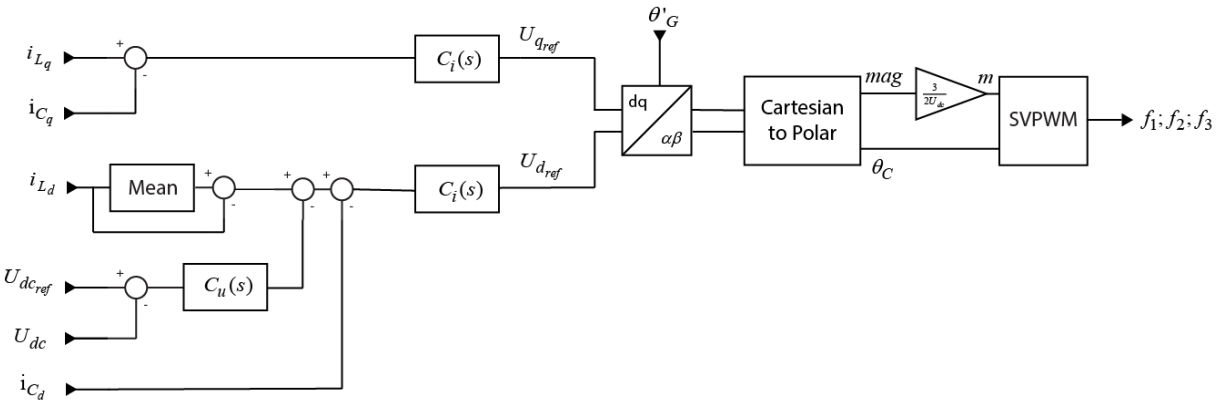



Figure 4.2 – Processor unit's schematic.

The processor unit's (Figure 4.2) function is to generate the gate signals of the semiconductors using the signals above. Firstly, the direct-axis current from the loads, $i_{L_d}$, is subtracted to its mean value (see sub-chapter "Harmonic content control"), obtained over a running window with an interval of 10 ms. To this value, the current generated by the DC voltage control loop (see sub-chapter "DC voltage control") is subtracted. The value resulting from this, aswell as the quadrature-axis current from the loads, $i_{L_q}$, are then subtracted by their converter's currents counterparts, $i_{C_d}$and $i_{C_q}$, in order to be fed into the controllers, $C_i(s)$ (see sub-chapter "Converter current control"). Past this, reference voltages, $U_{d_{ref}}$ and $U_{q_{ref}}$, are obtained. These voltages are then reconverted back into αβ values and then transformed in a polar value. The module of the polar value is then manipulated as described in the sub-chapter "SVPWM applied to three-phase power electronics". Having the polar value of the voltages for the converter to apply it is fed into the SVPWM algorithm and the gate signals are generated.

## 4.2 – Simulation results

The simulation results below show the currents in all the transformer arms during compensation. The results also show the voltages, currents, active power, reactive power and harmonic spectrum of one phase's current before and after the compensation. It is also shown the progression of the DC voltage when there is a step up of the microgrid current and the switch of flow of power when the power injected by the DC microgrid exceeds the power consumed by the load.

All of the experiments shown were taken with the following parameters:

- DC bus at 130 V
- Phase to phase voltage of the grid at 100 $V_{RMS}$.

### 4.2.1 – Experiment 1 – Balanced RL load

For the first experiment, a balanced RL load was added to the system (R=20 Ω/phase; L=23 mH/phase; lag=20º).

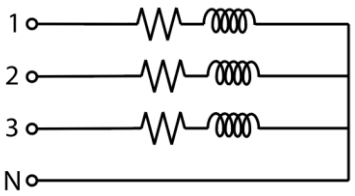



Figure 4.3 – Schematic of the load used in the first and second experiment.

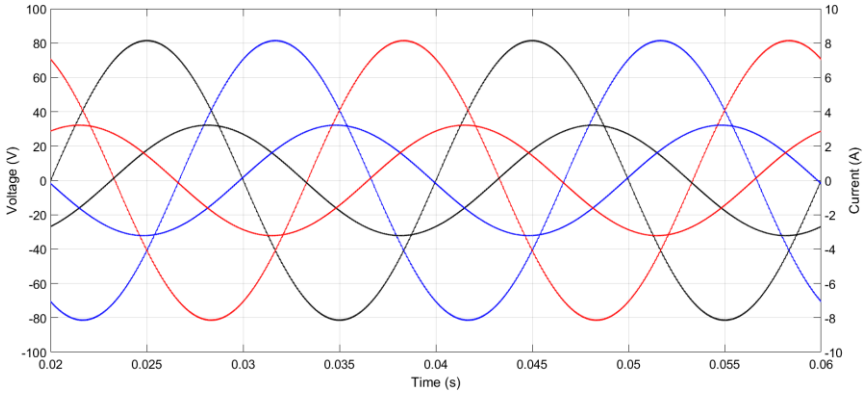
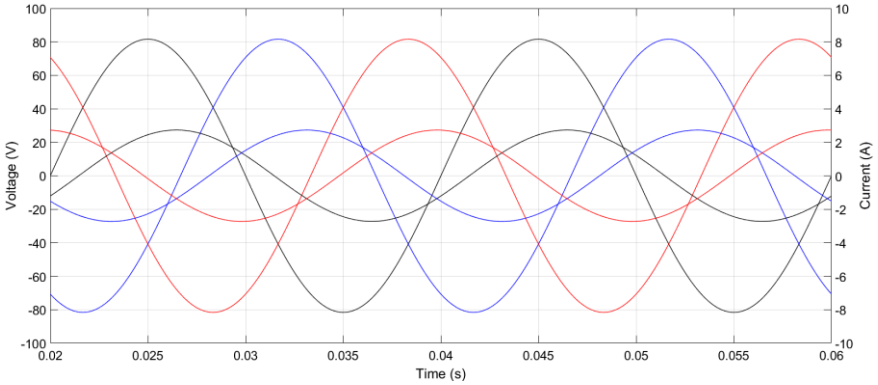
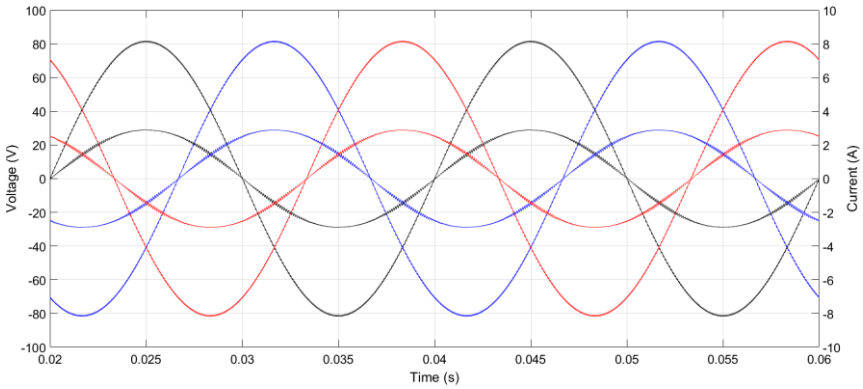



Figure 4.4 - Current (smaller) of a RL load and grid voltages (bigger).




a) Before Compensation




b) After Compensation

Figure 4.5 – Grid voltages (bigger) and currents (smaller) before (a) and after (b) compensation for a RL load.

From Figure 4.5, it is possible to see the controller can correct the phase of the current in each phase in the grid but adds ripple, which is more significant when any two phases cross each other.

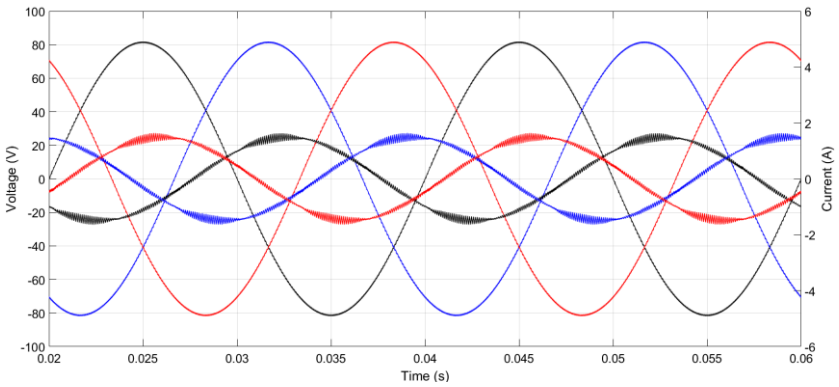
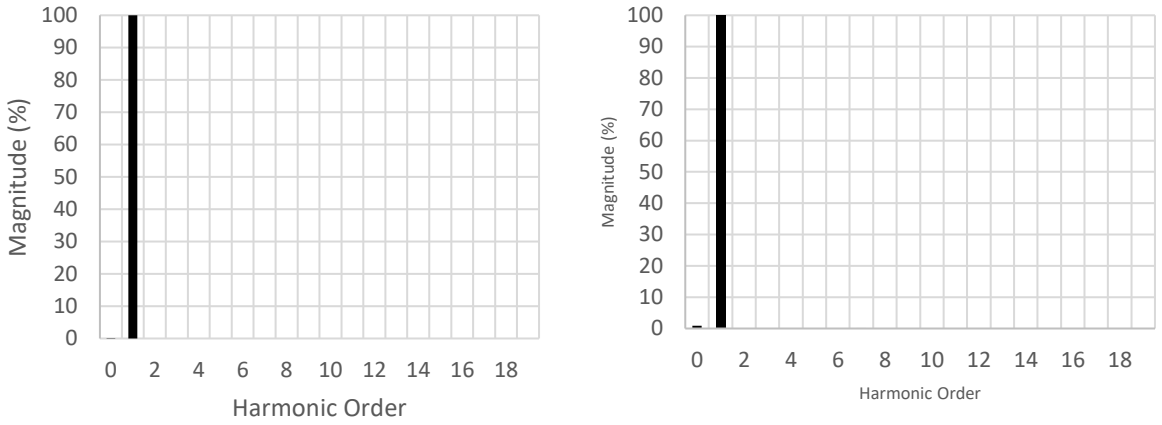



Figure 4.6 – Currents (smaller) generated by the power converter for a RL load and grid voltages (bigger).




a) Before compensation

b) After compensation

Figure 4.7 – Harmonic spectrum of grid current in one phase before (a) and after (b) compensation of a RL load.

Table 4.1 – THD of the current in one phase of the grid, active and reactive power on the grid before and after compensation of a RL load.

| | Before compensation | After compensation |
|---|---|---|
| Grid active power (W) | 300 | 350 |
| Grid reactive power (var) | 150 | 3 |
| Grid current THD (%) | 0.01 | 1.99 |

From observing Figure 4.7 and Table 4.1, it is noticeable that, for RL loads, the converter can almost correct power factor but adds significant harmonic distortion due to its switching characteristics.

## 4.2.2 – Experiment 2 – Unbalanced RL load

The second experiment was conducted with the same configuration for the load as seen in the precious experiment, in Figure 4.3, but with different values for each phase (R1=10 Ω; R2=30 Ω; R3=100 Ω; L1=10 mH; L2=30 mH; L3=100 mH).

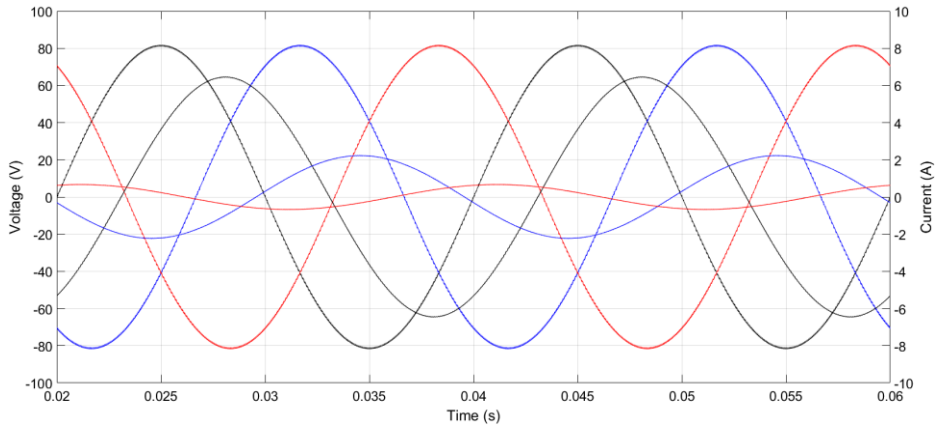
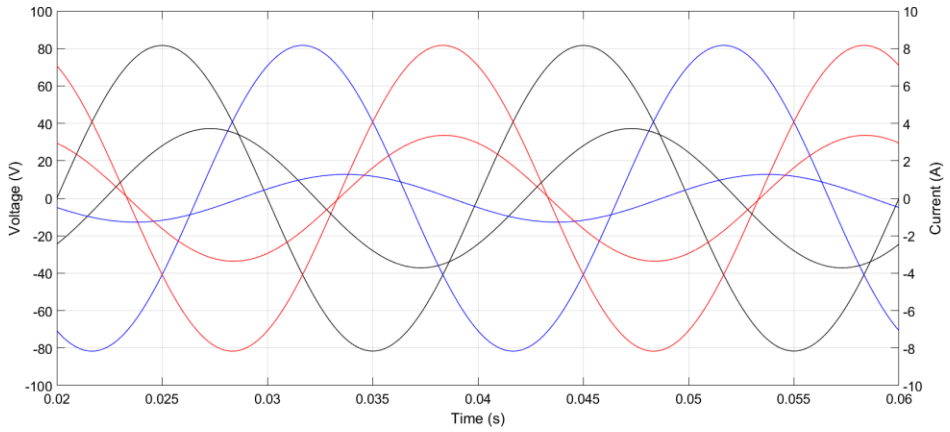
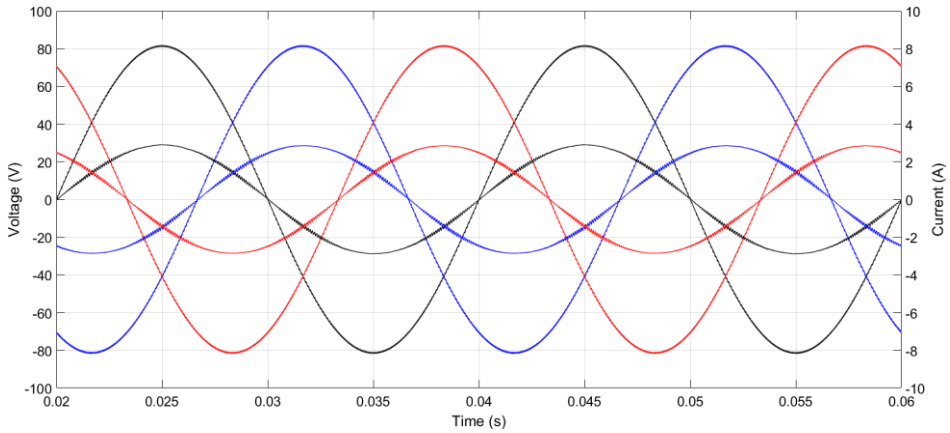



Figure 4.8 - Current (smaller) of an unbalanced RL load and grid voltages (bigger).




a) Before Compensation




b) After Compensation

Figure 4.9 - Grid voltages (bigger) and currents (smaller) before (a) and after (b) compensation for an unbalanced RL load.

As previously observed, the converter is able to significantly reduce the reactive power present in the grid but adds ripple to the current.

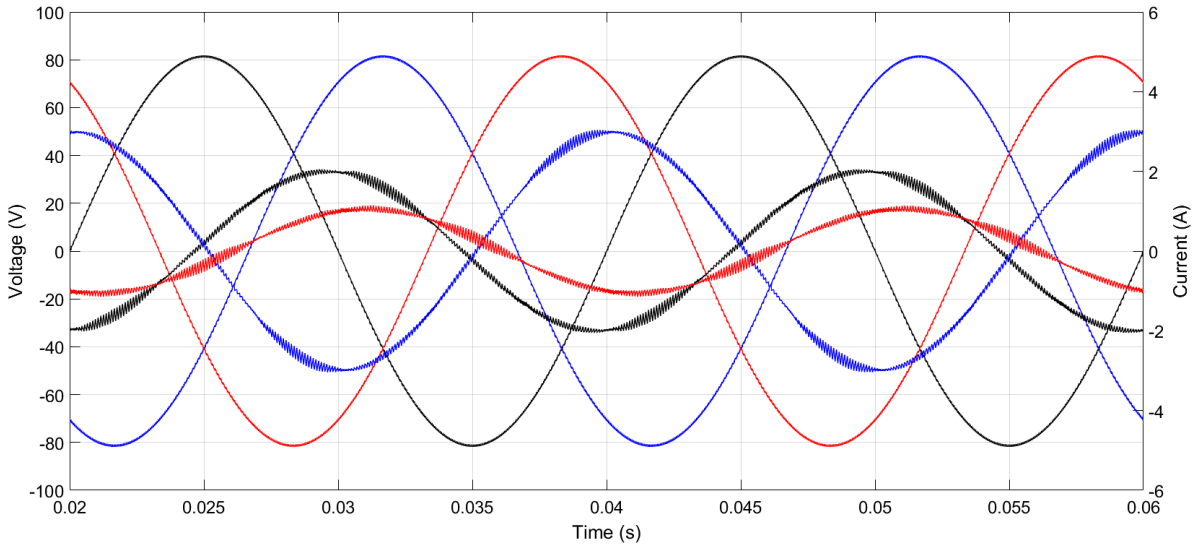
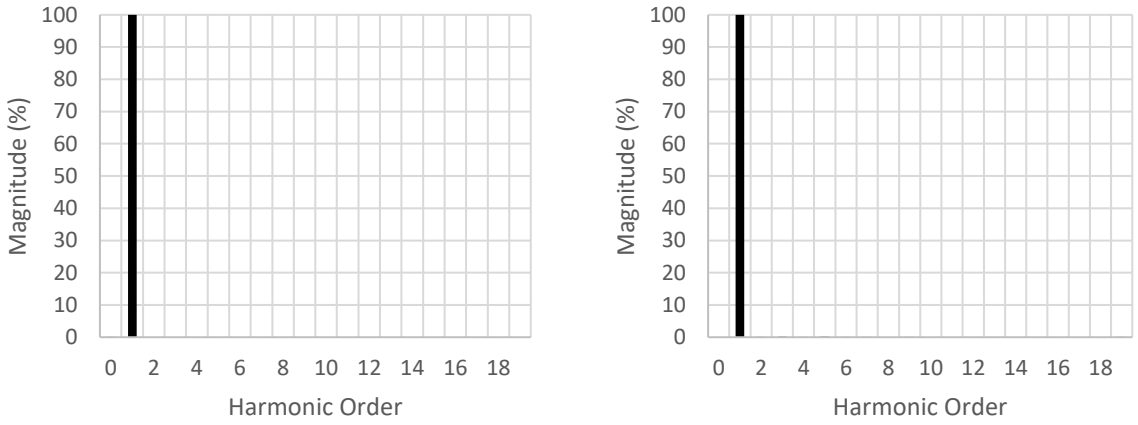



Figure 4.10 - Currents (smaller) generated by the power converter for an unbalanced RL load and grid voltages (bigger).




a) Before compensation

b) After compensation

Figure 4.11 – Harmonic spectrum of grid current in one phase before (a) and after (b) compensation of an unbalanced RL load.

Table 4.2 - THD of the current in one phase of the grid, active and reactive power on the grid before and after compensation of an unbalanced RL load.

| | Before compensation | After compensation |
|---|---|---|
| Grid active power (W) | 293 | 350 |
| Grid reactive power (var) | 134 | 3 |
| Grid current THD (%) | 0.01 | 1.92 |

### 4.2.3 – Experiment 3 – Rectified resistive load with an input impedance

The third experiment was conducted for a balanced, rectified R load with an input inductance (R=50 Ω; L=15 mH).

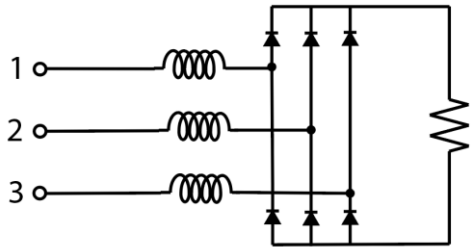



Figure 4.12 – Schematic of the load used in the third experiment.

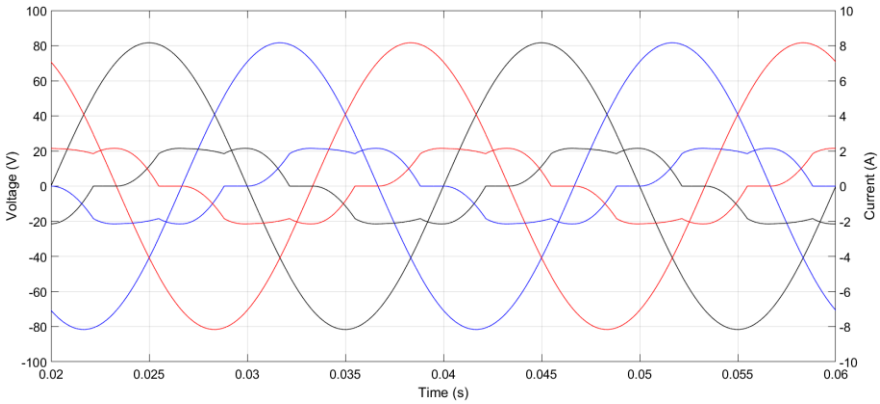
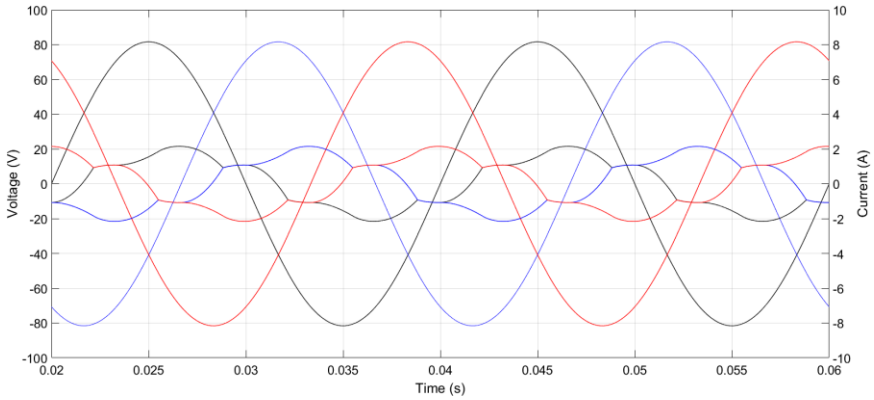
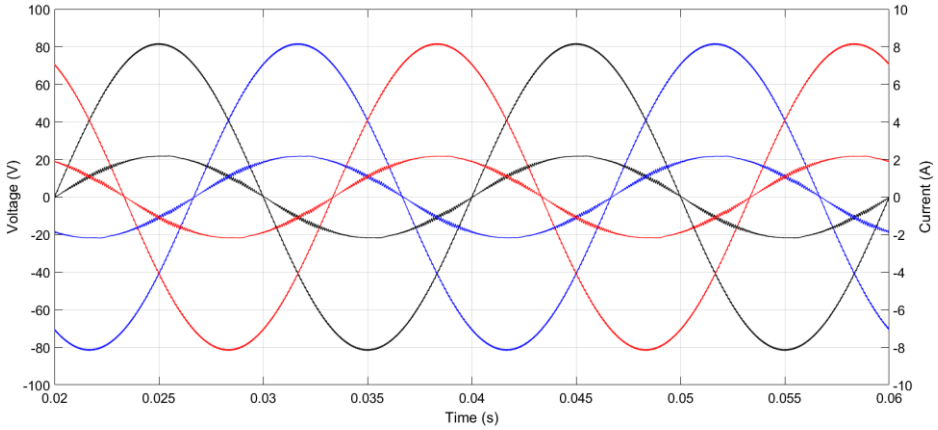



Figure 4.13 – Current (smaller) of a rectified RL load and grid voltages (bigger).

From observing Figure 4.14 and as previously stated, the converter is able to significantly reduce the reactive power present in the grid. The converter is also able to eliminate most of the harmonic content.




a) Before Compensation




b) After Compensation

Figure 4.14 - Grid voltages (bigger) and currents (smaller) before (a) and after (b) compensation for a rectified RL load.

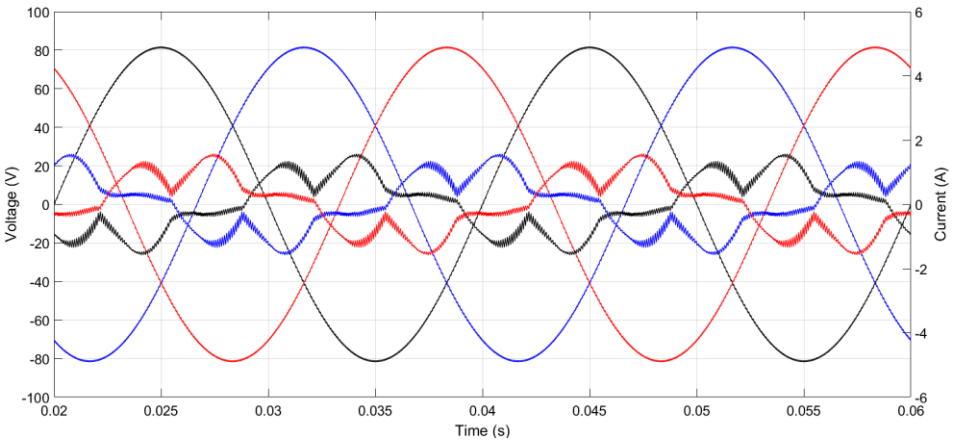
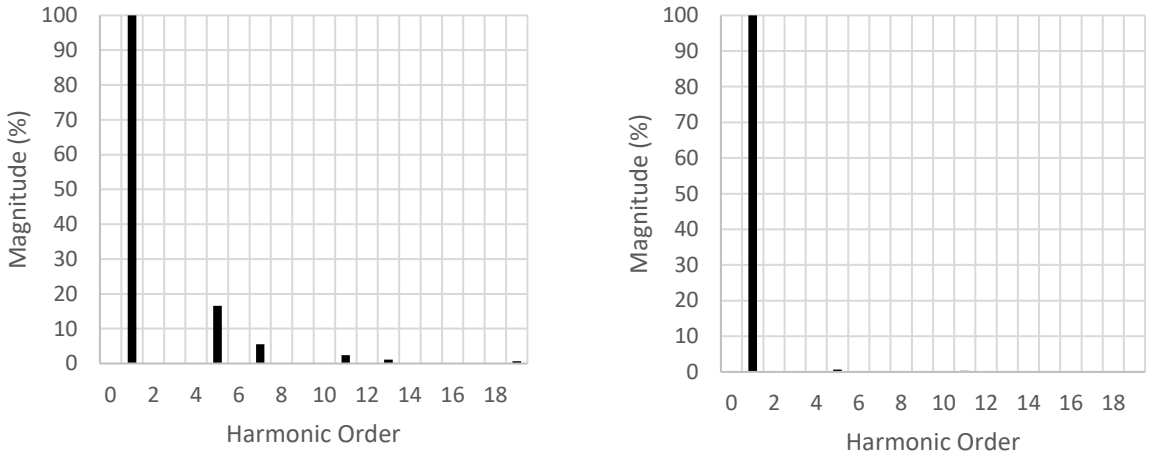



Figure 4.15 – Currents (smaller) generated by the power converter for a rectified RL load and grid voltages (bigger).

From observing Figure 4.16, it is noticeable that the converter could eliminate most of the harmonic content generated by the rectified RL load, namely the fifth, seventh, eleventh and thirteenth harmonic orders. In Table 4.3, we can observe that, for a rectified RL load, the converser is able to significantly reduce THD levels in the current of the grid as well as the reactive power injected by the grid.




a) Before compensation

b) After compensation

Figure 4.16 – Harmonic spectrum of grid current in one phase before (a) and after (b) compensation of a rectified RL load.

Table 4.3 – THD of the current in one phase of the grid, active and reactive power on the grid before and after compensation of a rectified RL load.

| | Before compensation | After compensation |
|---|---|---|
| Grid active power (W) | 212 | 266 |
| Grid reactive power (var) | 107 | 2 |
| Grid current THD (%) | 17.76 | 2.85 |

### 4.2.4 – Experiment 4 – Unbalanced rectified resistive load with an input impedance

The load used in the fourth experiment is the same as the one used in the third experiment but with a disconnected phase.

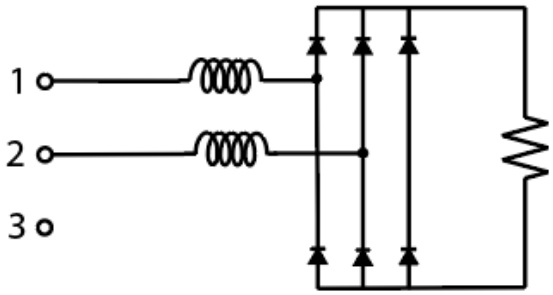



Figure 4.17 – Schematic of the load used in the fourth experiment.

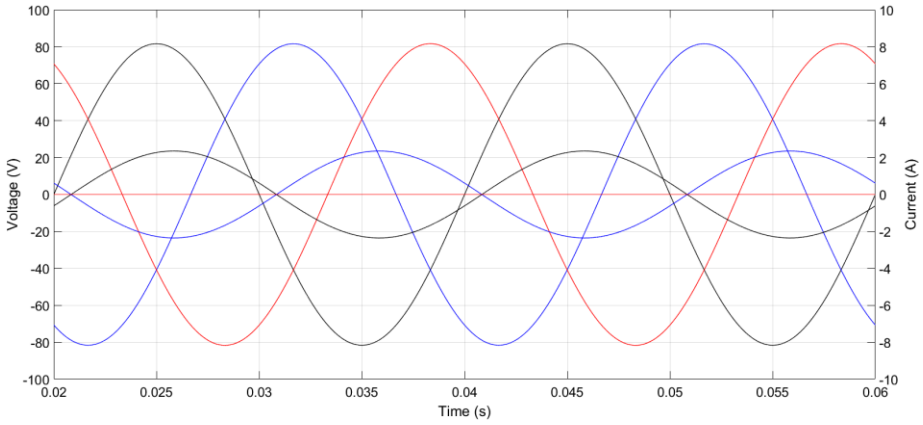
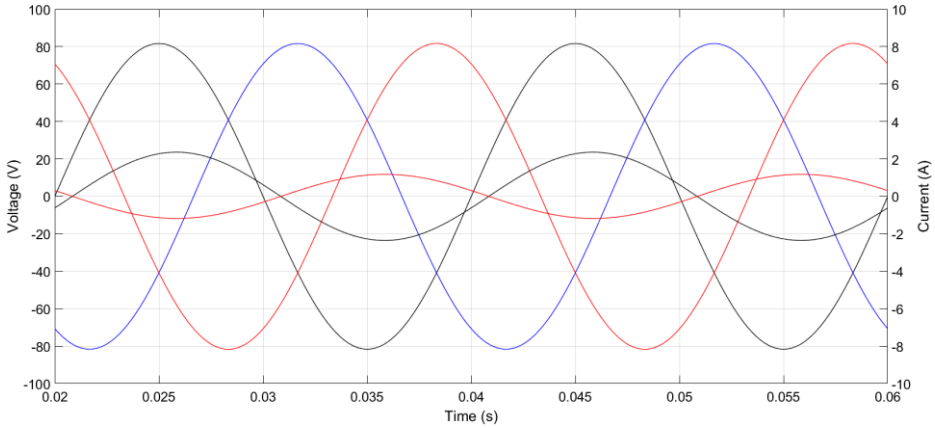
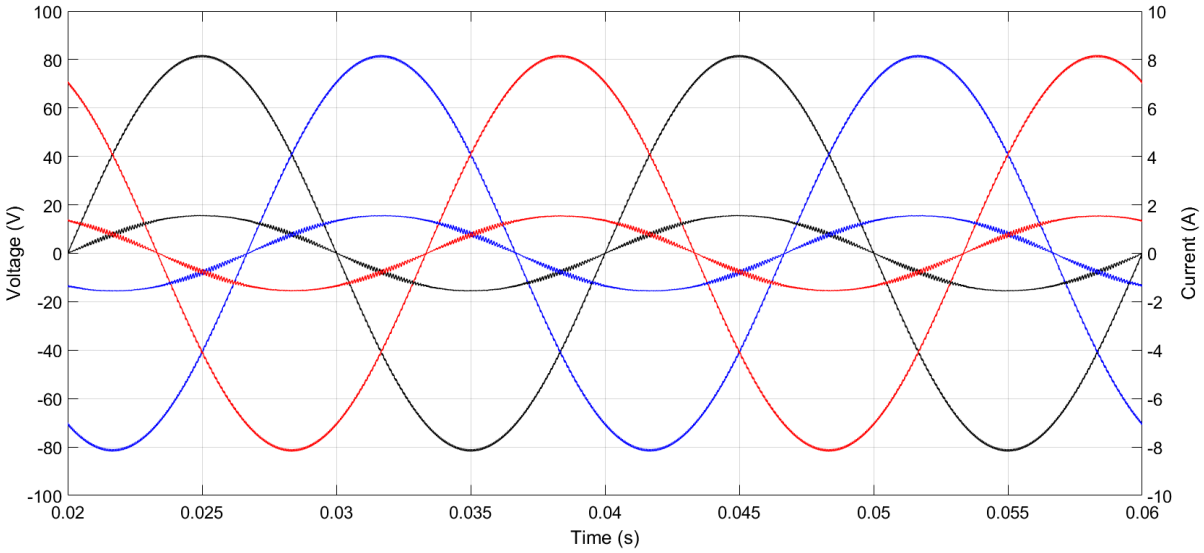



Figure 4.18 – Current (smaller) of an unbalanced rectified RL load and grid voltages (bigger).




a) Before Compensation




b) After Compensation

Figure 4.19 – Currents (smaller) generated by the power converter for an unbalanced rectified RL load and grid voltages (bigger).

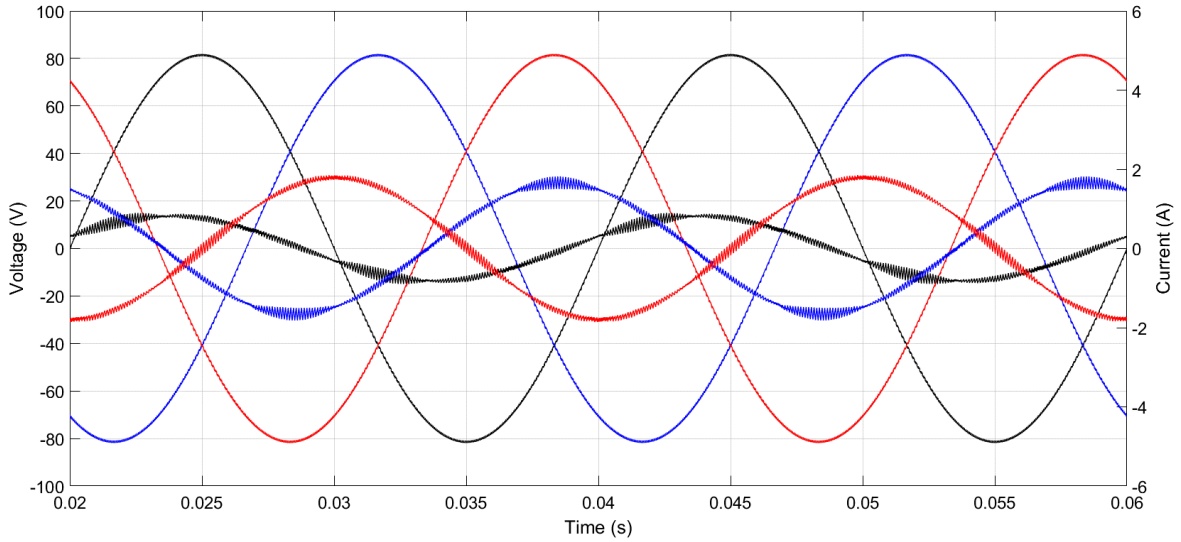
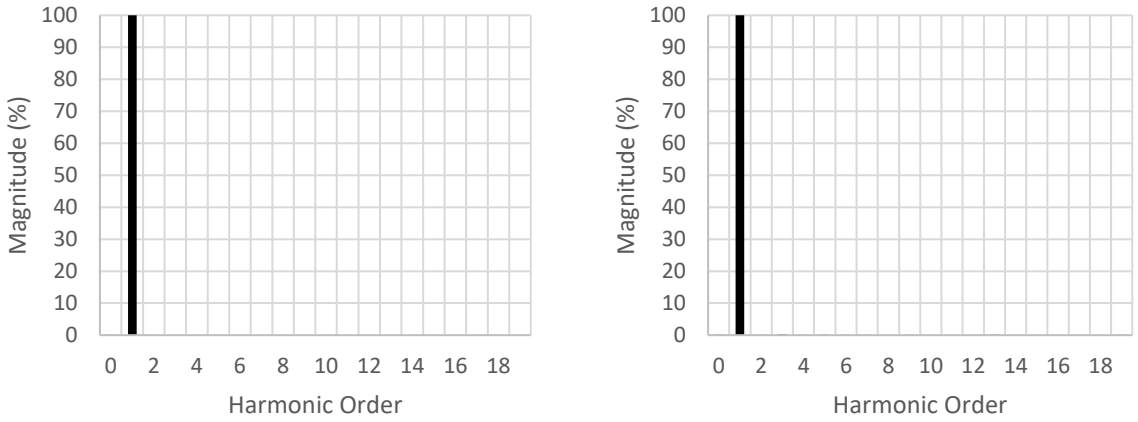



Figure 4.20 – Currents (smaller) generated by the power converter for an unbalanced rectified RL load and grid voltages (bigger).

Similarly to what was observed in experiments one and two, for an unbalanced rectified RL load, the converter is able to synchronize the currents with the voltages in the grid, reducing the reactive power significantly but adding ripple and worsening THD levels.




a) Before compensation b) After compensation

Figure 4.21 – Harmonic spectrum of grid current in one phase before (a) and after (b) compensation of an unbalanced rectified RL load.

Table 4.4 – THD of the current in one phase of the grid, active and reactive power on the grid before and after compensation of an unbalanced rectified RL load.

| | Before compensation | After compensation |
|---|---|---|
| Grid active power (W) | 140 | 190 |
| Grid reactive power (var) | 38 | 2 |
| Grid current THD (%) | 0.01 | 3.75 |

## 4.2.5 – Experiment 5 – DC voltage control

In the following experiment, the loads were disconnected from the system and the DC current, $i_{dc}$, was increased by 0.5A (from 0.5A to 1A) in order assess the DC voltage control functionality.

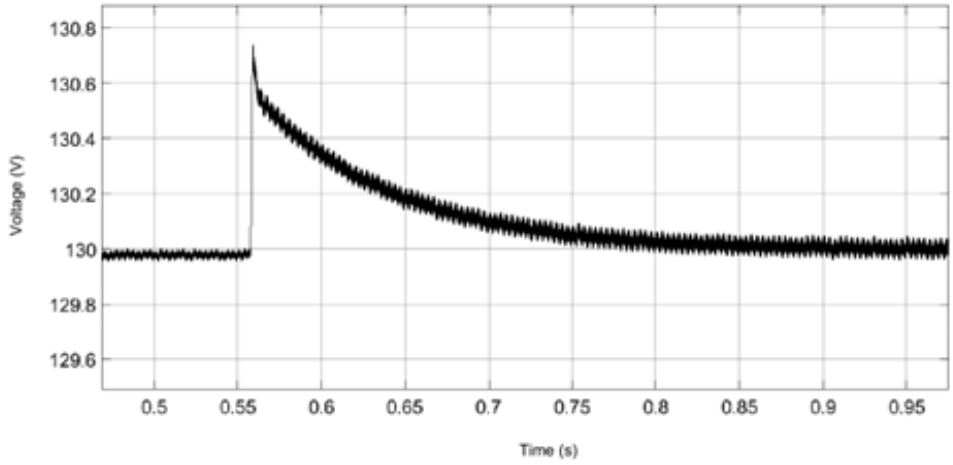



Figure 4.22 – DC voltage control for a step of 0.5A in the DC current

As it is possible to notice, for a step of 0.5A, the DC voltage overshot for about 0.7V but returned to the set point value in around 250 ms.

### 4.2.6 – Experiment 6 – Power flow

For the last experiment, the DC current was increased by 2A (from 2A to 4A) in order to visualize the power flow direction change from grid-system to system-grid.

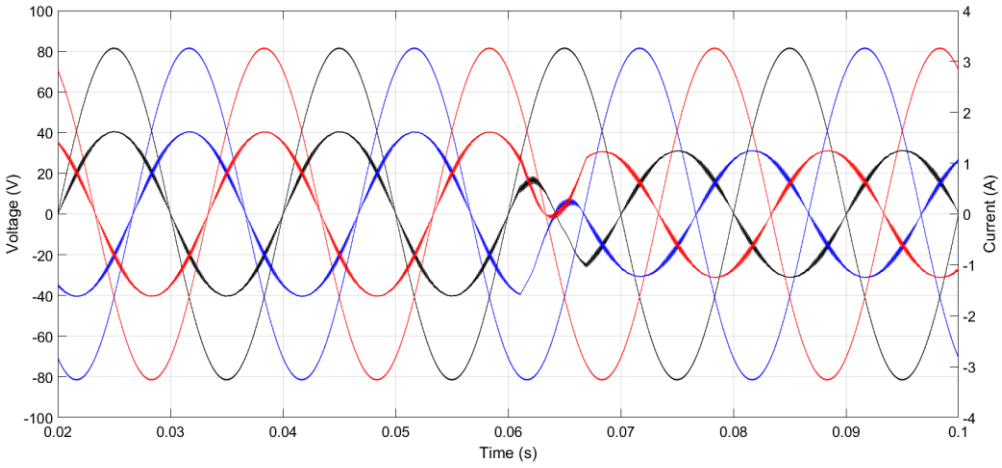



Figure 4.23 - Grid voltages (bigger) and currents (lower) before and after a step of 7 A in the DC current, for a 100 Ω resistive load.

From the image above, it is possible to visualize the change in position of the currents in relation to their respective voltages, signalling the shift in power flow after the step up of current.

# Chapter 5

# Laboratorial implementation

Due to the high number of mathematical operations, it was only possible to make some preliminary tests in the laboratory:

- A closed-loop inverter controlled by SVPWM, at the image of the main project's system;
- With the grid connected to different loads via the transformer, it was also possible to produce reference currents very similar to the ones obtained via simulation.

## 5.1 – Hardware used

The experimental system's architecture was obtained from the simulations schematic (Figure 4.1). In the laboratory, the grid's voltages are given by an autotransformer which was fixed at 30 $V_{RMS}$. The autotransformer is connected to the primary winding of the three-winding transformer. The other two windings are each connected to the loads and the converter. The primary winding has double the number of turns as the other two windings, resulting in a 2:1 winding ratio.

In order to measure both the voltages from the grid and the currents from the load, an isolated voltage and current sensing module is used. This module is fitted with multiple USM-3IV from Taraz Technologies which condition the signal. This data is then sent to the microcontroller unit – the STMicroelectronics' NUCLEO-G491RE – via 5V unipolar outputs. The DC voltage and the converter's currents are all measured locally in the three-phase power electronic converter – STEVAL-IHM023V3 from STMicroelectronics – and sent for the MCU via 5V unipolar outputs.

All the values sent to the MCU can then be visualized on a computer, at a frequency of 10 kHz, through a designated graphical interface in STMicroelectronics' STMStudio.

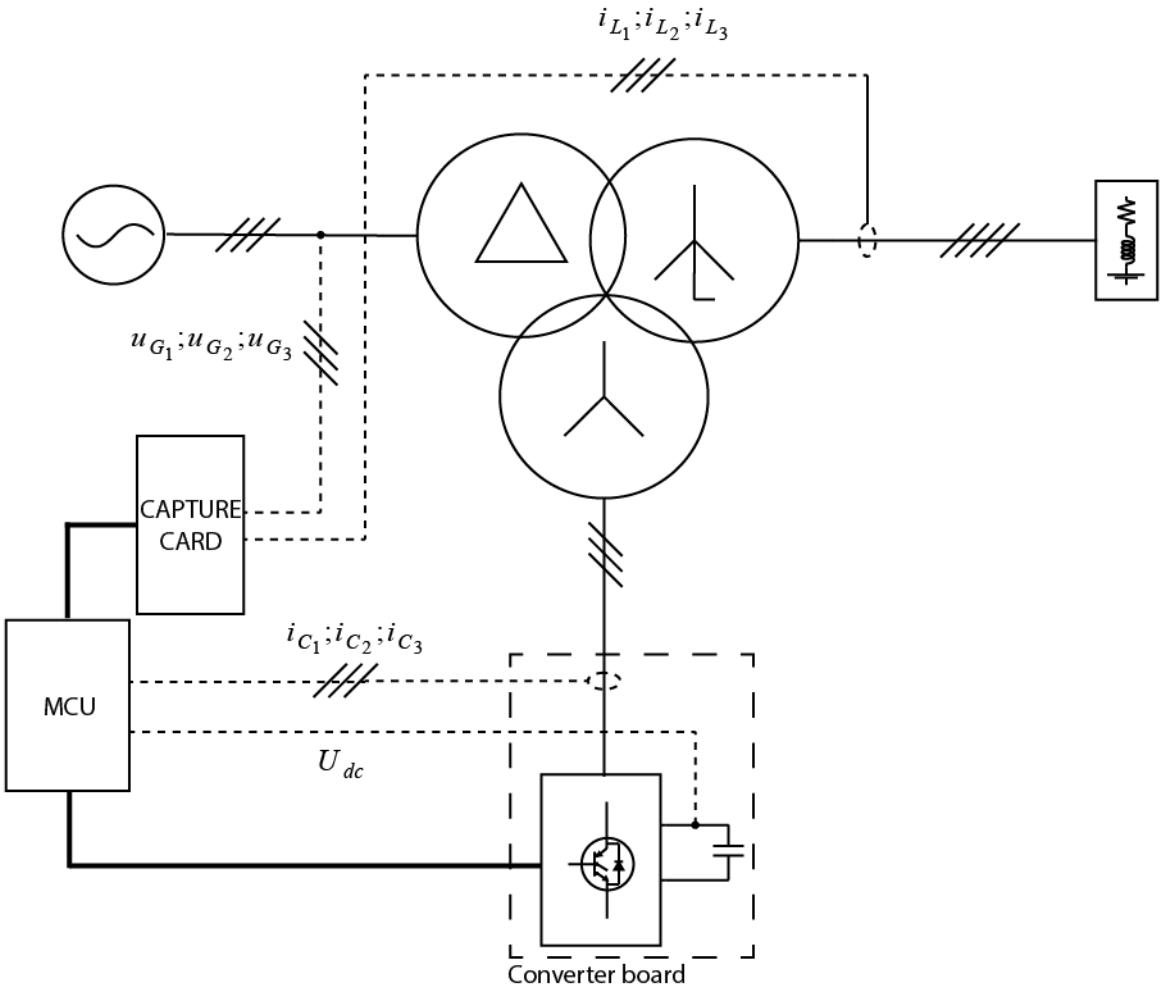



Figure 5.1 - Global schematic of the laboratory's setup.

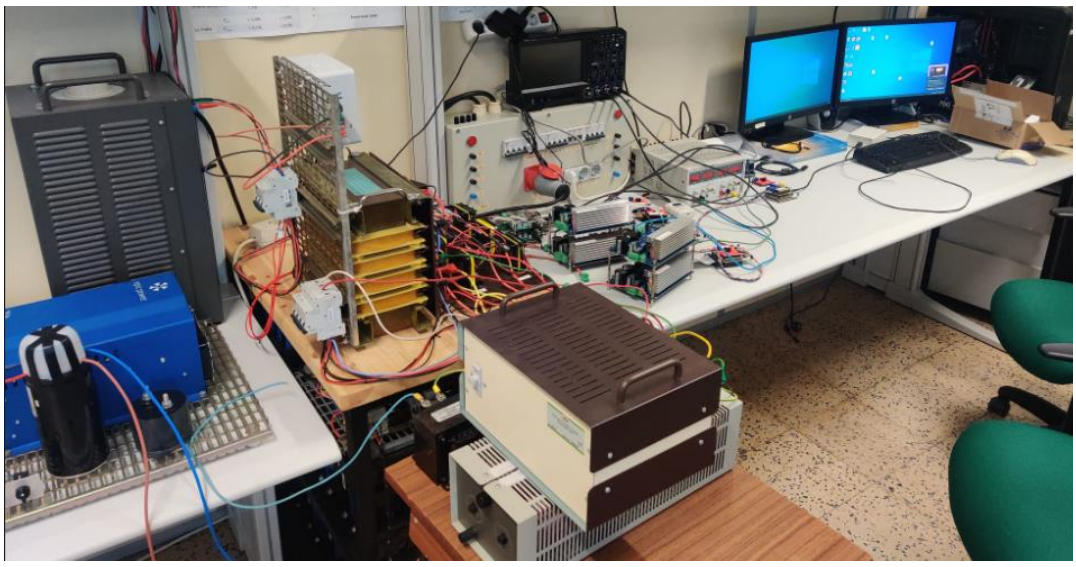


Figure 5.2 – Picture of the laboratorial implementation.

## 5.2 – Software implementation

The control algorithm for the active power filter, obtained in Chapter 3 , was implemented in the STMicroelectronics' microprocessor in C++ which files are in Attachment A. Table 5.1 summarises all the source and header files and their function.

Table 5.1 – Summary of the software files.

| File name | Function |
|---|---|
| app.h | Declaration of variables and structures for app.c |
| app.c | Main file which contains the control algorithm |
| ctrl_lib.h | Declaration of variables and structures for ctrl_lib.c |
| ctrl_lib.c | Definition a low pass filter and a PI controller |
| defs.h | Attribution of definitions to the system's constants, inputs and outputs |
| irq.h | Declaration of variables and structures for irq.c |
| irq.c | Function calling for interrupt requests |
| SVPWM.h | Declaration of variables and structures for SVPWM.c |
| SVPWM.c | Definition of the SVPWM algorithm |
| trans.h | Declaration of variables and structures for trans.c |
| trans.c | Definition of the transformations between 123, αβ, and dq reference frames |

## 5.3 – Experimental results

### 5.3.1 – SVPWM algorithm and current control loop

In order to test the switching algorithm and the control methods, a DC/AC inverter was implemented. A controlled voltage source was connected at the DC side of the converter, at 60V. The inverter's currents are controlled by a closed-loop control system and the setpoint of current was established at 0.5 $A_{pk}$.

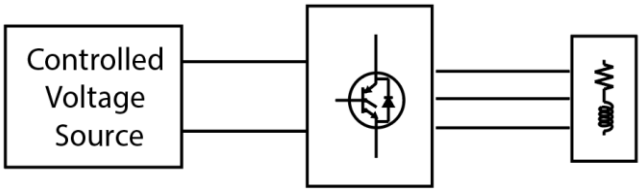



Figure 5.3 – Schematic of the system used to test the switching algorithm and current control loop.

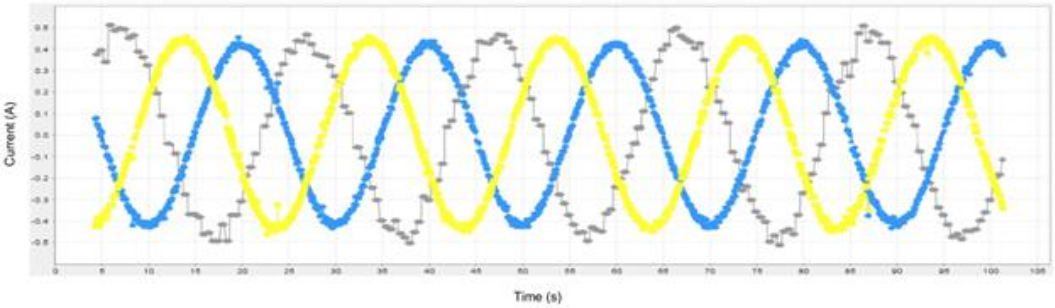



Figure 5.4 – Closed loop currents from the inverter for a RL load with a set point of 0.5 A of amplitude.

Noticeably, the controller is able to generate three currents acceptably phased from each other and with minimal error of amplitude.

### 5.3.2 – Active Power Filter

The system was also tested for its APF capabilities where the reference currents from the simulation were compared to the ones determined by the MCU. The reason for this is to find

out if the MCU can produce the reference currents. For these tests, voltage at the grid side was 50 $V_{RMS}$.

On the other hand, to verify the operation of implemented APF control system on MCU, the grid currents are emulated through the sum of the instantaneous values of the load currents with the load currents.

### Load 1 – Unbalanced RL load

For the first load, phase 3 was disconnected and phases 1 and 2 with an inductance of 250mH and different resistances of 7Ω and 10Ω.

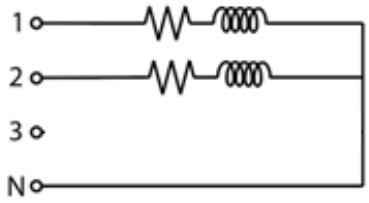



Figure 5.5 – Schematic of the unbalanced RL load.

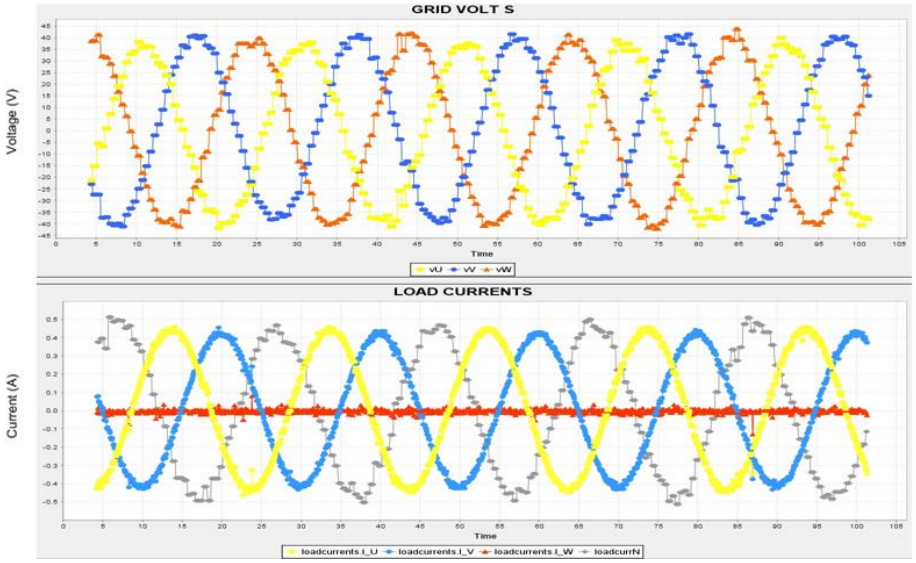



Figure 5.6 – Grid voltages and load currents in an unbalanced RL load, measured in the laboratory.

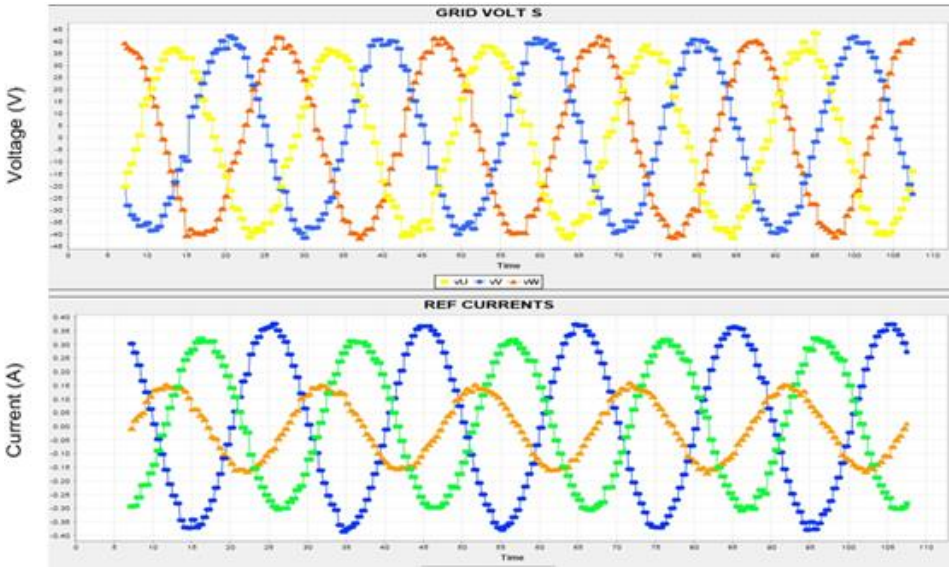



Figure 5.7 - Grid voltages and the reference currents for an unbalanced RL load, determined by the microprocessor.

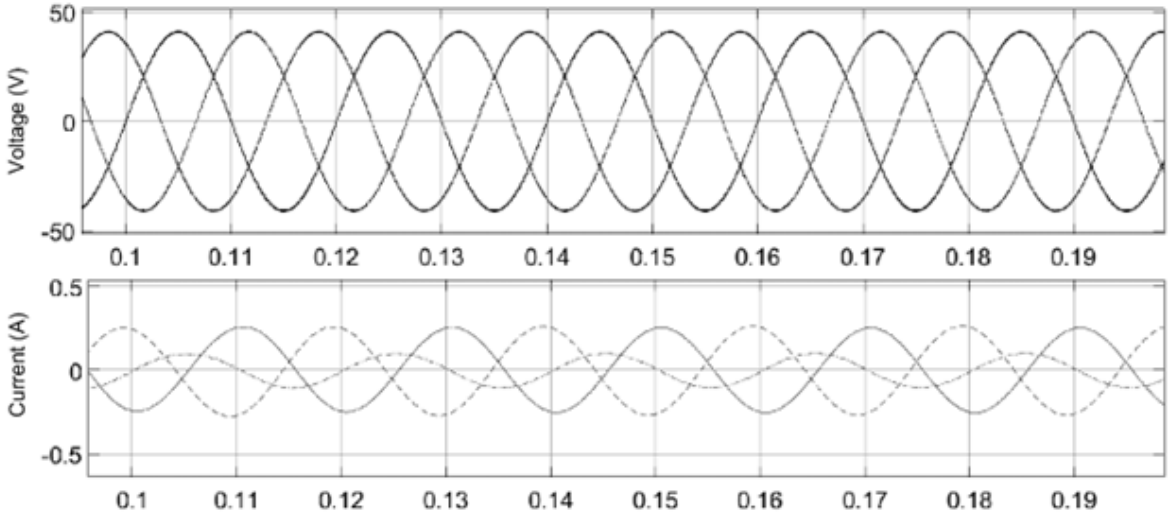



Figure 5.8 - Grid voltages and the reference currents for an unbalanced RL load, obtained via simulation.

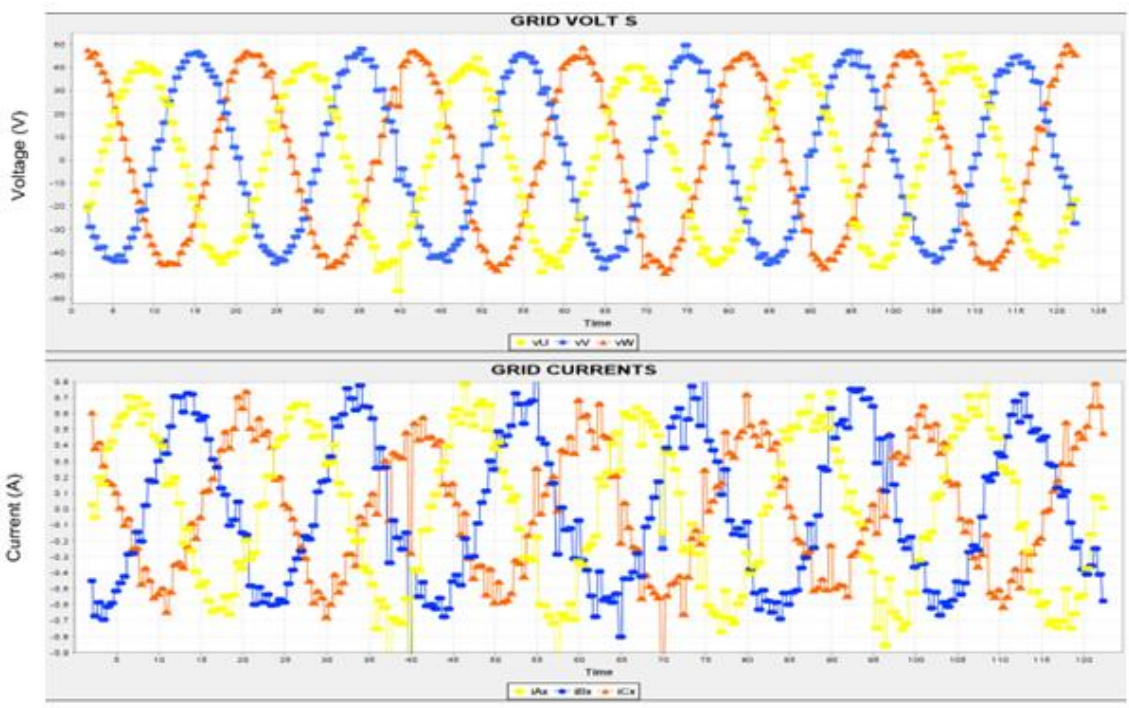



Figure 5.9 – Grid voltages and the instantaneous summation of the currents in the load and the reference currents for an unbalanced RL load, obtained by the microprocessor.

### Load 2 – Rectified RL load

For the second load, a rectifier was used with an input inductance of 2.5 mH and a resistor of 10 Ω.

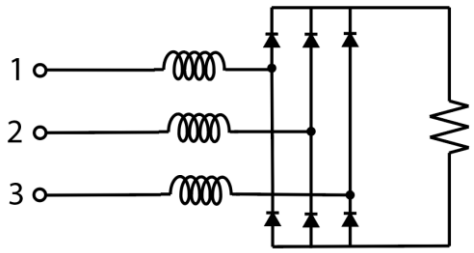



Figure 5.10 – Schematic of the rectified RL load.

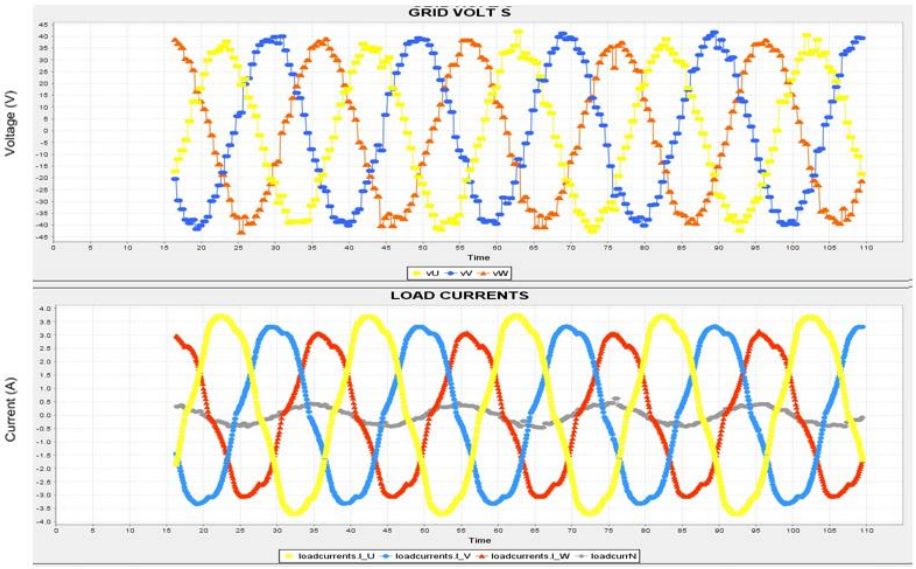



Figure 5.11 – Grid voltages and load currents in a rectified RL load, measured in the laboratory.

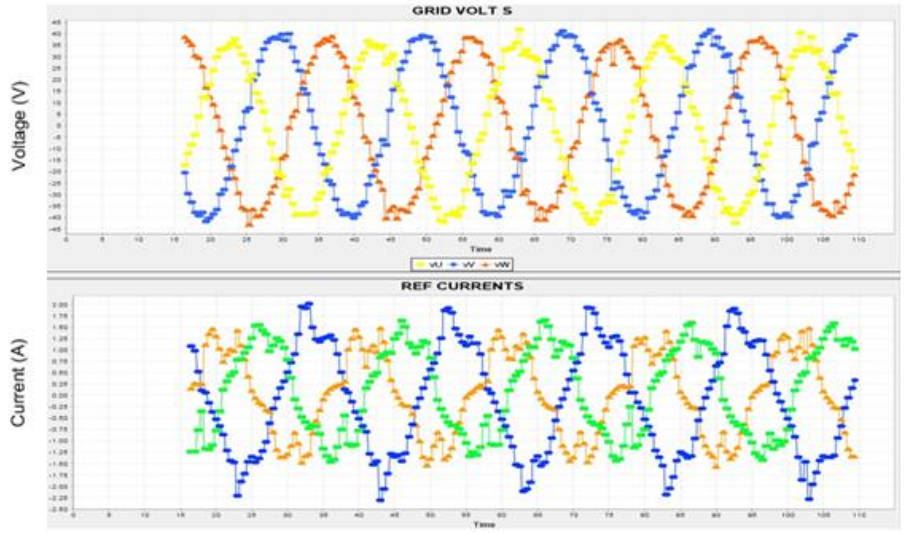



Figure 5.12 - Grid voltages and the reference currents for a non-linear R load, determined by the microprocessor.

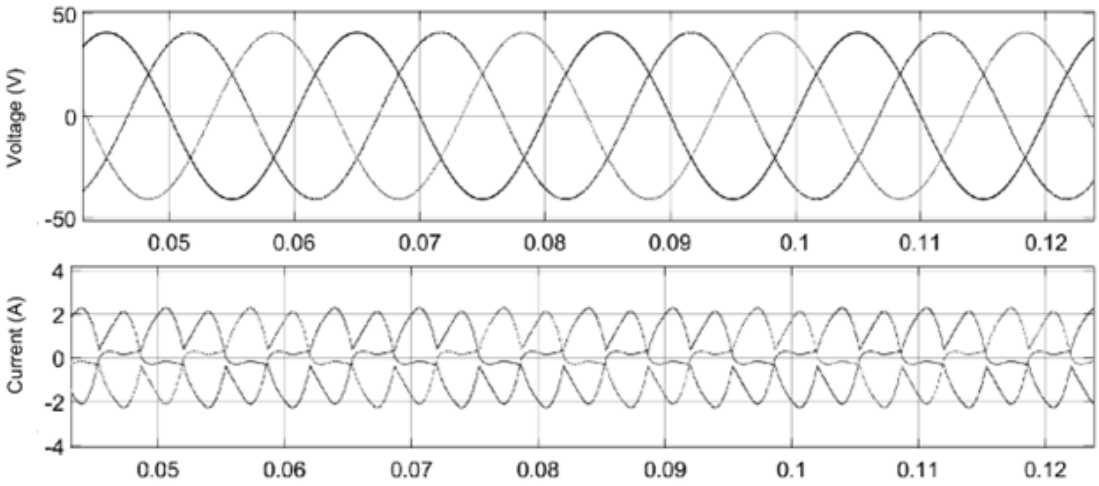



Figure 5.13 - Grid voltages and the reference currents for a non-linear R load, obtained via simulation.

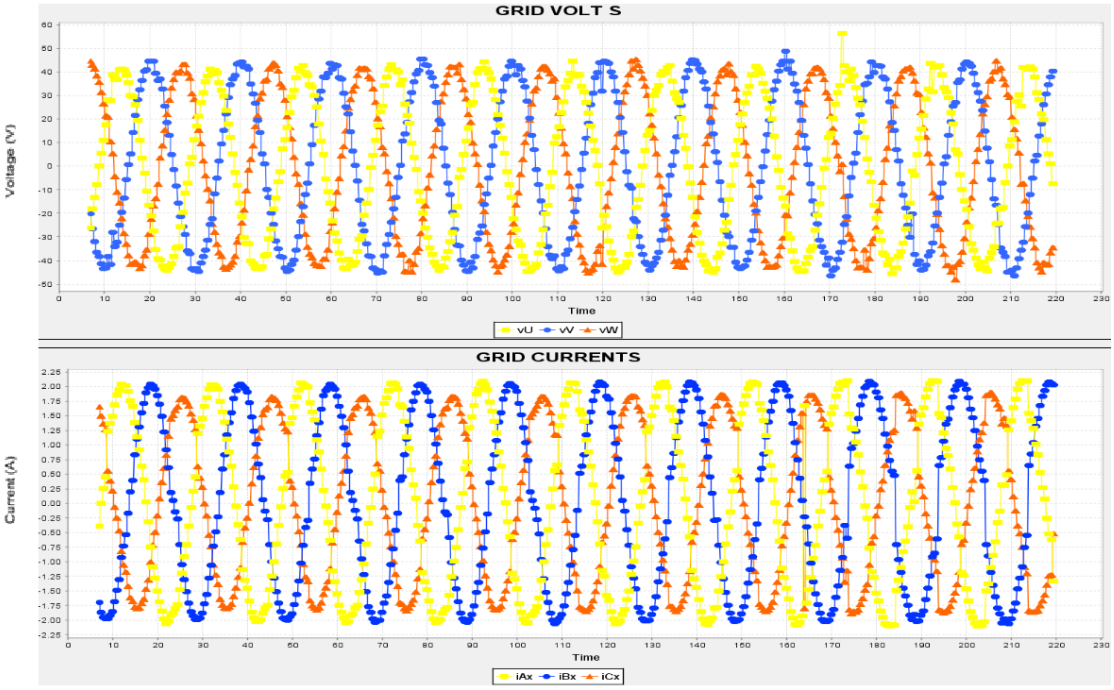



Figure 5.14 – Grid voltages and the instantaneous summation of the currents in the load and the reference currents for a rectified RL load, obtained by the microprocessor.

### Load 3 – Unbalanced rectified RL load

For the unbalanced and non-linear R load, phase 3 was disconnected from the load.

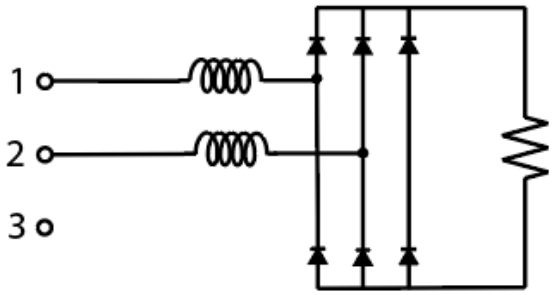



Figure 5.15 – Schematic of the unbalanced rectified load.

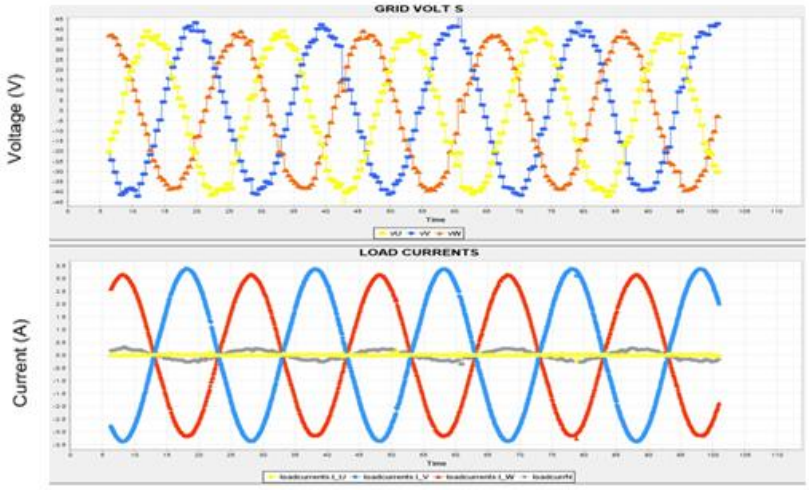



Figure 5.16 – Grid voltages and load currents in an unbalanced rectified RL load, measured in the laboratory.

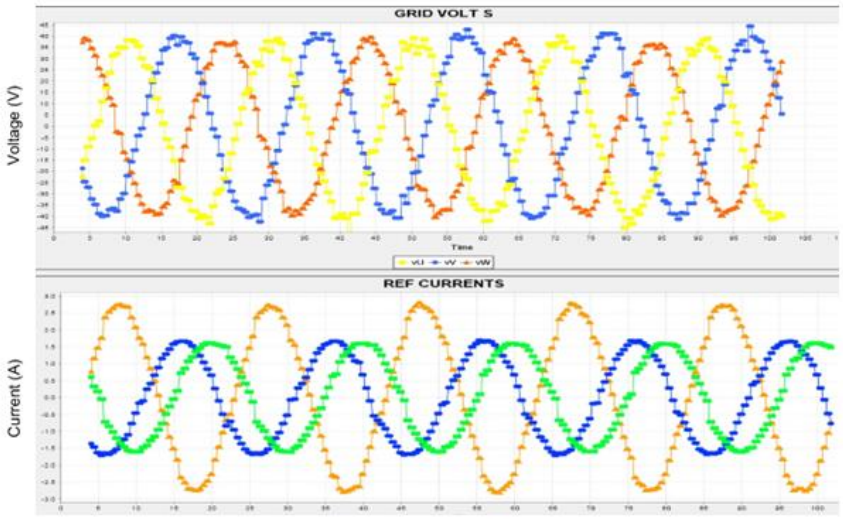



Figure 5.17 - Grid voltages and the reference currents for an unbalanced and non-linear R load, determined by the microprocessor.

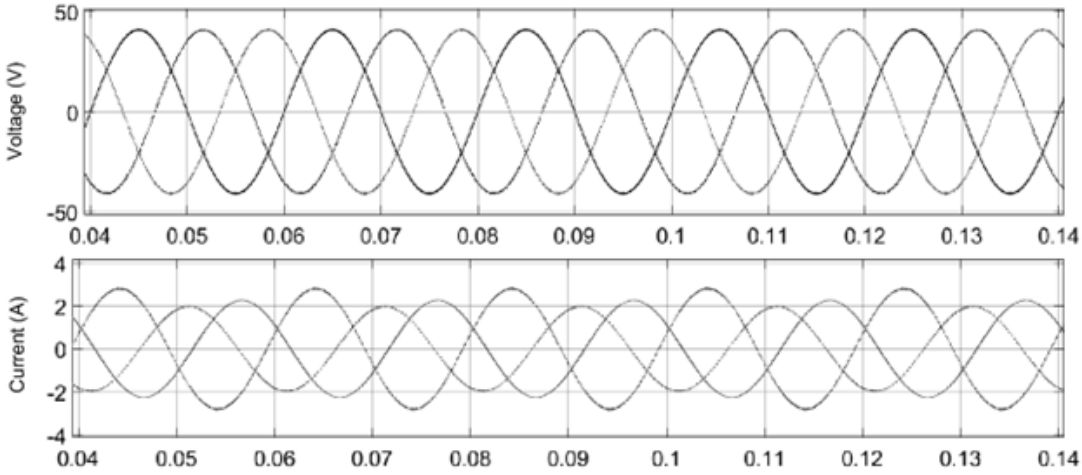



Figure 5.18 – Grid voltages (top) and the reference currents (bottom) for an unbalanced and non-linear resistive load, obtained via simulation.

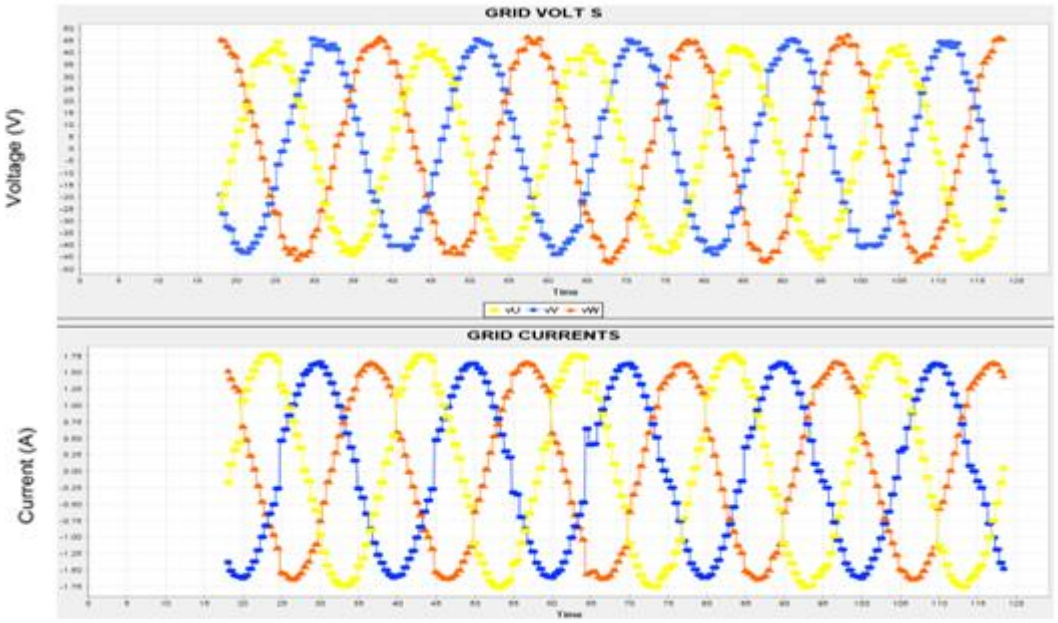



Figure 5.19 – Grid voltages and the instantaneous summation of the currents in the load and the reference currents for an unbalanced rectified RL load, obtained by the microprocessor.

From the results obtained, it is possible to visualize that the microprocessor can generate very similar reference currents to the ones obtained through the simulation. From Figure 5.9, Figure 5.14 and Figure 5.19 it is also possible to notice that the instantaneous summation of the reference currents with the load currents result in a set of three currents with a delay of around 30º (1.67 ms) which is related to the delay caused by the transformer as these currents are

obtained for the corrected angle, $\Theta'_G$. Thus, these current waveforms can be seen as the grid currents, after their amplitudes are corrected by the transformer turn ratio and phase shift.

# Chapter 6

# Conclusions and future work

## 6.1 – Conclusions

The principal motivation for this work was to demonstrate the viability of connecting a DC microgrid – which also has the function of an active power filter – onto a three-winding transformer in order to make the installation of DC microgrid into distribution transformer simpler and therefore faster while adding the benefits of having less “polluted” energy.

In this work, a mathematical model of the converter was obtained, 2 control loops for the DC voltage and for the converter currents were designed, the SVPWM switching technique was implemented, reference currents determined, and a simulation developed where the items above were tested. In this simulation, it was possible to test multiple loads connected to the system, while DC voltage is maintained and power flow from the grid inverted (system-grid). It was concluded that, for low harmonic distortion currents, the converter can worsen the THD levels – with the minimum THD value being 2% after compensation. Although the converter injects some harmonic content onto the system, it can keep it at standard-acceptable values – even for high harmonic distortion currents, where, in one case, THD was dropped from 17.76% to 2.85% – while significantly decreasing the reactive power (to below 5 Var) injected by the grid, increasing the power factor.

Experimentally, the objective was to build a prototype where simulation and real scenarios would be compared but the integration of the somewhat heavy algorithm posed some difficulties. Instead, there were two scenarios studied: one where SVPWM was tested for a DC/AC inverter in a closed loop and another for the active power filter capabilities of the converter when connected to unbalanced, non-linear loads. In these experiments, it was possible to verify the capability of the microprocessor to handle both the SVPWM algorithm in a closed loop as well as the reference current determination.

## 6.2 – Future work

Some suggestions for future work are also given:

- A different method for grid-synchronization can be beneficial to lower the flicker present when two phase voltages cross each other.
- Update the control algorithm in order to encompass voltage deregulation.
- Test a multi-level converter in order to reduce harmonic distortion injected.
- Implementation of a microprocessor which has more computational capacity.

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# ATTACHMENT A

# Software used in microprocessor

## app.h

```
#ifndef APP_H_
#define APP_H_

#include "main.h"
#include "defs.h"
#include "trans.h"

/* structure of ADC values */
typedef struct {
    uint16_t CHVrefint; /* ref voltage */
    uint16_t CH1;       /* I_U */
    uint16_t CH7;       /* I_V */
    uint16_t CH6;       /* I_W */
    uint16_t CH2;       /* I_V */
    uint16_t CH8;       /* I_W */
} ADC1data_t;

/* structure of ADC values */
typedef struct {
    uint16_t CH9;       /* Ref */
    uint16_t CH17;      /* U_1 */
    uint16_t CH11;      /* U_2 */
    uint16_t CH14;      /* U_3 */
    uint16_t CH12;      /* I_1 */
    uint16_t CH15;      /* I_2 */
    uint16_t CH5;       /* I_3 */
} ADC2data_t;


/* structure of ADC voltages [mV] */
typedef struct {
    uint16_t CHVrefint; /* ref voltage */
    uint16_t CH1;       /* I_U */
    uint16_t CH7;       /* I_V */
    uint16_t CH6;       /* I_W */
    uint16_t CH2;       /* I_W */
    uint16_t CH8;       /* I_W */
} ADC1voltages_t;

/* structure of ADC values */
typedef struct {
    uint16_t Ref;       /* Ref */
    uint16_t CH17;      /* U_1 */
    uint16_t CH11;      /* U_2 */
    uint16_t CH14;      /* U_3 */
    uint16_t CH12;      /* I_1 */
    uint16_t CH15;      /* I_2 */
    uint16_t CH5;       /* I_3 */
} ADC2voltages_t;
```

```c
/* structure of currents [A] */
typedef struct {
    float I_U; /* phase U current */
    float I_V; /* phase V current */
    float I_W; /* phase W current */
} currents_t;

/* structure of currents [A] */
typedef struct {
    float U_U; /* phase U current */
    float U_V; /* phase V current */
    float U_W; /* phase W current */
} voltages_t;

/* structure of measured voltages [V] and currents [A] */
typedef struct {
    float u1;
    float u2;
    float u3;
    float i1;
    float i2;
    float i3;
} meas_t;

/* structure of filtered voltages [V] and currents [A] */
typedef struct {
    float u1;
    float u2;
    float u3;
    float i1;
    float i2;
    float i3;
} out_t;


/*
 * function prototypes
 */
void hw_init();
void sw_init();
void loop();
void process_data_ADC1();
void process_data_ADC2();
void control_task();
void measToMaster(void);
void processMsg(uint8_t *pRxBuffer);

#endif /* APP_H_ */
```

## app.c

```
#include "app.h"
#include "ctrl_lib.h"
#include "SVPWM.h"
#include "_com.h"
#include "CAN.h"
#include "usart.h"
#include "math.h"
#include "trans.h"


extern UART_HandleTypeDef huart2;

static ADC1data_t ADC1data;           /* structure of ADC readings [12-bit] */
static ADC1voltages_t ADC1voltages;     /* structure of ADC voltages [mV] */

static ADC2data_t ADC2data;           /* structure of ADC readings [12-bit] */
static ADC2voltages_t ADC2voltages;     /* structure of ADC voltages [mV] */
static currents_t currents;           /* structure of currents [A] */
static currents_t loadcurrents;           /* structure of currents [A] */
static voltages_t gridvoltages;           /* structure of currents [A] */

static float R_NTC; /* NTC resistance for temperature calculation [Ohm] */
static float Vbus;        /* Vbus */
static float temp;        /* Temperature */
float pllV = 0, pllU = 0, pllW = 0;
int pll1 = 0, pll2 = 0;;
float sum;
float vU, vV, vW, theta;

static LowPassFlt_Instance_t fltU, fltI;
static SVPWM_instance_t SVPWM;        /* SVPWM modulator instance */
static PIRegulator_Instance_t PIdc, PId, PIq; /* current regulator instance */

float lpu, lpv, lpw, theta1, theta2,theta_M, idC, iqC;
float iaspi, ibspi;
float iLo = 0, iA, iB, iC, iAx, iBx, iCx, iLd, iLq, Vasp, Vbsp;
float idug, iaug, ibug;
float idspmean = 0;
float imaxsp = 0.5;
int bool1, bool2;
float iAsp, iBsp, iCsp, iasp, ibsp, idsp, iqsp, idspPI, iaspPI, ibspPI, amp, t = 0;
float pll1a, pll1b;
float idread;
float errorDC = 0, errorD, errorQ, Vd, Vq;
//float sine[200] = {1.0000,0.9995,0.9980,0.9956,0.9921,0.9877,0.9823,0.9759,0.9686,0.9603,
float iaread = 0, ibread = 0;
float sintheta[200] = {0.00000,0.03141,0.06279,0.09411,0.12533,0.15643,0.18738,0.21814,0.24
float cost, sint = 0;
//float theta[1000] = {-1.530818,-1.530738,-1.530657,-1.530577,-1.530496,-1.530414,-1.53033
float asin_t[1000] = {-1.5708,-1.5075,-1.4813,-1.4612,-1.4442,-1.4293,-1.4157,-1.4033,-1.39

float acos_t[1000] = {3.141592654,3.078336555,3.052120093,3.031993296,3.015017068,3.000053
float costheta[200] = {1.00000,0.99951,0.99803,0.99556,0.99211,0.98769,0.98229,0.97592,0.96
static CAN_meas_t CAN_meas; /* measurement data to send over CAN bus */
static CAN_ctrl_t CAN_ctrl; /* control data received over CAN bus */
```

```
float acos_t[1000] = {3.141592654,3.078336555,3.052120093,3.031993296,3.015017068
float costheta[200] = {1.00000,0.99951,0.99803,0.99556,0.99211,0.98769,0.98229,0.
static CAN_meas_t CAN_meas; /* measurement data to send over CAN bus */
static CAN_ctrl_t CAN_ctrl; /* control data received over CAN bus */
int xd = 0;
float irefA = 0, irefB = 0, irefC = 0;

int cnt_alpha_aux = 0;
float array_alpha_aux[200] = {0};

int cnt_beta_aux = 0;
float array_beta_aux[200] = {0};
/*
 * calculate temperature from NTC resistance
 */
float calcTemp(float R)
{
    float tmp;
    tmp = log(R / R0_NTC);
    tmp = 1.0f / T0_NTC + (1.0f / B_NTC) * tmp;
    tmp = 1.0f / tmp - 273.15f;
    return tmp;
}


/*
 * initialize hardware (MCU peripherals)
 */
void hw_init()
{
    /* initialize DMA1 CH1 to transfer values from ADC1 to memory */
    LL_DMA_SetMemoryAddress(DMA1, LL_DMA_CHANNEL_1, (uint32_t)&ADC1data);
    LL_DMA_SetPeriphAddress(DMA1, LL_DMA_CHANNEL_1, (uint32_t)&ADC1->DR);
    LL_DMA_SetDataLength(DMA1, LL_DMA_CHANNEL_1, 6);
    LL_DMA_ClearFlag_TC1(DMA1);
    LL_DMA_EnableIT_TC(DMA1, LL_DMA_CHANNEL_1);
    LL_DMA_EnableChannel(DMA1, LL_DMA_CHANNEL_1);

    /* calibrate ADC1 */
    LL_ADC_StartCalibration(ADC1, LL_ADC_SINGLE_ENDED);
    while (LL_ADC_IsCalibrationOnGoing(ADC1));

    /* initialize and run ADC1 */
    LL_ADC_Enable(ADC1);
    LL_ADC_REG_StartConversion(ADC1);

    /* initialize TIM1 for generating PWM and triggering ADC conversions */
    LL_TIM_EnableCounter(TIM1);
    LL_TIM_CC_EnableChannel(TIM1, PWM_UH | PWM_UL | PWM_VH | PWM_VL |
            PWM_WH | PWM_WL | PWM_ADC_TRIG);
    LL_TIM_EnableAllOutputs(TIM1);

    /* initialize DMA1 CH2 to transfer values from ADC2 to memory */
    LL_DMA_SetMemoryAddress(DMA1, LL_DMA_CHANNEL_2, (uint32_t)&ADC2data);
    LL_DMA_SetPeriphAddress(DMA1, LL_DMA_CHANNEL_2, (uint32_t)&ADC2->DR);
```

```
    LL_DMA_SetDataLength(DMA1, LL_DMA_CHANNEL_2, 7);
    LL_DMA_ClearFlag_TC2(DMA1);
    LL_DMA_EnableIT_TC(DMA1, LL_DMA_CHANNEL_2);
    LL_DMA_EnableChannel(DMA1, LL_DMA_CHANNEL_2);

    /* calibrate ADC2 */
    LL_ADC_StartCalibration(ADC2, LL_ADC_SINGLE_ENDED);
    while (LL_ADC_IsCalibrationOnGoing(ADC2))
        ;

    /* enable and run ADC2 */
    LL_ADC_Enable(ADC2);
    LL_ADC_REG_StartConversion(ADC2);

    /* enable TIM6 to trigger ADC conversions */
    LL_TIM_EnableCounter(TIM6);


    /* enable converter */
    GPIOA->ODR |= SHUTDOWN_Pin;

    /* bypass relay */
    GPIOC->ODR |= NTC_BYPASS_Pin;

    /* configure and start CAN */
#ifdef CAN_EN
    CAN_Config();
#endif /* CAN_EN */
}

/*
 * initialize software
 */
void sw_init()
{
    /* sample period */
    fltU.Ts = fltI.Ts = (float)((TIM6_PSC + 1) * (TIM6_ARR + 1) /
            (float)SystemCoreClock);

    /* filter time constants [s] */
    fltU.Tau = 0.5e-3;
    fltI.Tau = 3;

    /* initialize filter instances */
    LowPassFlt_Init(&fltU);
    LowPassFlt_Init(&fltI);

    /* initialize SVPWM modulator */
    SVPWM.mag = 0.0f;
    SVPWM.theta = 0.0f;

    /* Define DC controller`*/
    PIdc.Ts = (float)((TIM1_ARR + 1) / (0.5f * (float)SystemCoreClock));
    PIdc.Ti = 0.0033f * 2; //Ki = Ts/Ti --- Ts = (~~1e-4)
```

```
    PIdc.Kp = 0.030f;
    PIdc.limH = 3;
    PIdc.limL = -3;
    PIRegulator_Init(&PIdc);

    /* Define dq axis controller`*/
    PId.Ts = PIq.Ts = (float)((TIM1_ARR + 1) / (0.5f * (float)SystemCoreClock));
    PId.Ti = PIq.Ti = 9.1e-6f; //Ti = Ts/Ki (Ki=11.11) --- Ts = (~~1e-4)
    PId.Kp = PIq.Kp = 74.07f;
    PId.limH = PIq.limH = 120;
    PId.limL = PIq.limL = -120;
    PIRegulator_Init(&PId);
    PIRegulator_Init(&PIq);

    ClearBuffer();
}

/*
 * infinite loop
 */
void loop()
{

    /* reinitialize filter instances */
    LowPassFlt_Init(&fltU);
    LowPassFlt_Init(&fltI);
}

/*
 * process ADC data
 */
void process_data_ADC1()
{
    /* calc internal reference voltage */
    ADC1voltages.CHVrefint = __LL_ADC_CALC_VREFANALOG_VOLTAGE(ADC1data.CHVrefint,
            LL_ADC_RESOLUTION_12B);

    /* calculate voltages on ADC1 inputs */
    ADC1voltages.CH1 = ADCDataToVoltage(ADC1data.CH1, ADC1voltages.CHVrefint);
    ADC1voltages.CH7 = ADCDataToVoltage(ADC1data.CH7, ADC1voltages.CHVrefint);
    ADC1voltages.CH6 = ADCDataToVoltage(ADC1data.CH6, ADC1voltages.CHVrefint);
    ADC1voltages.CH2 = ADCDataToVoltage(ADC1data.CH2, ADC1voltages.CHVrefint);
    ADC1voltages.CH8 = ADCDataToVoltage(ADC1data.CH8, ADC1voltages.CHVrefint);

    /* calculate currents in all converter phases */
    currents.I_U = ADCVoltageToCurrent(ADC1voltages.CH1);
    currents.I_V = ADCVoltageToCurrent(ADC1voltages.CH7);
    currents.I_W = ADCVoltageToCurrent(ADC1voltages.CH6);

    /* calculate bus voltage */
    Vbus = (float)ADC1voltages.CH2 * VBUS_SENSE_GAIN;

    /* calculate temperature */
    R_NTC = calcResNTC(ADC1data.CH8);
```

```
    temp = calcTemp(R_NTC);
}

/*
 * process ADC data
 */
void process_data_ADC2()
{
    /* calculate voltages on ADC2 inputs */
    ADC2voltages.Ref = ADCDataToVoltage(ADC2data.CH9, ADC1voltages.CHVrefint);
    ADC2voltages.CH17 = ADCDataToVoltage(ADC2data.CH17, ADC1voltages.CHVrefint);
    ADC2voltages.CH11 = ADCDataToVoltage(ADC2data.CH11, ADC1voltages.CHVrefint);
    ADC2voltages.CH14 = ADCDataToVoltage(ADC2data.CH14, ADC1voltages.CHVrefint);
    ADC2voltages.CH12 = ADCDataToVoltage(ADC2data.CH12, ADC1voltages.CHVrefint);
    ADC2voltages.CH15 = ADCDataToVoltage(ADC2data.CH15, ADC1voltages.CHVrefint);
    ADC2voltages.CH5 = ADCDataToVoltage(ADC2data.CH5, ADC1voltages.CHVrefint);

    /* calculate currents in all converter phases */
    gridvoltages.U_U = ADCvToGridVoltage(ADC2voltages.CH17, ADC2voltages.Ref);
    gridvoltages.U_V = ADCvToGridVoltage(ADC2voltages.CH11, ADC2voltages.Ref);
    gridvoltages.U_W = ADCvToGridVoltage(ADC2voltages.CH14, ADC2voltages.Ref);

    loadcurrents.I_U = ADCvToGridCurrent(ADC2voltages.CH12, ADC2voltages.Ref, CS_TURNS_GRID_1);
    loadcurrents.I_V = ADCvToGridCurrent(ADC2voltages.CH15, ADC2voltages.Ref, CS_TURNS_GRID_2);
    loadcurrents.I_W = ADCvToGridCurrent(ADC2voltages.CH5, ADC2voltages.Ref, CS_TURNS_GRID_3);

    uint8_t rxdata;

    if(HAL_UART_Receive_IT(&huart2, rxdata, 1)==HAL_OK){
    //DC_AC_V2G
    //loadcurrents
    //currents
#ifdef BOARD_V2x
        uint8_t txdata[7];
        txdata[0] = (uint8_t)(ADC1voltages.CHVrefint>>4);
        txdata[1] = (uint8_t)(ADC2voltages.CH12>>4);
        txdata[2] = (uint8_t)(ADC2voltages.CH15>>4);
        txdata[3] = (uint8_t)(ADC2voltages.CH5>>4);
        txdata[4] = (uint8_t)(ADC1data.CH1>>4);
        txdata[5] = (uint8_t)(ADC1data.CH7>>4);
        txdata[6] = (uint8_t)(ADC1data.CH6>>4);
        HAL_UART_Transmit(&huart2, txdata, sizeof(txdata), 100);
#endif

    //DC_AC_PV
    //gridvoltage
    //currents
#ifdef BOARD_PV

        uint8_t txdata[7];
        txdata[0] = (uint8_t)(ADC1voltages.CHVrefint>>4);
        txdata[1] = (uint8_t)(ADC2voltages.CH17>>4);
        txdata[2] = (uint8_t)(ADC2voltages.CH11>>4);
        txdata[3] = (uint8_t)(ADC2voltages.CH14>>4);
```

```
        txdata[4] = (uint8_t)(ADC1data.CH1>>4);
        txdata[5] = (uint8_t)(ADC1data.CH7>>4);
        txdata[6] = (uint8_t)(ADC1data.CH6>>4);
        HAL_UART_Transmit(&huart2, txdata, sizeof(txdata), 100);
#endif

    }

}
/*
 * current control logic
 */
void control_task()
{

    LowPassFlt(gridvoltages.U_U, &lpu, &fltU);
    LowPassFlt(gridvoltages.U_V, &lpv, &fltU);
    LowPassFlt(gridvoltages.U_W, &lpw, &fltU);

    vU = 0.666*lpu + 0.333*lpv;
    vV = 0.666*lpv + 0.333*lpw;
    vW = 0.666*lpw + 0.333*lpu;

    plla = ABCtoa(vU, vV, vW);
    pllb = ABCtob(vU, vV, vW);

    array_alpha_aux[cnt_alpha_aux] = plla;
    cnt_alpha_aux++;
    if (cnt_alpha_aux>=200)
        cnt_alpha_aux=0;
    float max_alpha_value = 0;
    for (int i=0;i<200;i++){
        if (max_alpha_value<array_alpha_aux[i]){
            max_alpha_value = array_alpha_aux[i];
        }
    }

    int array_index = (((plla/max_alpha_value)+1)*500);
    if (array_index < 0)
    {
        array_index = 0;
    }else if (array_index > 999) {
        array_index = 999;
    }
    thetal = acos_t[array_index];
    if (pllb<0){
        thetal = thetal*-1;
    }



    array_beta_aux[cnt_beta_aux] = pllb;
    cnt_beta_aux++;
    if (cnt_beta_aux>=200)
```

```
    if (cnt_alpha_aux>=200)
        cnt_alpha_aux=0;
    float max_alpha_value = 0;
    for (int i=0;i<200;i++){
        if (max_alpha_value<array_alpha_aux[i]){
            max_alpha_value = array_alpha_aux[i];
        }
    }

    int array_index = (((plla/max_alpha_value)+1)*500);
    if (array_index < 0)
    {
        array_index = 0;
    }else if (array_index > 999) {
        array_index = 999;
    }
    thetal = acos_t[array_index];
    if (pllb<0){
        thetal = thetal*-1;
    }



    array_beta_aux[cnt_beta_aux] = pllb;
    cnt_beta_aux++;
    if (cnt_beta_aux>=200)
        cnt_beta_aux=0;
    float max_beta_value = 0;
    for (int i=0;i<200;i++){
        if (max_beta_value<array_beta_aux[i]){
            max_beta_value = array_beta_aux[i];
        }
    }



    array_index = (((pllb/max_beta_value)+1)*500);
    if (array_index < 0)
    {
        array_index = 0;
    }else if (array_index > 999) {
        array_index = 999;
    }
    theta2 = asin_t[array_index];
    if (plla<0){
        if (pllb>0){
            theta2 = M_PI-theta2;
        }else{
            theta2 = -M_PI-theta2;
        }
    }

    theta_M = (thetal+ theta2)/2;
```

```
theta_M = (theta1+ theta2)/2;
xd = theta_M*100/M_PI+100;
if (xd > 199)
    xd -= 200;
if (xd < 0)
    xd += 200; //xd = 0 -> theta=pi //xd=100 -> theta=2*pi //xd = 200 -> theta=0 (last one is done in SVPWM.GetSector (if theta > 2*pi -> theta -= 2*pi)


/****current setpoints in dq*****/
iLd = abtod(ABCtoa(loadcurrents.I_U, loadcurrents.I_V, loadcurrents.I_W), ABCtob(loadcurrents.I_U, loadcurrents.I_V, loadcurrents.I_W), -costheta[xd], -sintheta[xd]);
iLq = abtoq(ABCtoa(loadcurrents.I_U, loadcurrents.I_V, loadcurrents.I_W), ABCtob(loadcurrents.I_U, loadcurrents.I_V, loadcurrents.I_W), -costheta[xd], -sintheta[xd]);
iLo = ABCtoO(loadcurrents.I_U, loadcurrents.I_V, loadcurrents.I_W);


LowPassFlt(iLd, &idspmean, &fltI); //get id mean

errorDC = 100 - Vbus;
idug = PIRegulator(errorDC, &PIdc)*0;


idsp = iLd-idspmean - idug; /*- id*/

/*dq of the conveter currents */
idC = abtod(ABCtoa(currents.I_U, currents.I_V, currents.I_W), ABCtob(currents.I_U, currents.I_V, currents.I_W), -costheta[xd], -sintheta[xd]);
iqC = abtoq(ABCtoa(currents.I_U, currents.I_V, currents.I_W), ABCtob(currents.I_U, currents.I_V, currents.I_W), -costheta[xd], -sintheta[xd]);

/* errors of the current controllers*/
errorD = idsp - idC;
errorQ = iLq - iqC;

/*current controllers */
Vd = PIRegulator(errorD, &PId);
Vq = PIRegulator(errorQ, &PIq);


Vasp = dqtoa(Vd, Vq, -costheta[xd], -sintheta[xd]);
Vbsp = dqtob(Vd, iLq, -costheta[xd], -sintheta[xd]);

/******this part is just to check if the sum of the currents in the loads and in the converter will give us a perfect sinusoid*****/
irefA = abtoA(dqtoa(idsp, iLq, -costheta[xd], -sintheta[xd]), dqtob(idsp, iLq, -costheta[xd], -sintheta[xd]), iLo);
irefB = abtoB(dqtoa(idsp, iLq, -costheta[xd], -sintheta[xd]), dqtob(idsp, iLq, -costheta[xd], -sintheta[xd]), iLo);
irefC = abtoC(dqtoa(idsp, iLq, -costheta[xd], -sintheta[xd]), dqtob(idsp, iLq, -costheta[xd], -sintheta[xd]), iLo);
iAx = 20*(loadcurrents.I_U - irefA);
iBx = 20*(loadcurrents.I_V - irefB);
iCx = 20*(loadcurrents.I_W - irefC);
/******this part is just to check if the sum of the currents in the loads and ithe converter will give us a perfect sinusoid*****/

//SVPWM.theta += 0.005f * 2*M_PI;
SVPWM.theta = xd*0.005f * 2*M_PI + M_PI;
if (Vbus < 150 || Vbus > 50)
{
    //SVPWM.mag = abtomag(iasp, ibsp, theta1);
}else
{
    SVPWM.mag = 0;
```

```
    SVPWM_GetSector(&SVPWM);
    SVPWM_CalcDuty(&SVPWM);

    SVPWM_SetCCRVals(&SVPWM);
//  //}

}


/*
 * encode and send measurement data to master
 */
void measToMaster(void)
{
    /* convert and encode data */
    CAN_meas.data.I_out = (int16_t)(1000.0f * currents.I_U);
    CAN_meas.data.V_bus = (uint16_t)(Vbus);
    CAN_meas.data.temp = (int8_t)(temp);

    /* send data over CAN bus */
    CAN_SendMessage(CAN_meas.arr);
}
```

## ctrl_lib.h

```
#ifndef INC_CTRL_LIB_H_
#define INC_CTRL_LIB_H_

typedef struct {
    float C0;  /* filter constant C0 */
    float C1;  /* filter constant C1 */
    float Tau; /* filter time constant */
    float Ts;  /* sample period */
} LowPassFlt_Instance_t;

/*
 * function prototypes
 */
void LowPassFlt_Init(LowPassFlt_Instance_t *instance);
void LowPassFlt(float in, float *out, LowPassFlt_Instance_t *instance);



typedef struct {
    float Kp; /* proportional gain */
    float Ki; /* discrete integrator gain Ts/Ti */
    float Ui_1; /* integrator memory (previous sample) */
    float limH; /* upper limit */
    float limL; /* lower limit */
    float Ti; /* integrator time constant */
    float Ts; /* sample period */
} PIRegulator_Instance_t;

/*
 * function prototypes
 */
void PIRegulator_Init(PIRegulator_Instance_t *instance);
float PIRegulator(float in, PIRegulator_Instance_t *instance);

#endif /* INC_CTRL_LIB_H_ */
```

## ctrl_lib.c

```
/*
 * initialize Low Pass filter structure
 */
void LowPassFlt_Init(LowPassFlt_Instance_t *instance)
{
    instance->C0 = instance->Ts / (instance->Ts + instance->Tau);
    instance->C1 = 1.0f - instance->C0;
}

/*
 * Low Pass filter function
 */
void LowPassFlt(float in, float *out, LowPassFlt_Instance_t *instance)
{
    *out = instance->C0 * in + instance->C1 * (*out);
}

/*
 * initialize PI regulator structure
 */
void PIRegulator_Init(PIRegulator_Instance_t *instance)
{
    instance->Ki = instance->Ts / instance->Ti;
}

/*
 * PI regulator function
 */
float PIRegulator(float in,  PIRegulator_Instance_t *instance)
{
    float up, ui, u;

    up = instance->Kp * in;
    ui = instance->Ki * in + instance->Ui_1;
    u = up + ui;

    /* limits */
    if (u > instance->limH) {
        u = instance->limH;
    } else if (u < instance->limL) {
        u = instance->limL;
    } else { /* if output is not limited */
        instance->Ui_1 = ui; /* remember output of the integrator */
    }

    return u;
}
```

## defs.h

```
#ifndef DEFS_H_
#define DEFS_H_

#include <math.h>

/***********************
 *  Configurations
 ***********************/

/* CAN enable */
#define CAN_EN


//#define BOARD_V2x

#ifndef BOARD_V2x
#define BOARD_PV
#endif


/* aliases for the TIM1 channels */
#define PWM_UH LL_TIM_CHANNEL_CH1
#define PWM_UL LL_TIM_CHANNEL_CH1N
#define PWM_VH LL_TIM_CHANNEL_CH2
#define PWM_VL LL_TIM_CHANNEL_CH2N
#define PWM_WH LL_TIM_CHANNEL_CH3
#define PWM_WL LL_TIM_CHANNEL_CH3N
#define PWM_ADC_TRIG LL_TIM_CHANNEL_CH4

/* control settings */
#define T_PWM 0.0001f /* PWM period - 0.1 ms */

/* convert ADC value [12-bit] to voltage [mV], Vref is the reference voltage [mV] */
#define ADCDataToVoltage(ADCdata, Vref) ((uint16_t)((ADCdata) * (Vref) / ((1 << 12) - 1)))

/* convert ADC voltage [mV] and offset value [mV] to current [A] */
#define ADCVoltageToCurrent(ADCvoltage) ((float) \
    ((0.001f * ((ADCvoltage) - CS_OFFSET)) / (CS_RSENSE * CS_GAIN)))

/* calculate NTC resistance [Ohm] from the ADC value on the divider [12-bit] */
#define calcResNTC(ADCdata) ((float)(R1_TEMP * ((float)((1 << 12) - 1) / ((float)(ADCdata)) - 1)))


/* current sense circuit parameters */
#define CS_RSENSE 0.15f  /* shunt resistance [Ohm] */
#define CS_GAIN -1.7046f /* current sense circuit gain [V/V] */
#define CS_OFFSET 1700   /* current sense circuit offset [mV] */

/* voltage sense circuit parameters and calculation */
#define VS_GAIN_GRID 1.5f  /* [mV/V] */
```

```
#define ADCvToGridVoltage(ADCv, ref) (float)(((ADCv) - (ref)) / VS_GAIN_GRID)

#define CS_GAIN_GRID 15.0f      /* [mV/A] */
/* current sense circuit parameters and calculation */
//#ifdef BOARD_V2x
//#define CS_TURNS_GRID_1 15.0f   /* number of turns in the Hall current sensor (Secondary Side) */
//#define CS_TURNS_GRID_2 16.0f
//#define CS_TURNS_GRID_3 16.0f
//#endif

#ifdef BOARD_PV
#define CS_TURNS_GRID_1 15.0f   /* number of turns in the Hall current sensor (Primary Side) */
#define CS_TURNS_GRID_2 16.0f
#define CS_TURNS_GRID_3 16.0f
#endif


#define ADCvToGridCurrent(ADCv, ref, turns) (float)(((ADCv) - (ref)) / (CS_GAIN_GRID * (turns)))

/* Vbus sense circuit parameters */
#define VBUS_SENSE_GAIN 0.12542f /* Vbus sense circuit gain [V/mV] */
#define VBUS_SENSE_THRESHOLD 0   /* Vbus threshold for NTC bypass [V] */
#define VBUS_UVLO_THRESHOLD 0    /* Vbus threshold for UVLO [V] */

/* Temperature sense circuit parameters */
#define R1_TEMP 3600.0f /*  resistance in series with NTC for temperature measurement [Ohm] */
#define R0_NTC 10000.0f /* NTC resistance at rated temperature [Ohm] */
#define T0_NTC 298.15f  /* rated temperature of the NTC [K] */
#define B_NTC 3988.0f   /* B coefficient of the NTC [K] */


#endif /* DEFS_H_ */
```

## irq.h

```
#ifndef IRQ_H_
#define IRQ_H_

#include "main.h"

/*
 * function prototypes
 */
void DMA1_Channel1_IRQHandler();
/*
 * function prototypes
 */
void DMA1_Channel2_IRQHandler();
#endif /* IRQ_H  */
```

## irq.c

```
#include "irq.h"
#include "app.h"
#include "SVPWM.h"
#include "defs.h"

/*
 * ISR for DMA1 CH1 transfer complete event (ADC readings -> memory)
 */
void DMA1_Channel1_IRQHandler()
{
    LL_DMA_ClearFlag_TC1(DMA1);

    process_data_ADC1();
    control_task();

    DumpTrace();

#ifdef CAN_EN
    static uint32_t cnt;    /* counter */
    if (++cnt == 10000) {   /* 2 Hz */
        cnt = 0;
        measToMaster(); /* encode and send measurement data to master */
    }
#endif /* CAN_EN */
}
/*
 * ISR for DMA1 CH2 transfer complete event (ADC readings -> memory)
 */
void DMA1_Channel2_IRQHandler()
{
    LL_DMA_ClearFlag_TC2(DMA1);

    process_data_ADC2();

    //DumpTrace();
}
```

## SVPWM.h

```c
#ifndef SVPWM_H_
#define SVPWM_H_

#include "main.h"

/*
 * sector enumeration (6 sectors)
 */
typedef enum {
    S1 = 0, S2, S3, S4, S5, S6, S7, S8
} sector_t;

/*
 * Space vector PWM instance
 */
typedef struct {
    float mag; /* reference phasor magnitude (scaled 0-1) */
    float theta; /* reference phasor angle */
    sector_t sector; /* sector in which is the reference phasor */
    float duty1, duty2, duty3; /* duty cyces for PWM */
} SVPWM_instance_t;

/*
 * function prototypes
 */
void SVPWM_GetSector(SVPWM_instance_t *ins);
void SVPWM_CalcDuty(SVPWM_instance_t *ins);
void SVPWM_SetCCRVals(SVPWM_instance_t *ins);

#endif /* SVPWM_H_ */
```

## SVPWM.c

```
#include "SVPWM.h"
#include "app.h"

/*
 * Determine sector in which is the reference phasor
 */
void SVPWM_GetSector(SVPWM_instance_t *ins)
{
    /* theta has to be in range 0-2*pi */
    if (ins->theta < 0) {
        ins->theta += 2*M_PI;
    } else if (ins->theta > 2*M_PI) {
        ins->theta -= 2*M_PI;
    }

    // if else  - if mag <0.05 então setores 7 e 8(vetor 0), senão calcular pelo
    //se vetor anterior for 1,3ou 5 aplicar setor 7, se 2,4,6 então vetor 8


    /* sectors are defined with a step of pi/3 */
    ins->sector = (ins->theta / (M_PI/3));
}

/*
 * Calculate compare times for the reference phasor
 */
void SVPWM_CalcDuty(SVPWM_instance_t *ins)
{
    /* calculate times for adjacent vectors and zero-vector */
    float T1, T2, T0;
    T1 = ins->mag * sinf((ins->sector + 1) * M_PI/3 - ins->theta);
    T2 = ins->mag * sinf(ins->theta - ins->sector * M_PI/3);
    T0  = 1 - T1 - T2;

    /* depending on sector, calculate compare times for PWM */
    switch (ins->sector) {
    case S1:
        ins->duty1 = T1 + T2 + T0/2;
        ins->duty2 = T2 + T0/2;
        ins->duty3 = T0/2;
        break;
    case S2:
        ins->duty1 = T1 + T0/2;
        ins->duty2 = T1 + T2 + T0/2;
        ins->duty3 = T0/2;
        break;
```

```
    case S3:
        ins->duty1 = T0/2;
        ins->duty2 = T1 + T2 + T0/2;
        ins->duty3 = T2 + T0/2;
        break;
    case S4:
        ins->duty1 = T0/2;
        ins->duty2 = T1 + T0/2;
        ins->duty3 = T1 + T2 + T0/2;
        break;
    case S5:
        ins->duty1 = T2 + T0/2;
        ins->duty2 = T0/2;
        ins->duty3 = T1 + T2 + T0/2;
        break;
    case S6:
        ins->duty1 = T1 + T2 + T0/2;
        ins->duty2 = T0/2;
        ins->duty3 = T1 + T0/2;
        break;
    default: /* is not in any of the sectors */
        ins->duty1 = ins->duty2 = ins->duty3 = 0.0f;
        break;
    }
}
/*
 * Convert compare times to CCR values for timer and write them to registers
 */
void SVPWM_SetCCRVals(SVPWM_instance_t *ins)
{
    TIM1->CCR1 = (uint32_t)(TIM1_ARR * ins->duty1);
    TIM1->CCR2 = (uint32_t)(TIM1_ARR * ins->duty2);
    TIM1->CCR3 = (uint32_t)(TIM1_ARR * ins->duty3);
}
```

## trans.h

```
float ABCtoa(float A, float B, float C);
float ABCtob(float A, float B, float C);
float ABCtoO(float A, float B, float C);
float abtod(float a, float b, float cos, float sin);
float abtoq(float a, float b, float cos, float sin);
float dqtoa (float d, float q, float cos, float sin);
float dqtob (float d, float q, float cos, float sin);
float abtoA (float a, float b, float o);
float abtoB (float a, float b, float o);
float abtoC (float a, float b, float o);
float abtomag (float a, float b, float max);
```

## trans.c

```
#include "math.h"
#include "trans.h"


float a = 0;
float b = 0;
float o = 0;
float d = 0;
float q = 0;
float A = 0;
float B = 0;
float C = 0;
float mag = 0;

float ABCtoa (float A, float B, float C)
{
    a = 0.817 * (A - 0.5*B - 0.5*C);
    return a;
}
//
float ABCtob (float A, float B, float C)
{
    b = 0.817 * (0.866*B - 0.866*C);
    return b;
}

float ABCtoO (float A, float B, float C)
{
    o = 0.817 * (1/1.414*A + 1/1.414*B + 1/1.414*C);
    return o;
}


float abtod (float a, float b, float cos, float sin)
{
    d = a * cos + b *sin;
    return d;
}

float abtoq (float a, float b, float cos, float sin)
{
    q = -a * sin + b * cos;
    return q;
}

float dqtoa (float d, float q, float cos, float sin)
{
    a = d * cos - q * sin;
    return a;
}
```

```
float dqtob (float d, float q, float cos, float sin)
{
    b = d * sin + q * cos;
    return b;
}

float abtoA (float a, float b, float o)
{
    A = 0.817*(a + 0.707*o);
    return A;
}
float abtoB (float a, float b, float o)
{
    B = 0.817*(-0.5*a + 0.866*b + 0.707*o);
    return B;
}
float abtoC (float a, float b, float o)
{
    C = 0.817*(-0.5*a - 0.866*b + 0.707*o);
    return C;
}

float abtomag (float a, float b, float max)
{
    mag = sqrt(a*a + b*b);
    if (mag > 1){
        mag = 1;
    }
    return mag;
}
```