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Integer N Synthesizer Design for LoRa Transceivers

Vitor Fialho

Abstract: This paper presents the study and design of an Integer N synthesizer model for three LoRa ISM bands: 430 MHz, 868 MHz and 915 MHz. The proposed topology is composed by two voltage controlled oscillators working in two different bands. The presented model uses the same phase-frequency detector, charge pump and loop filter. This study is focused on dynamic and steady-state analysis in order to infer the synthesizer stability and bandwidth. The performed study shows that the settling time for all bands is less than 40 μ s for a bandwidth of 102 kHz.

Keywords: LoRa, Settling Time, Synthesizer, Transceiver

I. INTRODUCTION

Low power wide area networks (LPWAN) has become a predominant wireless communications topic due to novel technologies that provide a wide connectivity, for a low data rate and a low throughput [1]. One technology that emerged in the last few years is provided by Semtech with the long range (LoRa) product. LoRa is a non-cellular long range and low power wireless technology that operates in the unlicensed industrial, scientific and medical (ISM) frequency bands [2]. LoRa radio frequency (RF) signals are based on chirp spread spectrum (CSS) modulation whose versatility allows the communications at long distances, typically a few km to hundreds of km, depending if it is an urban or rural environment [1]. This modulation technique is used by LoRa wide area networks (LoRaWAN), that encode the information provided from multiple sensors working in low power consumption modules. This protocol, developed by LoRa Alliance, enables the communication with LoRa modules through the Internet.

Typical parameters that are used for LoRaWAN analysis and planning are: spreading factor (SF), code rate (CR), channel bandwidth (BW) and received signal strength intensity (RSSI) [3]. However, each LoRa signal must be transmitted in specific channel available in ISM band: 430 MHz, 868 MHz and 915 MHz [1].

The up and down conversion of the LoRa signal is performed by a transceiver typically in half-duplex[4]. The signal used for this purpose must be produced by a stable signal. For that purpose it is used a phase-lock loop (PLL) frequency synthesizer, which allows the carrier generation with frequency multiple of a single signal reference. The

main application is in generating local oscillator (LO) signals for the up- and down-conversion of RF signals.

Typical research works based on RF synthesizers are focused on building blocks optimization for fully integration, low power consumption, lock time and phase noise [5-8]. Although several manufacturers produce LoRa transceiver integrated circuits, detailed information about RF building blocks is very sparse. There are few manufactures that provide electrical information about LoRa RF specificities such as type of VCO used, charge pump current and loop filter components [4].

In this work it is presented the design of an Integer N synthesizer, implemented with a multi-band VCO, for LoRa ISM channels frequency conversion. The presented results, performed by MATLAB and Simulink simulations, are based on two voltage controlled oscillator architecture, optimized for three LoRa bands: 430 MHz (Band 1), 868 MHz (Band 2) and 915 MHz (Band 3).

This paper is organized as follows; in section II it is presented the synthesizer role on RF front-end. Section III presents the proposed model for this work, where the dynamic and steady state analysis are presented. The results and discussion are presented in section IV. The conclusions and the suggested future work are presented in section V.

II. SYNTHESIZER ROLE ON A TRANSCEIVER FRONT-END

The transceiver front-end can be divided in two main building blocks: base band (BB) and RF. Base band block is responsible for acquire, conditioning and formatting the signals from any source. This process is performed by a microcontroller or a digital signal processor (DSP). The RF block is responsible for the up conversion (TX) and down conversion (RX) of a specific channel whose frequency is defined by the synthesizer. In Fig.1 it is presented a generic transceiver composed by a DSP, a transmitter, receiver, synthesizer, duplexer and antenna. As depicted the synthesizer has a predominant role, since it is the common block between the transmitter and receiver.

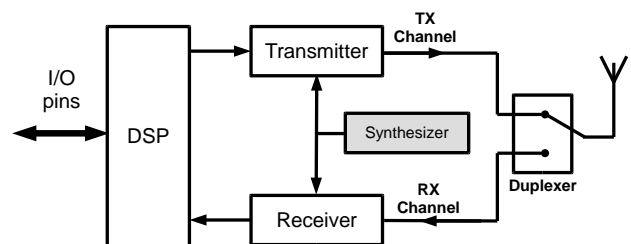


Fig. 1. Transceiver building blocks

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A. Transceiver building blocks

Fig.2 presents the RF transmitter topology. As depicted, the information deriving from the DSP is converted from binary to analog by the digital to analog converter (DAC). The synthesizer, together with a mixer, up-converts the BB signal to a desired channel with a specific frequency. The power amplifier (PA) amplifies the signal to the desired transmission power.

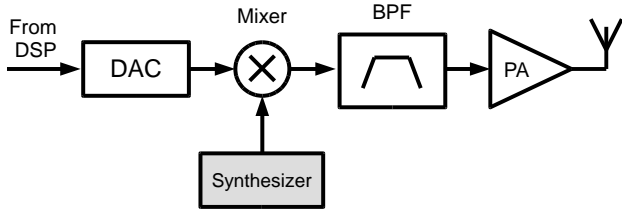


Fig. 2.RF transmitter topology

In Fig.3 it is presented the RF receiver topology. The low noise amplifier (LNA) amplifies the RF band in which the desired RF channel is located. The filtered channel is then down-converted by the mixer and synthesizer to BB signal for prior processing.

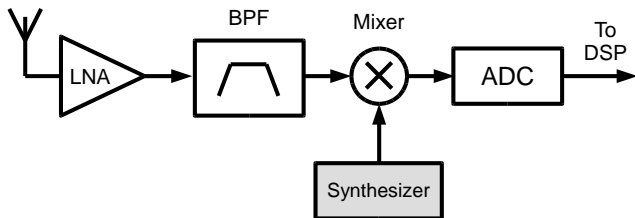


Fig. 3.RF receiver topology

As it turns out, the synthesizer has a preponderant role in a transceiver, since it is the common building block of the transmitter and receiver, providing the carrier signal for the modulation and demodulation processes. Since this study do not cover RF impairments, it is assumed that there is no IQ mismatch, the PA is operating in a linear zone and the combiner losses are negligible.

B. Synthesizer Typical Topology

Typical Integer N synthesizer architecture is presented in Fig. 4, and it is composed by an external low frequency reference signal whose frequency is divided by M , producing $v_{ref}(t)$, a phase-frequency detector (PFD), charge pump, loop filter, VCO and a frequency divider with a dividing ratio of N .

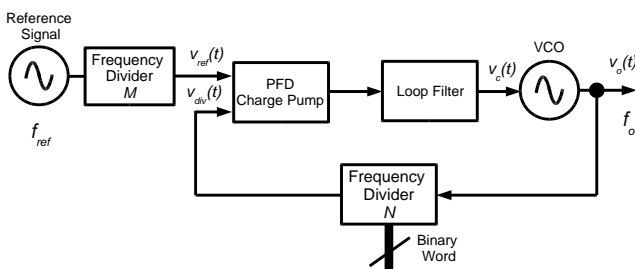


Fig. 4.Typical Integer N synthesizer building blocks

The low frequency reference signal, $v_{ref}(t)$, is compared with the signal, $v_{div}(t)$, from the frequency divider by N . This comparison is performed by the PFD and charge pump. These two blocks produce an output voltage proportional to

the phase and frequency difference between the reference signal and the feedback signal ($v_{div}(t)$).

The loop filter suppresses high frequency components from the output of the charge-pump and ensures loop stability. The filtered signal $v_c(t)$, is then applied to the VCO input control voltage. The output frequency (f_o), that depends on the reference frequency signal is expressed by (1).

$$f_o = \frac{N}{M} \cdot f_{ref} , \tag{1}$$

The divider block can be configured with a binary word that changes the dividing ratio.

III. PROPOSED MODEL FOR INTEGER N SYNTHESIZER

In Fig. 5 it is represented the proposed integer N synthesizer topology for this work. It is based on typical topology presented in Fig. 4, however instead of one VCO, this topology has two VCOs: one for 430 MHz band (VCO1) and the other for 868 MHz and 915 MHz (VCO2). This design option minimizes VCO dynamic range and optimizes it for fast locking and low phase noise. The VCO is selected according to the desired band. In this architecture the loop filter is the same for both bands.

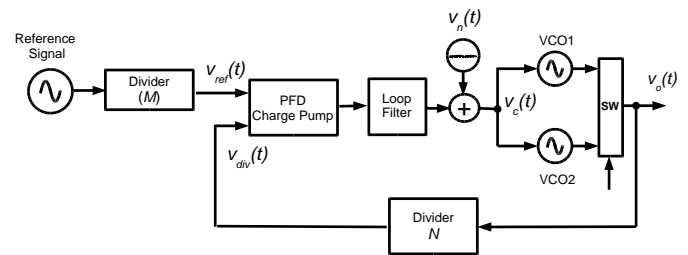


Fig. 5.Integer N synthesizer building blocks

To enable the study of the synthesizer in non-ideal conditions, one noise source is used at the VCO input, as represented in Fig. 5 by $v_n(t)$. This noise source presents a Gaussian amplitude distribution with zero mean and variance v_n^2 .

The PFD was implemented with the standard logic circuit composed by D type flip-flops, as presented in Fig. 6 [6]. The charge-pump current (I_{CP}) is 2.5 mA.

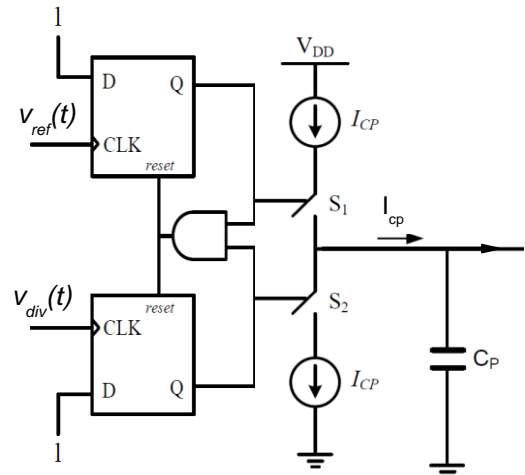


Fig. 6.PFD topology with charge pump



The loop filter used in this work is shown in Fig. 7 [5]. It is composed by the charge pump capacitor (C_p) and R_z in series with C_z , which imposes a zero at the frequency 401 kHz and two poles: 0 Hz and 48 kHz.

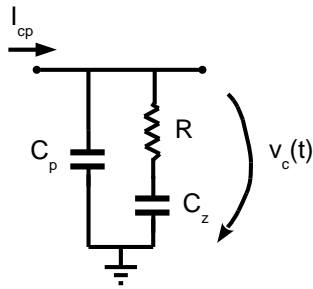


Fig. 7. Synthesizer loop filter

In Fig. 8 it is presented the ideal VCO output frequency variation with the control voltage. When $V_c=0$ V, the VCO output signal frequency is designated by quiescent frequency, (f_q). Thus, the VCO frequency may change between f_q and f_{max} . The slope of this linear variation corresponds to the VCO gain (K_{VCO}) which is given in Hz/V.

$$f_o = f_q + K_{VCO} \cdot V_c \quad (2)$$

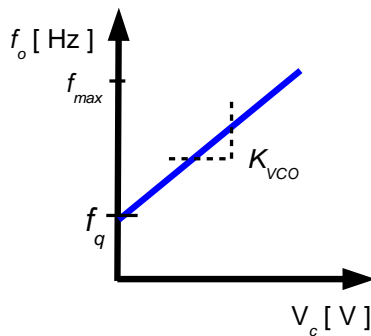


Fig. 8. VCO – voltage vs frequency

The divider N architecture is composed by a counter and a JK flip-flop. The counter output is active when it reaches the value N , activating the flip-flop guaranteeing a synchronous signal between the input and the output of the divider [5].

Table I presents the values used for this work [4]. The common values for all bands are shown first, such as the loop filter components and the PFD gain. For each frequency band it is presented the VCO characteristics.

Table- I: Synthesizer building blocks values used on simulations

	C_z	4.4 nF
	C_p	49 nF
	R	820 Ω
	K_{PFD}	$3,9 \times 10^{-3}$ rad/V
	I_{CP}	2.5 mA
Band 1	K_{VCO}	150 MHz/V (VCO 1)
	f_q	400 MHz
	N	215
Band 2	K_{VCO}	150 MHz/V (VCO 2)
	f_q	800 MHz
	N	434
Band 3	K_{VCO}	150 MHz/V (VCO 2)
	f_q	800 MHz
	N	457

A. Dynamic Analysis

The design of any synthesizer implies the analysis in dynamic (transient) state in order to verify the system stability. This can be done by verifying the VCO control voltage, $v_c(t)$. In sake of simplicity, the noise source is not active for these simulations.

In Fig. 9 it is presented $v_c(t)$, for the three LoRa ISM frequency bands. As depicted, the settling time is 30 μ s for all bands which corresponds to the suggested values [4]. These graphics are obtained by starting the simulation for each desired channel. Changing the channel during simulation it will be analyzed in section IV.

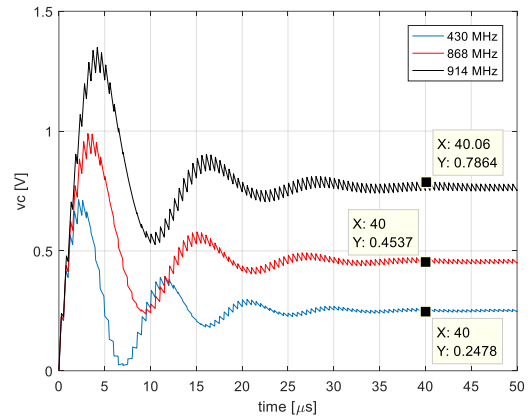


Fig. 9. VCO control voltage for three LoRa bands

According to expression (2) and the values presented in Table I, it is possible to verify, for each frequency, what is the mean value of $v_c(t)$. As an example, for $f_o= 868$ MHz, the VCO control voltage stabilizes when $V_c \approx 0.45$ V which corresponds to $800 \text{ MHz} + 150 \text{ MHz/V} \times 0.45 \text{ V}$.

Other study strand consists in changing the K_{VCO} value. This option is useful since it can be establish a tradeoff between loop bandwidth and the synthesizer stability. Assuming the nominal K_{VCO} is 150 MHz/V, as presented in Table I, it was produced a variation of ± 50 MHz/V. The evolution for the three VCO gains is presented in Fig. 10. These results are obtained for division ratio of 434, which implies a $f_o= 868$ MHz.

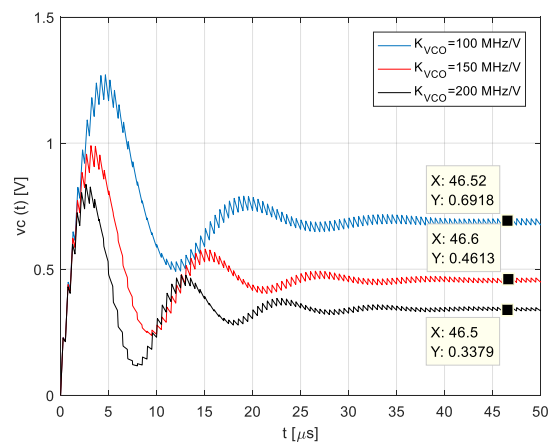


Fig. 10. VCO control voltage for different K_{VCO} values



In Fig. 11, Fig. 12 and Fig. 13 is presented the synthesizer output signal spectrum for 430 MHz, 868 MHz and 915 MHz, respectively. These spectrums are obtained with $v_n^2=0$ W. As depicted the synthesizer generates a carrier in the desired frequency.

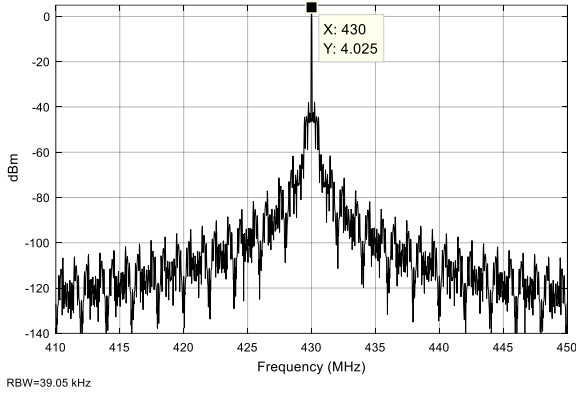


Fig. 11. Synthesizer output spectrum for 430 MHz

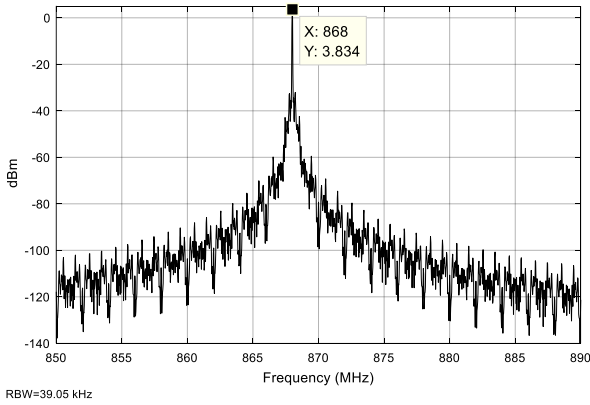


Fig. 12. Synthesizer output spectrum for 868 MHz

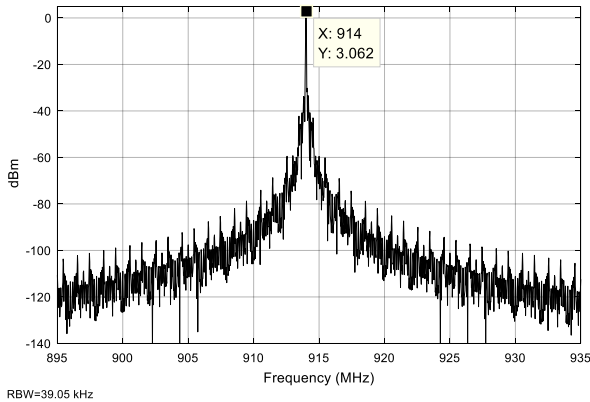


Fig. 13. Synthesizer output spectrum for 915 MHz

B. Steady State Analysis

The synthesizer transient response is a nonlinear phenomenon that cannot be formulated easily. However, assuming the synthesizer in lock conditions, a linear approximation can be used. Fig. 12 shows the synthesizer linear model given by

$$H(s) = \frac{\varphi_o(s)}{\varphi_i(s)}, \tag{3}$$

where $\varphi_i(s)$ e $\varphi_o(s)$, corresponds to the input and output phase, respectively. Thus, in steady state, the synthesizer can be

analyzed in Laplace domain where each building block is represented as depicted in Fig. 12. Open and closed loop expressions are given by (4) and (5).

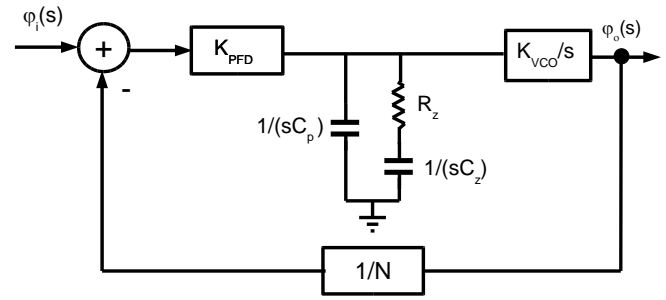


Fig. 14. Integer N synthesizer linear model

The open loop transfer function, $H_{OL}(s)$ is given by

$$H_{OL}(s) = \frac{K(1 + sC_zR_z)}{s^2N[sC_pC_zR_z + (C_p + C_z)]}, \tag{4}$$

and the closed loop $H_{CL}(s)$ is given by

$$H_{CL}(s) = \frac{NK(1 + sC_zR_z)}{s^3NC_pC_zR_z + s^2N(C_p + C_z) + sKC_zR_z + K}, \tag{5}$$

where $K = K_{VCO} \cdot K_{PFD}$. All values used are available in Table I. In Fig. 13 it is presented the amplitude and phase of $H_{OL}(s)$ for Band 2, e.g., 868 MHz. In Fig. 15 it is presented the amplitude $|H_{OL}(s)|$ and phase $\arg[H_{OL}(s)]$ variation of expression (4).

With this representation it is possible to obtain the cross over frequency, $|H_{OL}(s)|=0$ dB, which allows calculating the synthesizer bandwidth and phase margin.

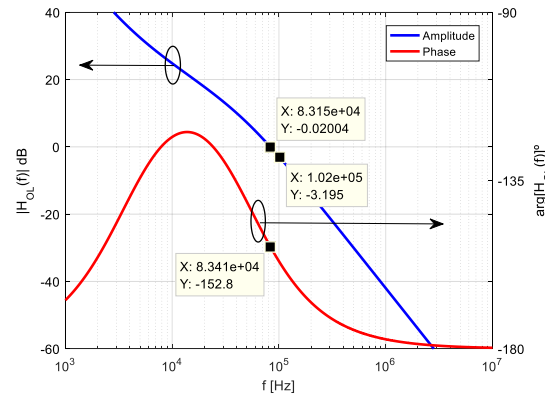


Fig. 15. Open loop: amplitude and phase response

As depicted the cross over frequency is $f_{co} = 83.1$ kHz which implies that the synthesizer bandwidth of 102 kHz. The angle obtained for presented f_{co} is -152° , which corresponds to a phase margin of 27° . Table II presents the cross over frequency, loop bandwidth and phase margin regarding the K_{VCO} values presented in Fig. 10.



Table- II: Steady state parameters variation with K_{VCO}

$K_{VCO}=100$ MHz	$f_{co} = 65.5$ kHz
	$f_{3dB} = 80.2$ kHz
	Phase margin= 32°
$K_{VCO}=150$ MHz	$f_{co} = 83$ kHz
	$f_{3dB} = 100.7$ kHz
	Phase margin= 27°
$K_{VCO}=200$ MHz	$f_{co} = 97.6$ kHz
	$f_{3dB} = 117.9$ kHz
	Phase margin= 23°

In Fig. 16 it is presented the amplitude and phase of $H_{CL}(s)$ for Band 2. According to (5), when $s \rightarrow 0$, $|H_{CL}(s)| \approx N$, thus the synthesizer low frequency gain is 52 dB which corresponds to $20 \log_{10}(N)$, for $N=434$. Despite the slight overshoot, the synthesizer is stable, as depicted in Fig. 9 and Fig. 10.

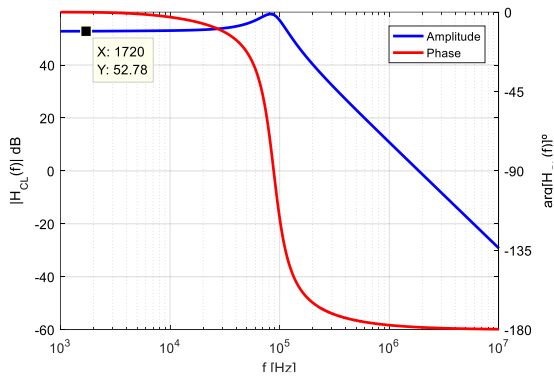


Fig. 16. Closed loop: amplitude and phase response

IV. RESULTS AND DISCUSSION

This section presents the simulation results of the proposed model in section III, based on spectral and dynamic analysis. All performed simulations were made with the noise source with a Gaussian distribution configured with a variance of $v_n^2=10 \mu W$. Fig. 17 shows the histogram of the noise source amplitude distribution, which is obtained with a time of sampling of 0.1ns and the simulation time is configured for 400 μs .

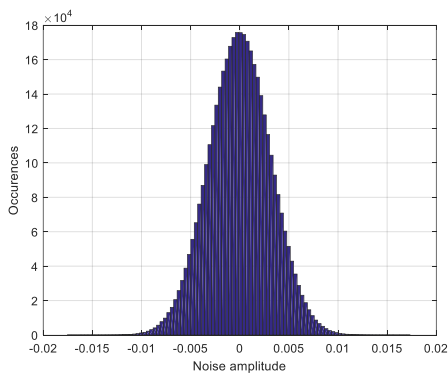


Fig. 17. Noise source histogram for $v_n^2=10\mu W$

In Fig. 18 and Fig. 19 it is presented the spectrum of the synthesizer output signal, where the noise floor tends to -80dBm. Comparing this spectrum with the one shown in Fig

11 it is possible to verify the noise source impact, due to the noise floor increase.

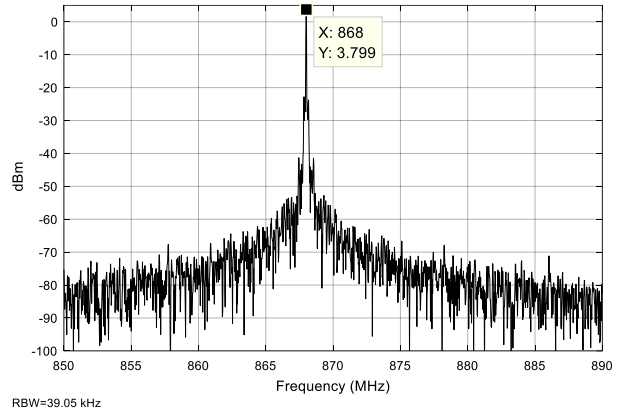


Fig. 18. Synthesizer output spectrum for 868 MHz

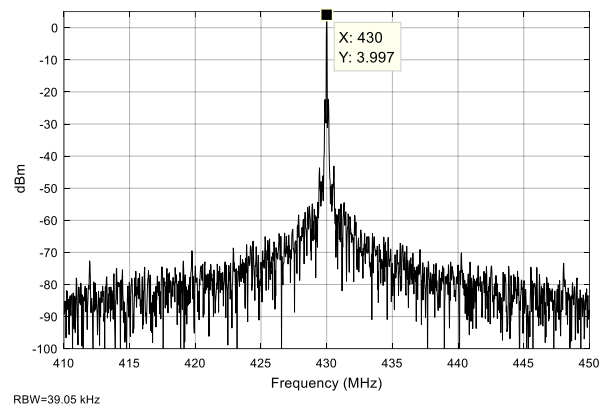


Fig. 19. Synthesizer output spectrum for 430 MHz

In Fig. 20 the VCO control voltage evolution, during synthesizer channel changing, is presented. This representation allows the synthesizer evaluation (loop stability and settling time) during channel selection. The presented results are obtained for a frequency change from 868 MHz to 430 MHz. This is done by changing the division ratio, according to the values presented in Table I.

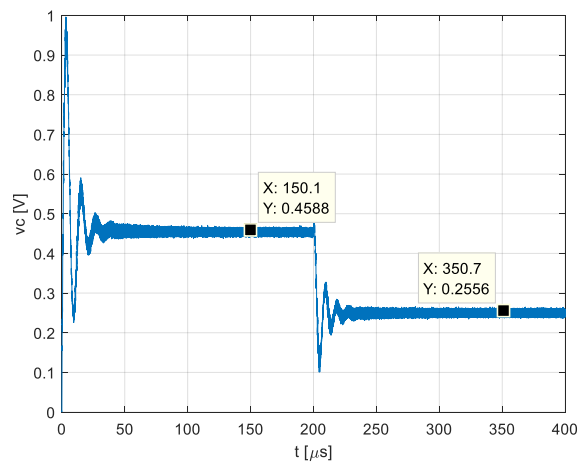


Fig. 20. VCO control voltage - channel changing



For the synthesizer output frequency of $f_o = 868$ MHz, the VCO control voltage stabilizes when $V_c \approx 0.45$ V which corresponds to $800 \text{ MHz} + 150 \text{ MHz/V} \times 0.45 \text{ V}$. For $f_o = 430$ MHz, $V_c \approx 0.26$ V, which corresponds to $400 \text{ MHz} + 150 \text{ MHz/V} \times 0.26 \text{ V}$.

As depicted for each selected frequency the synthesizer stabilizes $40\mu\text{s}$ after the channel selection.

V. CONCLUSIONS AND FUTURE WORK

This work presented a design method focused on Integer N synthesizers for LoRa ISM frequency bands. The obtained results are supported on simulations performed in dynamic and steady state. With this simulation model it is possible to change multiple parameters of the Integer N synthesizer. In the VCO it is possible to change its gain, quiescent frequency and amplitude. It is possible to change the dividing ratio while the simulation is performed, and then verify the locking time by inspecting the VCO control voltage evolution.

The proposed model presented in this work has two VCOs instead of only one that covers all dynamic range. This option lead to a lower VCO gain, which implies a lower loop bandwidth, however it is less sensible to noise from the control VCO control voltage.

For the three LoRa ISM bands used in this work, the synthesizer settling time is less than $40 \mu\text{s}$ for each one. A simulation of channel changing was performed and the settling time remains identical. VCO gain presents an impact on synthesizer bandwidth, however a variation of 50 MHz implies a bandwidth difference of 20kHz . Therefore, the presented work denotes that is possible, with a low gain VCO, cover three frequency bands low settling time.

Regarding future work it is proposed the study of phase noise and power consumption with this topology.

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