Fault Tolerant Operation of Three-Phase 3 Level T-Type qZS Inverters using Sliding Mode Current Controllers

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***Abstract*— Due to the boost characteristic and the several possible outputs of quasi-Z-source inverters (*qZSI*), these topologies can be valuable options to operate under fault conditions, provided the controller is able to take advantage of the available output states. Thus, the development of control systems to take advantage of the available outputs is needed. Hence, this paper focuses on the development of a control system to operate a three-phase three-level T-Type *qZSI* under fault tolerant conditions. The controller is based on a sliding mode current controller associated to a vectorial modulator selecting the available outputs. The proposed strategy for the controller and modulator is presented taking into consideration the normal and fault-tolerant requirements. The strategy also considers the balance of the capacitors under fault tolerant condition. The converter operating in both modes is tested through several simulation studies.**

Keywords*— *Fault Tolerant; T-Type converter, quasi-Z-source inverter (qZSI); Vectorial Modulatior Introduction (Heading 1)

I. INTRODUCTION

Power electronic converters are critical equipment for the development of the industry and comfort for the people. Indeed, they are used in a huge variety of equipment, such as motor drives, flexible *AC* transmission systems (*FACTS*), high voltage *DC* transmission (*HVDC*) and power supplies for electronic consumers [1]. One of the areas extensively studied and benefited in the last decade has been renewable energy conversion [2, 3]. Among the several renewable sources, photovoltaic (*PV*) generators are now considered as fundamental in the road to lower greenhouse gas emission. For PV generators, the power electronic converters are critical as the interface between the solar panels and the *AC* grid and/or *DC* loads. Converters and fault tolerant operation are a key element to the widespread use of solar *PV* energy.

In *PV* generators connected to the *AC* grid, power electronic converters are responsible for the energy conversion between the *DC/AC* voltage, as well as, the *PV* panel operation in the maximum power point (*MPP*). Several converters topologies, with or without galvanic isolation, have been proposed to interface *PVs* [4-10]. Another issue related with the adopted *DC/AC* topologies, is the use of inverters with two or more than two voltage levels (multilevel). Initially it was adopted the use of inverters with two-voltage levels. The first topologies used well known inverters capable of operation only in buck mode. This is an important limitation for *PV* applications. Thus, to avoid an additional *DC/DC* converter, inverters were proposed with *buck-boost* capability, such as the case of the Z and quasi-Z voltage source inverter (*ZVSI*, *qZVSI*) [11-13]. Besides the boost capability, *ZVSI* and qZVSI introduces a new state, namely the shoot-through (*ST*) state. It is characterized by the simultaneous conduction of both switches of the same inverter leg. This state is critical in boost mode since it allows the increase of the *DC* voltage applied to the inverter. The possibility to use this state will also improve the reliability of the inverter.

Multilevel inverters have been proved to be a good solution for *PV* applications as they present advantages, such as, higher performance and higher power density. Therefore, the adoption of *PV* generators without galvanic isolation using multilevel inverters is now a reality. Several topologies were proposed, the three most known are the cascaded H-bridge, neutral point clamped and flying capacitor [14,15]. Meanwhile, another multilevel topology emerged with interesting characteristics, the so called T-type inverter [16-18]. However, the original T-type topology can only operate in buck mode like the two-level inverter. Thus, the T-type topology associated to an impedance

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source network was rapidly proposed for *PV* applications [19-25].

One important aspect for *PV* inverters is their reliability. Several proposals have been made in order to improve their capability to operate under fault tolerant conditions. There are two possibilities to add fault tolerant capability to inverters, namely increasing the hardware complexity (increasing the number of power semiconductors) or through the change of the modulation or control. Several topologies have been proposed in which the operation in tolerant mode is achieved through a change of the power circuit. These topologies have been proposed for the two-level *qZVSI* as can be seen in [26-28]. Given the advantages of multilevel topologies their operation in fault tolerant mode has also been explored. Indeed, one of the interesting capabilities of multilevel topologies is their capability to operate in fault tolerant mode due to a fault in a power semiconductor, changing only the modulation or control system. Thus, several approaches using this concept have been proposed for the multilevel *qZVSIs* [22, 29, 30]. Usually, under faults the inverter operates at reduced power. However, due to the capability of the boost mode associated to the *qZVSIs* inverters, this problem can be overcome through the increase of the *DC* voltage applied to the inverter [22].

To propose a fast and robust controller for the three-phase T-Type *qZVSI*, this paper presents a sliding mode current controller associated to a vectorial modulator for the three-phase T-Type *qZVSI*. The controller and modulator operation in fault tolerant mode is detailed for the three-phase T-Type *qZVSI*. As it will be shown, the fault tolerant mode requires a modification in the adopted strategy for the voltage vectorial modulator. Nevertheless, the modification leads to a robust controller even in faulty conditions. Several tests will be presented to confirm the fault tolerant operation.

II. Control of the T-Type qZVI Source in Normal and Fault Tolerant Condition

The simplified power circuit of the three-phase three-level T-Type *qZSI* is presented in Fig. 1. The topology consists into two impedance source networks including four inductors (L_1-L_4), four capacitors (C_1-C_4) and two diodes (D_1, D_2). The three-phase T-Type inverter is connected at the output of the impedance source networks, with the middle point of the networks connected to the three bi-directional switches.

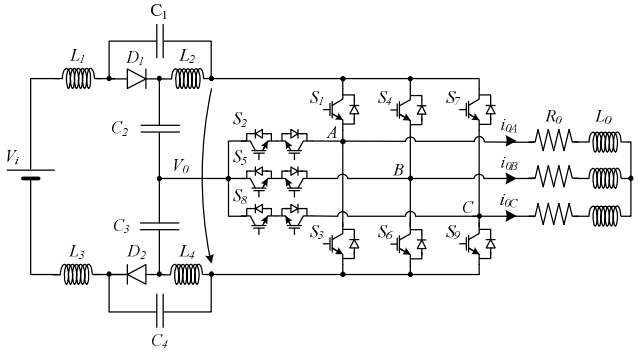


Fig. 1. Power electronic circuit of the three-phase T-Type qZSI.

To control the converter in normal and fault tolerant mode, it is proposed the use of a sliding mode current controller associated to a voltage vector modulator (Fig. 2). The outputs of the current controller will be the inputs of the voltage modulator, as space vector modulation will be adopted to ensure that the *AC* currents will track their references. The vector modulator samples the capacitor voltages V_{C2} and V_{C3} to additionally ensure their balance. Thus, the vector voltage to be selected by the current controller must ensure the capacitors V_{C2}, V_{C3} voltage balance. The modulator must also deal with power semiconductor faults. As explained hereafter, the vector modulator must select vectors to enable fault tolerant capability. Therefore, the adopted vector selection strategy of the modulator must have an insight if the converter is operating in normal or in fault tolerant mode.

To develop the vectorial voltage modulator, a dynamic model of the inverter it needed to know the position of the *AC* voltage space-vectors, which are functions of the switch states S_j. To obtain the model, it is assumed the switches are ideal. Therefore, it can be considered that they are related to discrete and non-linear switching functions that could take one of three possible values depending on the state S_j of the semiconductor switches. The respective output voltages will correspond to three voltage levels. In this way, the output voltages will be related to switching functions Fi presented in equation (1), being $i = A, B, C$ and $j = 1, 4, 7$. From (1), the output *AC* voltages are given from the switching functions Fi as written in (2), where the *AC* voltages (V_A, V_B and V_C) are the phase-neutral voltages.

$$F_i = \begin{cases} 1 & if\ S_j\ is\ on \wedge S_{j+1}\ is\ off\ \wedge S_{j+2}\ is\ off \\ 0{,}5 & if\ S_j\ is off \wedge S_{j+1} is on \wedge S_{j+2} is off \\ 0 & (if\ S_j\ is off \wedge S_{j+1} is off \wedge S_{j+2} is on)\ \vee \\ & (if\ S_{1,2,3} is on \vee S_{4,5,6} is on \vee S_{7,8,9} is on) \end{cases} \quad (1)$$

$$\begin{bmatrix} V_A \\ V_B \\ V_C \end{bmatrix} = V_o \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} F_A \\ F_B \\ F_C \end{bmatrix} \quad (2)$$

To obtain the vector diagram and to develop the vector modulator, the Clarke-Concordia transformation is applied to (2). In the $\alpha\beta$ coordinates plane, 27 voltage space-vectors are obtained, although only 19 have distinct affixes (Fig. 2). The 27 voltage vectors are also listed in Table I, which also includes the switching combinations needed to obtain each voltage vectors.

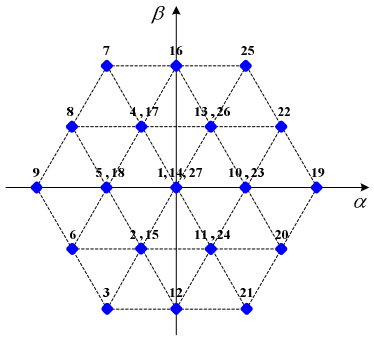


Fig. 2. AC voltage vectors in the plane of the $\alpha\beta$ coordinates.

TABLE I. OUTPUT VOLTAGE VECTORS OF THE THREE-PHASE THREE-LEVEL T-TYPE QZSI INVERTER

Vector	F_A	F_B	F_C	V_o/V_{dc}	V_β/V_{dc}
1	0	0	0	0.0000	0.0000
2	0	0	0.5	-0.2041	-0.3536
3	0	0	1	-0.4082	-0.7071
4	0	0.5	0	-0.2041	0.3536
5	0	0.5	0.5	-0.4082	0.0000
6	0	0.5	1	-0.6124	-0.3536
7	0	1	0	-0.4082	0.7071
8	0	1	0.5	-0.6124	0.3536
9	0	1	1	-0.8165	0.0000
10	0.5	0	0	0.0000	0.0000
11	0.5	0	0.5	-0.2041	-0.3536
12	0.5	0	1	-0.4082	-0.7071
13	0.5	0.5	0	-0.2041	0.3536
14	0.5	0.5	0.5	-0.4082	0.0000
15	0.5	0.5	1	-0.6124	-0.3536
16	0.5	1	0	-0.4082	0.7071
17	0.5	1	0.5	-0.6124	0.3536
18	0.5	1	1	-0.8165	0.0000
19	1	0	0	0.8165	0.0000
20	1	0	0.5	0.6124	-0.3536
21	1	0	1	0.4082	-0.7071
22	1	0.5	0	0.6124	0.3536
23	1	0.5	0.5	0.4082	0.0000
24	1	0.5	1	0.2041	-0.3536
25	1	1	0	0.4082	0.7071
26	1	1	0.5	0.2041	0.3536
27	1	1	1	0.0000	0.0000

The three-phase T-Type *qZVSI* inverter has the capability to use shoot-through states. These states allow the converter operation in boost mode, increasing the *DC* voltage seen at the input of the three-phase T-Type inverter. The increase of this voltage is function of the so called boost factor (*B*), given as:

$$V_o = B\,V_i = \frac{1}{1-2\,D}\,V_i \tag{3}$$

where variable *D* is related with the shoot-through duty-cycle.

In the quasi-Z inverter, there are possible combinations associated to the shoot-though states. The shoot-through states are associated to the three vectors located at the origin of the $\alpha\beta$ plane. The applied voltage to the load is zero during the application of these vectors, but the shoot-through state will affect the amplitude of all remaining voltage vectors.

To control the output *AC* currents a sliding mode controller will be used. This controller can be designed from the state-space equations of the converter given by (4) in $\alpha\beta$ coordinates, where Γ_A, Γ_B, Γ_C are defined in (5).

$$\begin{bmatrix} \frac{di_\alpha}{dt} \\ \frac{di_\beta}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_o}{L_o} & 0 \\ 0 & -\frac{R_o}{L_o} \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + \sqrt{\frac{2}{3}}\,V_o \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \Gamma_A \\ \Gamma_B \\ \Gamma_C \end{bmatrix} \tag{4}$$

$$\begin{cases} \Gamma_A = \frac{1}{3}(2F_1 - F_2 - F_3) \\ \Gamma_B = \frac{1}{3}(-F_1 + 2F_2 - F_3) \\ \Gamma_C = \frac{1}{3}(-F_1 - F_2 + 2F_3) \end{cases} \tag{5}$$

Considering the space vector control inputs $V_o[\Gamma A\ \Gamma B\ \Gamma C]^T$, the strong relative degree of the i_α, i_β currents is unity [31]. Therefore, the sliding mode manifold functions f_α, f_β, given in (6), should be proportional to the current errors to obtain a robust sliding mode switching current controller (proportionality constant is unity). The current references $i_{\alpha ref}$, $i_{\beta ref}$ are to be defined by a AC (or DC) power controller, outside the scope of this paper.

$$\begin{cases} f_\alpha = i_{\alpha ref} - i_\alpha \\ f_\beta = i_{\beta ref} - i_\beta \end{cases} \tag{6}$$

To obtain the control law the control vector to be selected must ensure the stability condition (7). Therefore, if $f_\alpha > 0$, then its time derivative $\dot{f}_\alpha$ must be negative to ensure stability. This reasoning also applies for f_β. For example, if $f_\alpha > 0$ and $f_\beta > 0$, this means both i_α, i_β currents must be increased. Therefore, as the current derivatives in (4) are proportional to $V_o[\Gamma A\ \Gamma B\ \Gamma C]^T$, the time derivatives $\dot{f}_\alpha$, $\dot{f}_\beta$ will be proportional to $-V_o[\Gamma A\ \Gamma B\ \Gamma C]^T$, and therefore to increase the i_α, i_β currents a vector with non-zero α, β components in the first quadrant of Fig. 2 must be chosen (vectors 25, 22, 13, or 26).

$$\begin{cases} f_\alpha \dot{f}_\alpha < 0 \\ f_\beta \dot{f}_\beta < 0 \end{cases} \tag{7}$$

As there are 27 vectors to choose from, the f_α, f_β, values must be quantized in 5 levels each, creating variables λ_α, $\lambda_\beta \in$ {-2, -1, 0, 1, 2} to be able to have 5×5 = 25 distinct positions decision tables, enough considering there are only 19 distinct vector affixes.

To quantize variables $\lambda_\alpha, \lambda_\beta \in$ {-2, -1, 0, 1, 2} in five levels, an extension of [32] could be used, or the stability condition (7) can be applied directly, given a small allowed current ripple Δi, as in [33]. However, it is also convenient to use two multilevel hysteresis comparators, with five levels

each, to output the λ_α, λ_β variables to be applied in the voltage vector modulator to select the most appropriate vector. This approach ensures the controller robustness as the sliding surfaces neither the control laws are dependent on the three-phase T-Type *qZVSI* parameters

A. T-Type QZVI Source in Normal Condition

The choice of the voltage vector in the modulator will be function of the five values of each of the λ_α, λ_β variables. Operation in normal faultless conditions or in fault tolerant modes will also condition the choice of the voltage vector, as well as the need to balance the capacitors voltages.

In normal faultless operation, the need to balance the capacitors voltages dictates the use of Tables II and III. They give the voltage vector to be selected as a function of λ_α, λ_β variables of the sliding mode current controller and relative value of the two capacitor voltages V_{C2}, V_{C3}.

As an example, suppose that λ_α, λ_β variables have the values $\lambda_\alpha = 1$, $\lambda_\beta = 1$. Consider also that the capacitor C_2 voltage (V_{C2}, fig. 1) is higher than the capacitor C_3 voltage capacitor (V_{C3}), then table II should be used and the voltage vector 26 should be selected. Otherwise, if $V_{C2} < V_{C3}$ then table III shows the voltage vector 13 should be used.

TABLE II. SWITCHING TABLE FOR $V_{C2}>V_{C3}$, IN NORMAL CONDITIONS

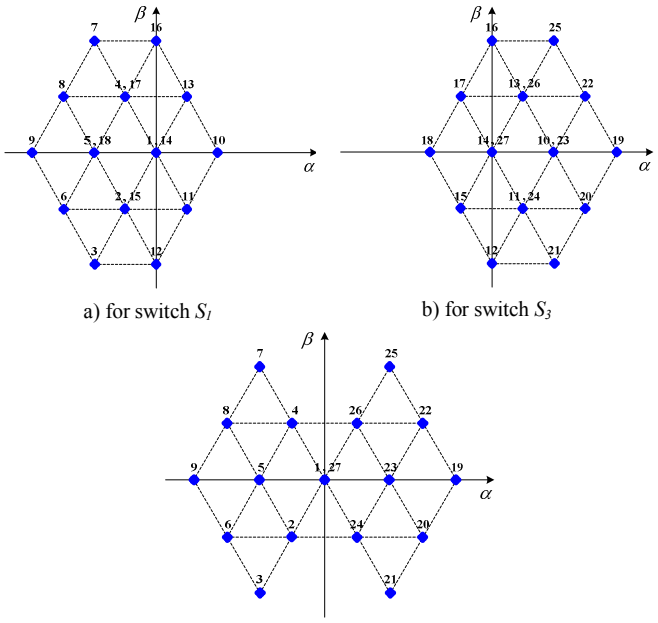
$\lambda_\beta \setminus \lambda_\alpha$	-2	-1	0	1	2
-2	3	3	12	21	21
-1	6	15	15,24	24	20
0	9	18	1;14;27	23	19
1	8	17	17,26	26	22
2	7	7	16	25	25

TABLE III. SWITCHING TABLE FOR $V_{C2}<V_{C3}$, IN NORMAL CONDITIONS

$\lambda_\beta \setminus \lambda_\alpha$	-2	-1	0	1	2
-2	3	3	12	21	21
-1	6	2	2,11	11	20
0	9	5	1;14;27	10	19
1	8	4	4,13	13	22
2	7	7	16	25	25

B. T-Type QZVI Source in Fault Tolerant Condition

When there is a fault in one of the power semiconductors, there is a reduction of the number of voltage vectors, since some switching combinations are now not possible. The impact on the performance of the converter is different, depending upon the power semiconductor under fault. Let´s see the three-possibilities for the first leg (*A*). If the fault is in the upper or lower power semiconductor (S_1 or S_3) then some higher amplitude voltage vectors will be affected. Fig. 3 a) and b) shows the *AC* voltage vectors in the plane of the $\alpha\beta$ coordinates when there is a fault in those switches. So, for example in the case of the upper power semiconductor, vectors 19 to 27 will not be available. Due to that, there will be an inappropriate choice of the vectors, as well as it is not possible to apply the required voltage to ensure that in the positive side of the current reference the measure current follow it. In this way, two actions must be performed in this condition. First, a new choice of the voltage vectors, and second, the increase of the amplitude of the voltage vectors to provide the necessary amplitude to ensure that the current follows the references. The new choice of vectors in the case of a fault in power semiconductor S_1, the selected voltage vector function of the current controller and capacitor voltages will now be given by Tables IV and V.



a) for switch S_1 b) for switch S_3

c) for switch S_2

Fig. 3. AC voltage vectors in the plane of the $\alpha\beta$ coordinates when there is a fault in the switches.

TABLE IV. SWITCHING TABLE FOR $V_{C2}>V_{C3}$, FOR A FAULT IN THE UPPER POWER SEMICONDUCTOR S_1

$\lambda_\beta \setminus \lambda_\alpha$	-2	-1	0	1	2
-2	3	3	12	11	11
-1	6	15	15,24	11	11
0	9	18	1;14	10	10
1	8	17	17,26	13	13
2	7	7	16	13	13

TABLE V. SWITCHING TABLE FOR $V_{C2}<V_{C3}$, FOR A FAULT IN THE UPPER POWER SEMICONDUCTOR S_1

$\lambda_\beta \setminus \lambda_\alpha$	-2	-1	0	1	2
-2	3	3	12	11	11
-1	6	2	2,11	11	20
0	9	5	1;14	10	10
1	8	4	4,13	13	13
2	7	7	16	13	13

The increase of the amplitude of the voltage vectors will be ensured by the increase of the shoot through duty-cycle. Increasing the shoot-through time duration all vectors different from zero will increase their amplitude (Fig. 4). For example for a fault in power semiconductor S_1, in the limit the increase must be made in order to ensure that the amplitude of vectors 10, 11 and 13 become nearly the same of the previous amplitude of the vectors 19, 21 and 25.

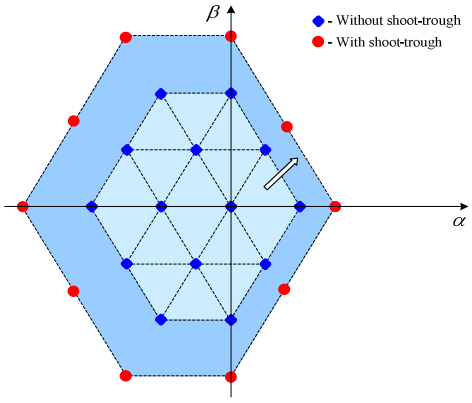


Fig. 4. AC voltage vectors in the plane of the $\alpha\beta$ coordinates.

In case of a fault in the power switches that are connected to the middle point (S_2, S_5, S_8), the impact on the performance of the converter is smaller (Fig. 3 c)). The number of missing vectors is lower than for the previous cases. Moreover, the vectors with higher amplitude will not be affected. Hence, in this case, it is not required to increase the shoot-through duty cycle. However, the choice of vectors must be changed in order to ensure the best performance of the converter. Thus, for this fault condition, the adopted voltage vector function of the current controller and capacitor voltages will be given by Tables VI and VII.

TABLE VI. SWITCHING TABLE FOR $V_{C2}>V_{C3}$, FOR A FAULT IN THE POWER SWITCH S2.

$\lambda_\beta \setminus \lambda_\alpha$	-2	-1	0	1	2
-2	3	3	24	21	21
-1	6	6	24	24	20
0	9	9	1;27	23	19
1	8	8	26	26	22
2	7	7	26	25	25

TABLE VII. SWITCHING TABLE FOR $V_{C2}<V_{C3}$, FOR A FAULT IN THE POWER SWITCH S2.

$\lambda_\beta \setminus \lambda_\alpha$	-2	-1	0	1	2
-2	3	3	2	21	21
-1	6	2	2	20	20
0	9	5	1;27	19	19
1	8	4	4	22	22
2	7	7	4	25	25

The shoot-through state duty-cycle is generated by the implementation of a carrier signal that is compared to a reference defined by the needed amplitude of vectors. The block diagram is presented (Fig. 5).

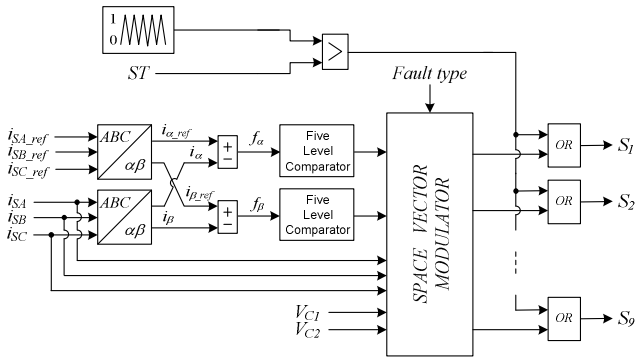


Fig. 5. Block diagram of the proposed control system.

III. RESULTS IN NORMAL AND FAULT TOLERANT CONDITION

To test the proposed control system for the three-phase T-Type *qZVSI* in Fig. 1, the parameters listed in table II were used. Several simulations in *Matlab/Simulink* are presented hereafter.

TABLE VIII. PARAMETERS OF THE SYSTEM

Input *DC* voltage	250 V
Capacitors C_1 and C_4	400 µF
Capacitors C_2 and C_3	1000 µF
Inductors L_1, L_2, L_3 and L_4	200 µH
Inductor Load L_o	10 mH
Resistor Load R_o	10 Ω

A first test simulates a fault in the power semiconductor S_1. Fig. 6 presents the *AC* current waveforms and capacitor C_2 and C_3 voltages before and after the fault without using the fault tolerant strategy (fault at t = 0.6 s). The results show that after the fault there is a huge distortion in the *AC* current i_1, while the other two phase currents are also distorted. The distortion is much more visible in the positive side of the phase *A* current i_1, which is clearly understandable since it is not possible to apply the maximum *DC* voltage at that phase. Moreover, since the adopted vectors are no more associated to the positive quadrants of the α axis, phase *A* current can never become positive. Regarding the capacitors voltage balance, it is seen that an important ripple appears. However, they average values still remain acceptably similar. This is due to the fact that in the negative side of the phase *A* current, all the required vectors are available, the modulator is able to choose vectors to ensure the voltage balance.

Fig. 7 shows the *AC* current waveforms and capacitor C_2 and C_3 voltages before and after the same fault now using the proposed fault tolerant strategy (fault at t = 0.6 s). From this figure it is seen that the distortion of the phase *A* current i_1 current is strongly reduced. Some distortion remains, especially in the positive side of the phase *A* current. Although the modulator chooses the correct vectors their amplitude is not enough to increase the current for the required value. Analyzing the voltage balance between capacitors C_2 and C_3 it is seen that they are perfectly balanced before the fault, but after it an important ripple appears. However, with the increase of the shoot-through duty cycle (Fig. 8) the currents recover

their low initial THD and the ripple and imbalance of the capacitors voltages decreases.

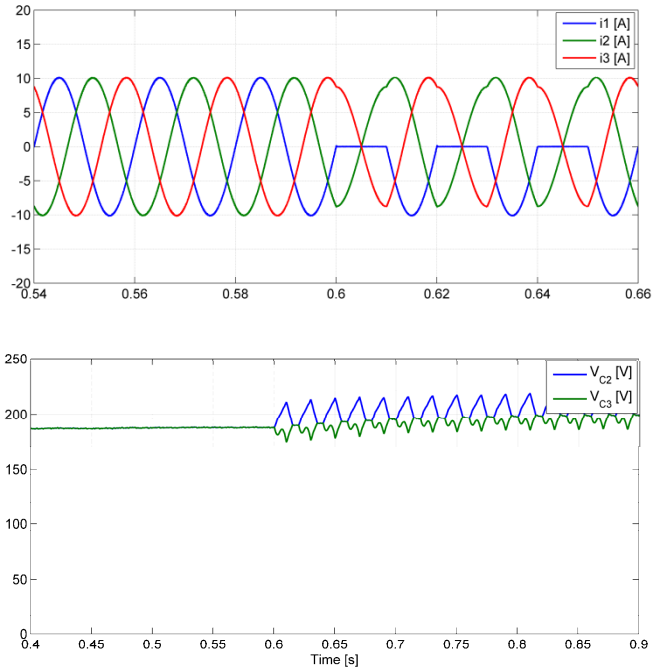


Fig. 6. Simulation waveforms of the *AC* currents before and after a fault in S_1 without the use of the fault tolerant strategy.

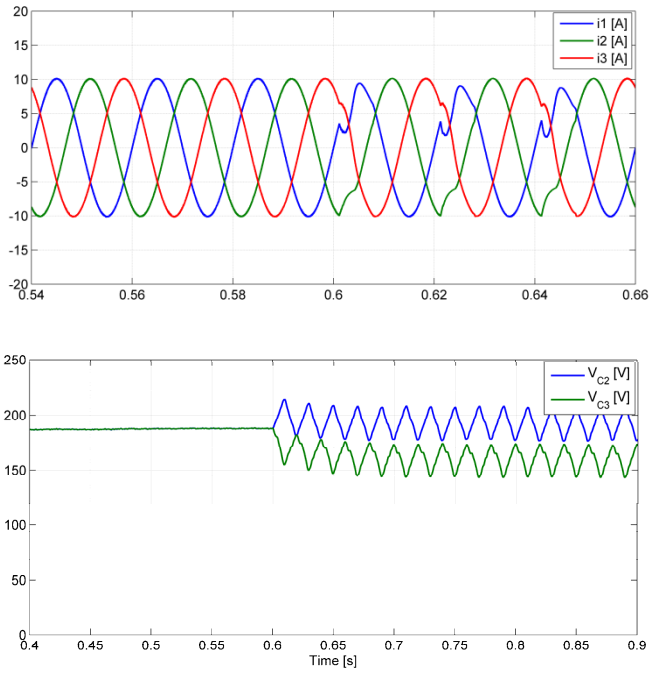


Fig. 7. Simulation waveforms of the *AC* currents and C_2 and C_3 capacitors before and after a fault in S_1 with the use of the fault tolerant strategy and without increase of the shoot-through duty cycle.

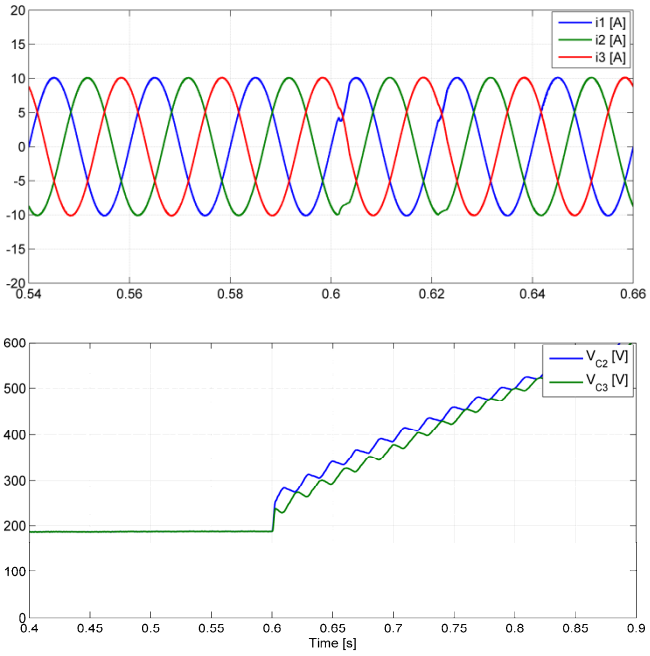


Fig. 8. Simulation waveforms of the *AC* currents and C_2 and C_3 capacitors before and after a fault in S_1 with the use of the fault tolerant strategy and with increase of the shoot-through duty cycle.

IV. Conclusions

In this paper a fast and robust controller to operate the three-phase T-Type *qZVSI* in normal and fault tolerant operation was presented. The developed controller was based on the combination of a sliding mode current controller with a voltage vectorial modulator. It was found that the strategy to select the vector voltage modulator must be adapted to the possible fault types of power semiconductors. Depending on the faulty power semiconductor, in fault tolerant mode the boost operation of the *qZVSI* should also be regulated in order to compensate the reduction of the available voltage vectors. The proposed vectorial modulator considers the above factors in order to achieve the fault tolerant operation without reduction of the injected power. The balance between the *DC* capacitor voltages was considered, in normal operation as well as in fault tolerant mode. The capabilities described by the proposed system were verified through simulation tests. Several results in normal and fault condition were presented confirming the expected results.

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